Low-Power QPSK Transmitter Based on an Injection-Locked Power Amplifier

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***Abstract*—An injection-locked frequency divider was used as a quadrature phase-shift keying (QPSK) modulator by exploiting the property that a polarity flip of the injected signal results in a phase shift of 90 degrees at the output. Furthermore, the power amplifier was integrated with the divider by adding a transformer to couple to the antenna. Combining these two ideas resulted in a high-efficiency, high-bandwidth QPSK transmitter, capable of operating at up to 120 Mbit/s and delivering 1.3 mW output power with a system efficiency of 38%.**

I. Introduction

Constant envelope modulation schemes, such as quadrature phase-shift keying (QPSK), make it possible to limit the power dissipated in the RF transmitters since non-linear and high-efficiency power amplifiers (PAs) can be used. Furthermore, the PA can be simply fed by a signal coming from a voltage-controlled oscillator (VCO) without requiring any mixer to up-convert the baseband signal. Phase modulation can be generated using both closed-loop (e.g. PLL) and open-loop (e.g. phase multiplexer) architectures [1] [2]. Closed loop solutions are typically less noisy, while open loop ones allow a larger modulation bandwidth and potentially higher data rates [3] [4].

This paper presents a low-noise open-loop QPSK transmitter based on a new PA topology where the phase modulator and PA are merged into a single stage called an injection-locked power amplifier (ILPA). The presented structure exploits the property of injection-locked frequency dividers (ILFDs) to act as a phase rotator when fed by a modulated RF signal. The proposed solution eliminates the need for a multiplexer typically required in open-loop wide-band modulators and does not require multiple phases of the transmitted signal to be synthesized simultaneously. The presented QPSK transmitter offers a large modulation bandwidth, a low error-vector-magnitude (EVM), and a relatively high power efficiency.

The paper is structured as follows: section II is focused on the analysis of the ILFD as a phase modulator, section III discusses how to design an injection-locked PA, section IV describes the characteristics of the proposed prototype, and section V summarizes the measurements results.

II. Injection-locked LC Divider as a Modulator

A. Theory of operation

Quadrature generation can be achieved using two ILFDs driven by antiphase inputs [5]. Based on this idea, a single ILFD driven by an input that flips polarity can be used to generate an output whose output phase shifts by increments of 90° (Fig. 1). This can be seen more clearly by treating the divider as a time-invariant system. A phase shift of θ at the input with frequency ω_{in} corresponds to a time shift of θ/ω_{in}. Since the system is time-invariant, the output also experiences the same time shift. This leads to a phase shift of $\theta(\omega_{out}/\omega_{in}) = \theta/2$ at the output, assuming divide-by-2 operation. Therefore, a polarity flip (i.e. 180° phase shift) at the input will correspond to a 90° phase shift at the output. This makes a divide-by-2 ILFD a suitable candidate for directly and efficiently generating QPSK signals.

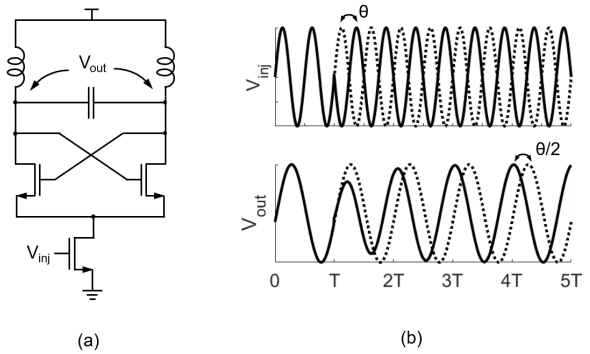

Fig. 1. (a) An injection-locked LC frequency divider with tail injection. (b) The injected signal and corresponding output voltage for an unmodulated (dotted line) and modulated (solid line) input.

A phase shift of 180° and -180° at the input are indistinguishable, but lead to different phase shifts of 90° and -90° at the output based on the analysis above. This suggests that it is possible for the phase at the output to shift in both directions. The direction of the phase shift depends on the relative position of the output frequency (ω_{out}) with respect to the resonant frequency of the ILFD (ω_o). More specifically, if $\omega_{out} < \omega_o$, the output phase will advance by 90° each time the input polarity is flipped, and if $\omega_{out} > \omega_o$, the output phase will lag by 90°. This is consistent with the intuition that an LC tank will tend to oscillate at its resonant frequency. Because the output phase only shifts in one direction by steps of 90°, we may require up to three polarity flips at the input to transition between any two arbitrary QPSK symbols.

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B. ILFD modulation bandwidth

The modulation bandwidth of the ILFD is limited by the settling time of the output phase and the minimum time between two polarity flips at the input that produce two successive 90° shifts at the output. Assuming class B biasing of the input, a first-order approximation for the time constant associated with the output phase change is

$$\tau = \frac{2Q}{\omega_o} \tag{1}$$

where Q is the quality factor of the tank, and ω_o is the resonant frequency of the tank. From (1), it is clear that a lower Q will result in a shorter settling time. The impact of the quality factor will be discussed in the PA section since it will determine also the capability of the ILFD to work efficiently as a PA. To give an idea, assuming $Q = 4$ (which will be a reasonable choice in the proposed design) and $\omega_o = 2\pi \cdot 2.4 \times 10^9$ rad/s, we get a settling time of roughly 0.5 ns. This corresponds to a 1% settling time of $4.5\tau = 2.3$ ns. This means that we can transition between consecutive symbols at roughly 400 MHz.

To make multiple transitions, it is necessary to wait a certain amount of time before flipping the input polarity again in order for the phase shift to proceed as desired. If successive polarity flips occur too quickly, the oscillator will not have time to respond and the output phase will revert to its original value. We define the minimum switching time as the minimum time between two polarity flips for proper operation. This can be calculated by noting that the phase shift will continue in the same direction if the instantaneous output frequency at the time of the polarity flip is on the same side of the resonant frequency as the steady-state output frequency. Assuming exponential settling of the output phase, an estimate of the minimum switching time is

$$t_{min} = \frac{2Q}{\omega_o} \ln \left| \frac{\pi}{4Q \frac{\Delta\omega}{\omega_o}} \right| \tag{2}$$

where $\Delta\omega$ is difference between the output frequency and the resonant frequency. To decrease the minimum switching time, it is preferable to operate with an output frequency not too near the resonant frequency. However, it must still be within the locking range of the ILFD. Also, operating too close to the edge of the locking range leads to a drop in the output amplitude. Thus, selecting an output frequency somewhere in the middle would be optimal. With the same parameters as above and a deviation from the resonant frequency of 4%, the minimum switching time is roughly 0.9 ns. As noted previously, we need a maximum of three transitions to move between two arbitrary QPSK signals. The first two transitions can occur at the minimum switching time, while the final transition should be given enough time to fully settle (i.e. within 1%). This results in a minimum symbol period of around 4.1 ns, or a theoretical maximum data rate of 240 Msymbols/s. However, this neglects other factors which may limit the speed, such as the spectral considerations.

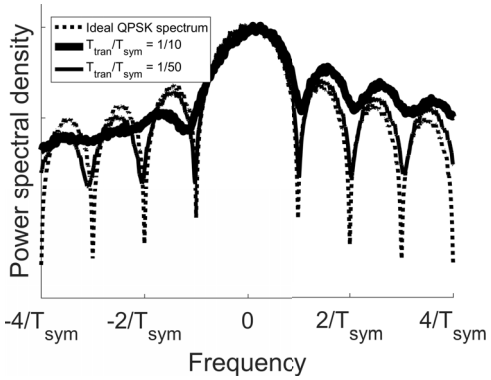

Fig. 2. Simulated output spectra for various ratios of transition time (T_{tran}) and symbol period (T_{sym}).

C. Spectrum of the transmitted signals

If the transition time is small compared to the symbol period, the indirect transitions from one symbol to the next would be virtually unnoticeable and the output spectrum would match up closely with that of an ideal QPSK output. As the transition time becomes a significant fraction of the symbol period, an asymmetry appears in the output spectrum (Fig. 2). It can be seen that when this ratio is large, the side lobes drop off more slowly. This could be an issue because the resulting signal may not have sufficient attenuation outside the main lobe to meet the transmit mask requirements.

To reduce the effect of these non-idealities, the transition period must be much shorter than the symbol period. In other words, the system needs to be oversampled. This can be easily achieved with the proposed design while maintaining a high data rate because of the high bandwidth as described in the previous subsection.

III. Combining PA with Divider

The last component of the transmitter chain is the power amplifier, which delivers the signal to the antenna at the required power level. In this work, the idea is to use the divider as a non-linear power amplifier fed by a modulated signal around twice the output frequency. The divider is coupled to the antenna through an integrated transformer resonating around the desired output carrier frequency. This solution removes the need of having a separate power amplifier in the system and also performs differential to single-ended conversion.

A. Efficiency

Ignoring the matching network, the theoretical efficiency of the ILFD is

$$\eta = \frac{P_{RF}}{P_{DC}} = \eta_{max} \frac{V_p}{V_{DD}} \tag{3}$$

where P_{RF} is the power delivered to the load of the oscillator, P_{DC} is the total power consumption, η_{max} is the maximum efficiency and is dependent on the injection scheme, V_p is the amplitude of oscillations at the output, and V_{DD} is the supply voltage. Using a square wave with 50% duty cycle as the

injected current leads to $\eta_{max} = 2\sqrt{2}/\pi \approx 0.9$. V_p is limited by the voltage headroom required to keep all the transistors in saturation. Realistically, this corresponds to $V_p \approx 0.6V_{DD}$. To obtain the total efficiency, the expression above must be multiplied by the efficiency of the matching network, given by Han and Perreault [6] as:

$$\eta_m = 1 - \frac{Q}{Q_L} \tag{4}$$

where Q is the quality factor associated with the transformation, which in our case can be considered the resulting quality factor of the tank after accounting for the transformed impedance, and Q_L is the quality factor of the inductor in the LC tank. Therefore, it is advantageous to use a lower Q to increase the efficiency of the matching network. Note that this is also beneficial for increasing the speed of phase change. However, decreasing the Q too much would mean that excessively large currents would be needed to obtain the maximum efficiency, requiring large transistors whose parasitics would degrade the overall performance. Typical values of $Q = 4$ and $Q_L = 12$ result in $\eta_m = 0.67$. Overall, an efficiency of around 30% to 40% should be achievable with this design.

IV. Circuit Design

The ILPA was designed in 65 nm CMOS technology with a concentric on-chip transformer using the ultra-thick metal layer. The schematic is shown in Fig. 3. It was optimized for delivering around 1.5 mW to the 50 Ω load. The inductance of the primary (L_p) was 10 nH, while the inductance of the secondary (L_s) was 2.5 nH. The quality factors of the primary and secondary were 12 and 4, respectively, around 2.4 GHz. The coupling factor between the two was 0.7.

A digitally-controlled capacitor bank was designed to be tunable between 260 fF and 520 fF, with a nominal value of 440 fF for a resonant frequency of 2.4 GHz. A combination of differential and common-mode capacitors was used to shift the peak of the common-mode response away from the input frequency so that the output swing would not be too degraded. The injected current was a square wave with 50% duty cycle alternating between 0 and 10 mA. This was implemented using a current source (M_1) in series with a switch (M_2). The current source transistor used a length of 100 nm to increase the output resistance, and a V_{eff} of 150 mV, leading to a width of 20 µm. The switch used a length of 60 nm and a width of 36 µm for a maximum V_{DS} of around 100 mV. To minimize the V_{DS} across the switch, a low-V_T device was used and the body was tied to the source to eliminate the body effect and minimize the threshold voltage. This allowed for larger voltage swing at the output for increased efficiency. The gate capacitance of the switch is driven by a 4.8 GHz signal so it is a significant source of power consumption in the circuit. With the current sizing, the gate capacitance is around 30 fF.

The cross-coupled pair (M_3/M_4) used a length of 60 nm and a width of 48 µm — large enough to ensure that the loop gain was sufficiently higher than 1 so that oscillations would start and to keep the voltage drop across them low, but also not so large that the parasitic gate capacitances significantly affect the resonant frequency.

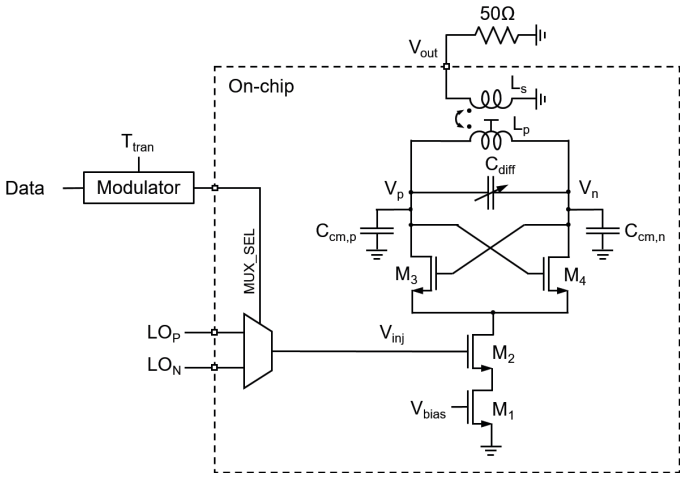

Fig. 3. Schematic of the proposed transmitter. The multiplexer and injection-locked power amplifier are on-chip. The multiplexer selection signal is generated in software. External LOs were used as inputs.

The ILPA is driven by a pair of complementary external LO signals. A multiplexer selects between the positive or negative LO signal and is driven by a post-processed input (generated in software) that results in the desired pattern at the output. The output of the multiplexer is connected to the switch in series with the current source and controls the injected current.

V. Measurements

To test the maximum modulation bandwidth, we use a sine wave from the Agilent MXG Analog Signal Generator (N5183A). This does not allow for arbitrary input data sequences as the output can only cycle from one QPSK symbol to the next, but this method still allows for a rough estimate of the maximum data rate that could be supported. The reason for doing so is because our vector signal generator can only output a digital bitstream at 50 MHz. Due to the oversampling required by our design, this would only allow us to test at data rates that are a fraction of this value. The resonant frequency was set to 2.4 GHz and the injected signal was set to 4.4 GHz for an output frequency of 2.2 GHz.

The chip micrograph is shown in Fig. 4(a). The total die area was 1 mm^2 while the active area was 0.24 mm^2. The majority of the active area was taken up by the transformer.

A. Efficiency

The ILPA achieved a maximum system efficiency of 38% while delivering 1.3 mW to the load (Fig. 4(b)). The divider consumed 3 mW, while the multiplexer consumed 0.4 mW. However, this did not include the input LO power since an external LO was used.

B. Maximum modulation bandwidth and EVM

The modulator maintained functionality with polarity flips at a frequency of up to 360 MHz (Fig. 5(a)), or every 2.8 ns,

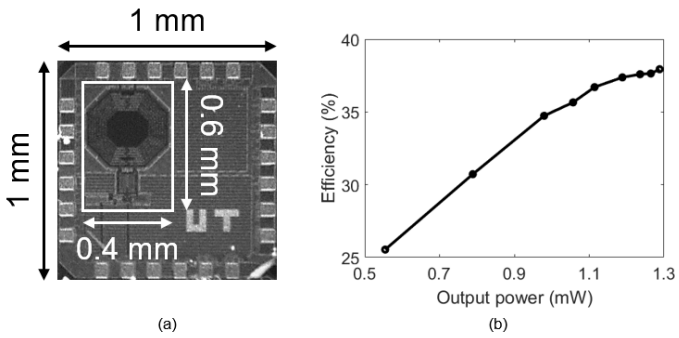

Fig. 4. (a) Chip micrograph. (b) Efficiency vs. output power.

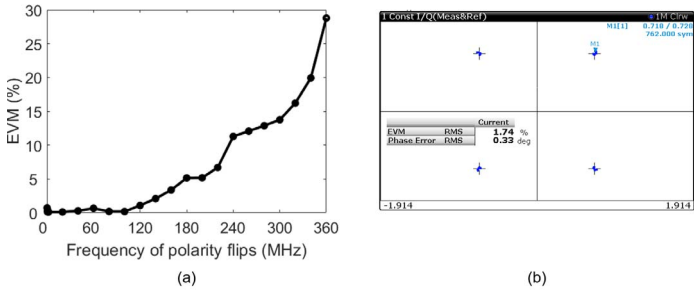

Fig. 5. (a) EVM vs. frequency of polarity flips of the injected signal. (b) Constellation diagram with polarity flips at 150 MHz.

which is close to the predicted 1% settling time. However, to maintain a reasonable EVM of around 5%, the polarity flips need to be slowed down to around 180 MHz. Since up to three polarity flips are required to transition between two QPSK symbols, a conservative estimate of the maximum modulation bandwidth would be (180 MHz)/3 = 60 Msymbols/s or 120 Mbit/s. The actual upper bound on the modulation bandwidth could be higher because only the final transition needs to fully settle.

The constellation diagram for polarity flips at 150 MHz, corresponding to an equivalent data rate of 100 Mbit/s, is shown in Fig. 5(b). The EVM at this data rate was measured to be 1.74%.

C. Phase noise

The ILPA is still a frequency divider, so under locked conditions, the phase noise is mainly determined by the phase noise of the input LO (Fig. 6). Using the external LO, the phase noise is -136 dBc/Hz at 1 MHz offset.

The results are summarized in Table I. Compared to other designs, ours can handle higher data rates, while also achieving higher efficiency and low EVM.

VI. Conclusion

An efficient QPSK transmitter based on an injection-locked LC power amplifier designed in 65 nm CMOS technology was presented. The PA was merged with an injection-locked LC divider by using an integrated transformer to couple to the antenna. It delivered up to 1.3 mW of output power with a system efficiency of 38% and a maximum data rate of 120 Mbit/s. The EVM was 1.74% at an equivalent data rate of 100 Mbit/s.

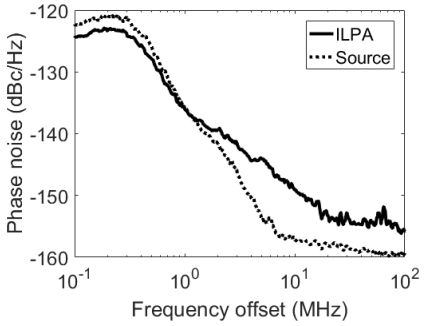

Fig. 6. Phase noise of the ILPA and the driving LO source.

TABLE I
Comparison Table

	[1]	[2]	[3]	[4]	This work
Frequency (GHz)	2.9-4.0	0.405-0.406	0.915	0.9	2.4
Modulation	QPSK	QPSK	QPSK/ O-QPSK	QPSK/ 16-QAM	QPSK
Technology	65 nm	0.13 µm	0.18 µm	65 nm	65 nm
Active Area (mm^2)	0.52	N/A	0.28	0.08	0.24
Supply (V)	1.2	1.2	1.4	1.2/0.77	1.2
Output power (dBm)	N/A	-6	-3	-9/-15	+1
Power (mW)	5	2.8	5.6	2/1.3	3.4
Efficiency (%)	N/A	9.0	8.9	6.3/2.4	37.9
Data rate (Mbit/s)	20	60	100	50/100	100
EVM (%)	1.58	5.7	5.97	5.28	1.74
Phase noise at 1 MHz offset (dBc/Hz)	-110	-105	-125	-100	-136

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