Quantized Analog RX Front-End for SAW-Less Applications

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***Abstract*—A quantized analog RX front-end is presented, where the input signal is split and processed by an array of RF analog front-ends. This approach allows to expand the dynamic range of the receiver while keeping a low power and a low voltage supply. A prototype integrated in 65nm CMOS technology shows a compression point up to 10.5dBm, IIP3 between 1 to 20.5dBm and IIP2 between 45 to 75dBm, a noise figure in sensitivity equal to 1.9dB while consuming 14mW for the analog signal amplification and 37.5mW/GHz for the clock generation and distribution. The active area is only 0.25mm^2.**

Keywords—quantized analog receiver; harmonic rejection; voltage-mode LNA; high compression point; saw-less receiver

I. INTRODUCTION

Surface acoustic wave (SAW) filters are widely used in cellular systems for resilience to large unwanted interferers. SAW filters are bulky and costly off-chip components, therefore in recent years a lot of research focus has been concentrated on eliminating them, by developing high-linear receiver architectures. Three main approaches can be found in literature which try to address this problem: mixer-first architectures [1], RF N-path filters [2], and current-mode receivers based on a low-noise transconductance amplifiers (LNTAs) where voltage signal is amplified only after down conversion [3, 4]. The first two solutions allow to handle very large interferers thanks to the absence of amplifiers in the RF section, which typically introduce distortion. However, the lack of amplification results in high noise figures (NF), and the large amount of switching in N-path filters requires high power consumption in the frequency generation. For this reason, (LNTA) followed by passive current mixers are the most common approach. Transformers can be used at the input to boost the input swings which are otherwise limited to the power supply [4]. However, current-mode operation of LNTA has some inherent disadvantages. First of all, it requires the mixer switches to have very low values to (down to a few ohms) to prevent the LNTA output compression. Then, the overall flatness of the gain depends on matching of the nMOS and pMOS and is susceptible to PVT variations. Moreover, current-mode operation is inherently less power efficient than the voltage-mode because voltage signal swing is maintained at level much smaller than supply [5]. To increase the power efficiency, a voltage mode LNA can be implemented as proposed in [6] where the output impedance is shaped by impedance up-conversion preventing large interferers from saturating the output. Yet, compression point cannot reach values as high as in current-mode receivers.

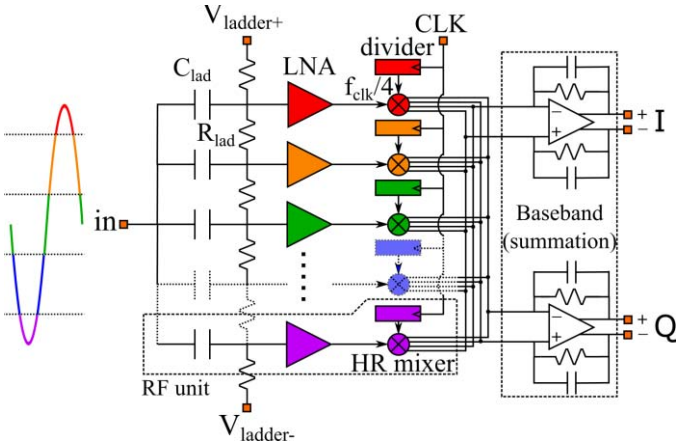

Fig. 1. Overall system architecture.

In this work, we present a novel receiver architecture based on the quantized amplification concept introduced in [7]. Receiver (RX) front-end is sliced in multiple RF units each amplifying and down-converting only a portion the input signal. With this approach, even if each RF unit has very limited compression point, the overall receiver can handle voltage signals even larger than the supply voltage (without requiring any inductor or transformer). In addition, the proposed voltage-mode approach has the following benefits: a higher power efficiency compared to current mode solutions, a straight forward harmonic rejection scheme, high IIP3 and IIP2 even when the RX front-end implemented is single-ended, and the possibility to reconfigure the dynamic range of the receiver.

The paper structure is as follows: Section II describes the system architecture, section III provides experimental results, and section IV concludes the paper.

II. SYSTEM ARCHITECTURE

Fig. 2. shows the conceptual system architecture of the proposed receiver. It is composed of N RF units, each one dedicated to amplifying a portion of the input signal, and a single baseband unit (I and Q) summing and filtering the outputs of RF units. The quantization of the signal is obtained by shifting the dc at the input of each unit by a resistive ladder, so that each unit

amplifies a different portion of the input signal. In this way, while the single RF unit has a limited input range, the overall RX front-end covers much larger input range. The input signal is ac coupled through ladder capacitors C_{lad}, which also low-pass filter the noise of the ladder resistors.

The input range of a single unit is defined by its output swing divided by gain. For example in this case the rail-to-rail output of single LNA is 0.8V and gain is 8, therefore input range is 100mV. Therefore, it is sufficient to use 8 RF units to cover the whole supply voltage range. On the other hand overlapping the input ranges results in flat gain and better linearity [7], therefore in this work 100 RF units are used. This does not come at the expense of larger area or power, as also demonstrated in [7], because the total area defined by the noise constraint of the system is simply divided into 100 slices.

In fact, expanding the input range increases the dynamic range of the system, compared to a single RF unit. The offsets between the input bias points of adjacent RF units is defined by the total voltage drop on the resistive ladder (V_{lad}), therefore it is possible to reconfigure the input range and the gain of the receiver, and even increase the input range beyond the supply voltage of the LNA. This is illustrated in Fig. 2., where the virtual gain characteristics of the RX front-end (obtained from sum of all LNA output voltages) is plotted for V_{lad} voltages from 0 to 1V. Smaller V_{lad} voltages correspond to larger gain and lower NF, but also a lower compression point, while larger V_{lad} voltages correspond to higher compression point, but lower gain and larger NF. In general increasing the compression point in such system corresponds to a larger dynamic range, because the maximum signal power increases quadratically, while the noise power increases linearly with the expansion of the input range. Therefore, V_{lad} can be reduced in sensitivity and increased in the presence of large blockers, which makes the receiver adaptable to various scenarios.

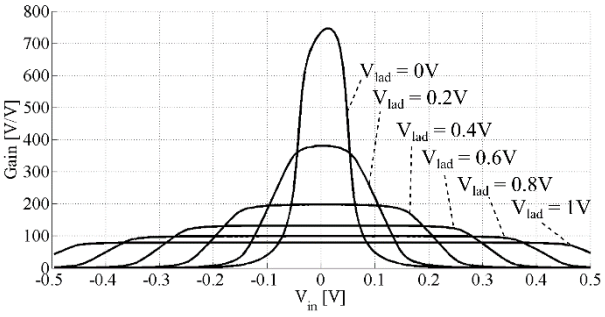

Fig. 2. Simulated virtual gain characteristics of the receiver.

In addition to the LNAs, each RF unit contains a harmonic rejection mixer and divide-by-four clock divider generating the phases required to cancel 3rd and 5th harmonics of the LO signal. Mixers contain high impedances converting LNA voltages to currents. Output currents of all RF units are added in two differential baseband TIAs (I and Q).

Fig. 3. shows the detailed schematic of the RF unit. LNA is an inverter based resistive-feedback amplifier, where the feedback resistor is 3-bit adjustable between the values 8kΩ to 64kΩ. This facilitates matching under different gain configurations.

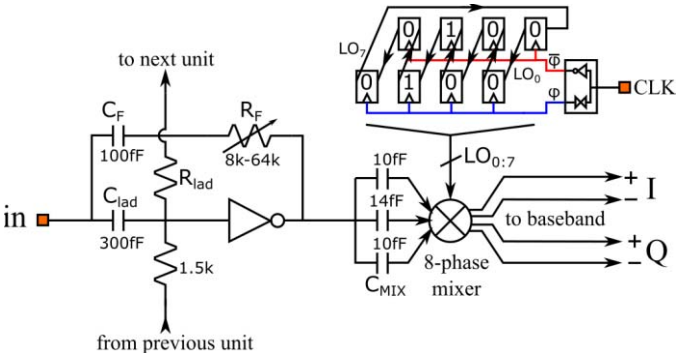

Fig. 3. RF unit's schematic.

LNA is followed by capacitive high impedance load, converting its output voltage to a current entering the passive mixer. Three different capacitors are used for harmonic rejection as will be explained later, but in general impedance of these capacitors is larger than the resistance of the mixer switches, which limits the voltage swing on mixer switches for better linearity. Mixer is driven by LO signals generated with a divide-by-four clock divider. Divider is composed of 4 high-level and 4 low-level triggered latches generating 8-phase LO signals with 25% duty cycle. Divider is fed through single clock signal at $4\times f_{LO}$, and internally generates the clock-bar required to drive latches.

Fig. 4.a. shows the schematic of the harmonic rejection mixer. Considering that LNA generates a voltage output, a current proportional to the transconductance of the three capacitors flows through each capacitance. These currents are directed to one of the baseband terminals, as nMOS switches of the mixer are toggled by the 8 LO phases shown in Fig. 4.b. This creates effective LO_I and LO_Q signals as shown in Fig. 4.c., which corresponds to a sine wave sampled and held at 8 points if $C_2 = 1.41C_{1a,b}$. Such a sine wave does not have 3rd and 5th harmonics as required. Voltage-mode harmonic rejection has several benefits over the conventional current-mode used in [3, 4]. First of all, scaling done in impedance rather than in 8 different opamps or G_M cells which saves area and power. Moreover, capacitance ratios can be made more precise than matching active devices in fine technologies. Then, LO phases can be overlapped, therefore it is possible to use 25% duty-cycle waveform rather than 12.5% as required by current mode. Wider pulses are less vulnerable to jitter and rise/fall times therefore are more desirable at higher frequencies. Finally, the compression point is not sensitive to mixer resistance, because it is preceded by a larger impedance. Also note that any non-linearity introduced by the mixers are averaged among RF units just like the transfer-characteristics of LNA, and does not cause a significant issue.

Baseband is implemented as a TIA composed of a 3-stage feed-forward compensated differential amplifier with parallel feedback resistors and capacitors of 2.5kΩ and 8pF. 60pF capacitor is placed between input terminals to provide low impedance at high frequencies beyond opamp's unity gain frequency. This capacitor provides additional filtering together with opamp's increasing input resistance at high frequencies. TIA's are designed to provide 30dB attenuation at 100MHz.

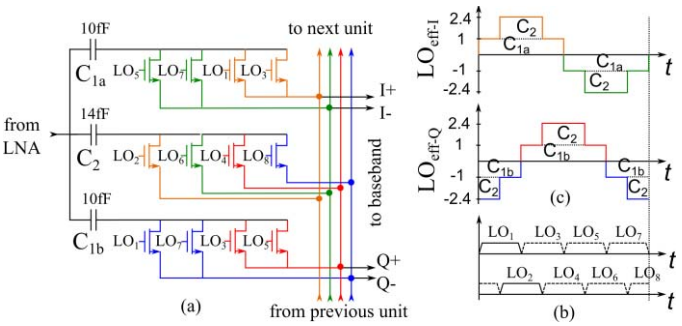

Fig. 4. a) Schematic of harmonic rejection mixer. b) 8-phase 25% duty-cycle LO signals. c) Effective LO_I and LO_Q signals.

III. Experimental Results

The chip micrograph is shown in Fig. 5. It was fabricated in 65nm CMOS technology and occupies an active area of 0.25mm^2. It was wire bonded on a board for testing purposes, losses of which were measured to be 0.5dB to 1dB from 700MHz to 1.4GHz and were de-embedded from the measurements.

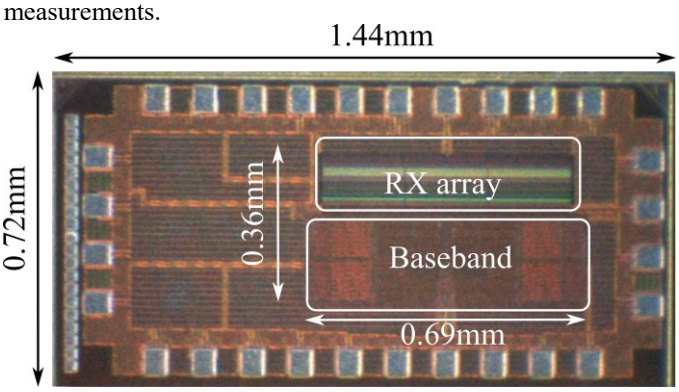

Fig. 5. Die Micrograph. Active area is 0.25mm^2.

Due to the wideband nature of the inverter amplifier the input could be matched in the range of 0.7GHz to 2GHz, however due to the incorrectly estimated parasitics, divider did not start up after 5.6GHz (corresponds to f_{LO} = 1.4GHz) and was consuming 37.5mW/GHz which was twice as much as estimated with the post layout simulations. LNA supply is 0.8V and it is consuming 9.3mA in sensitivity mode (V_{lad} = 0V) and 7.3mA in high linearity mode (V_{lad} = 1V) in presence of 10dBm blocker. The current reduces because the crowbar current in the inverters decreases with larger signals. Baseband consumes 6.5mA from a 1V supply in sensitivity and 8mA in the presence of B_{1dB} blocker.

Fig. 6.a. shows the RF gain of the receiver for different V_{lad} voltages. The gain can be adjusted within 15dBm by changing V_{lad} from 0 to 1V. Fig. 6.b. shows the baseband filtering profile. The 3dB cutoff frequency of the baseband is 15MHz, and 30dB filtering is obtained at 100MHz. Using quantized amplifier approach allows the system to be more linear for higher input powers because linearity performance relies on the averaging of transfer characteristics among multiple units.

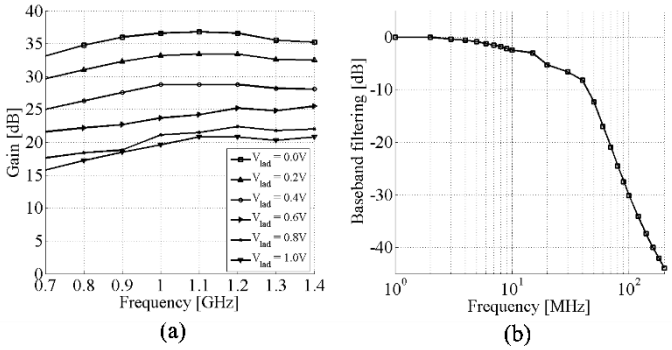

Fig. 6. (a) RF gain and (b) the baseband filtering profile.

This can be appreciated by observing IM3 and IIP3 shown in Fig. 7, and IM2 and IIP2 shown in Fig. 8, for two tone tests at 100MHz offset. With increasing signal amplitude IM3 and IM2 stop increasing with the 3rd order and 2nd order slope respectively, and flatten out until the receiver saturates. The input power at which this phenomenon occurs increases with increasing V_{lad} as expected. Such linearity is hard to characterize with the concept of IIP3 and IIP2 as they depend on signal amplitude. In general IIP3 ranging from 0 to 20dBm and IIP2 from 35 to 75dBm is achieved. Note that linearity is more critical at higher signal powers, therefore obtaining higher IIP3 and IIP2 for larger input powers as in this case is advantageous.

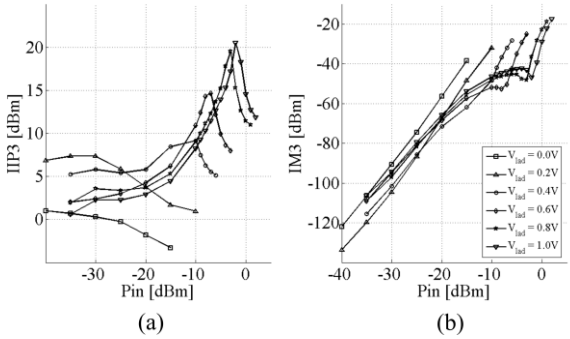

Fig. 7. (a) Measured IIP3 and (b) IM3 using two tones at 702MHz and 800MHz with f_{LO} = 900MHz.

Fig. 9. shows the P_{in} vs P_{out} of a blocker at 100MHz offset from carrier. Input compression point can be extracted from this plot which becomes -8.5dBm for V_{lad} = 0V and increases to 10.5dBm for V_{lad} = 1V.

Fig. 10.a. shows the NF of the system across the operating frequencies. It remains within 1.0-2.8dB (average is 1.9dB) until 1.3GHz and starts increasing at 1.4GHz because of dysfunctional divider. In presence of B_{1dB} blocker, the noise figure increases to a maximum of 7.9dB. Fig. 10.b. shows the increase in the 1dB compression point and the NF for increasing V_{lad}. Note that compression increases by 19dB while NF only by 13dB. This corresponds to 6dB increase in the dynamic range between the configurations for the smallest and the largest V_{lad}.

Harmonic rejection was measured to be 40-67dB for the 3rd order LO harmonic and 47-70dB for the 5th order LO harmonic.

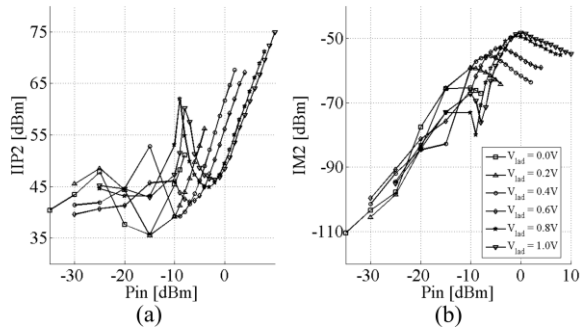

Fig. 8. (a) Measured IIP2 and (b) IM2 using two tones at 1GHz and 1.002GHz.

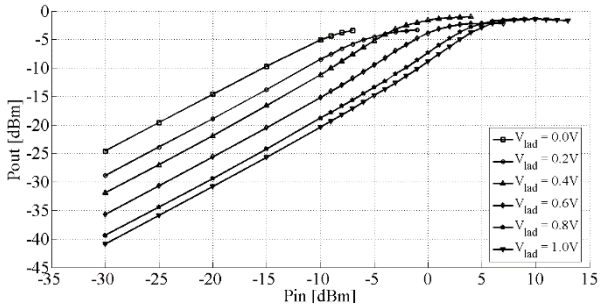

Fig. 9. Output power vs. input power of a blocker at 100MHz offset.

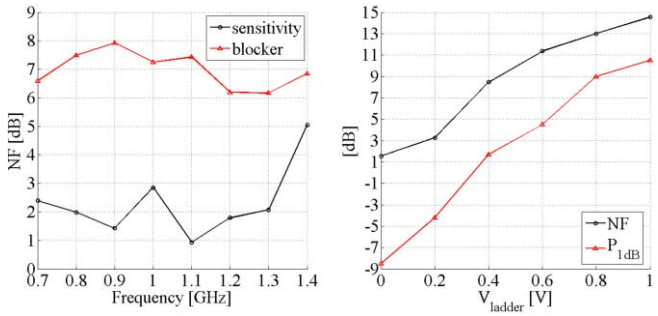

Fig. 10. (a) NF vs. frequency evaluated at sensitivity and in presence of -9dBm blocker (V_{lad} = 0). (b) NF vs. V_{lad} evaluated at 900MHz, and the 1dB compression point.

Table I gives the comparison of the implemented receiver with the state of the art. Note that the presented work even though implemented in the oldest technology (i.e. 65nm), achieves the best power efficiency for the signal path (LNA and Baseband) and has the largest compression point, comparable even to differential mixer first receivers* (i.e. 12dBm) [1]. IIP3 and IIP2 values are harder to compare, as in the proposed system these values change with the input signal level, however peak IIP3 and IIP2 are still larger or at least comparable to the state of the art. Sufficient harmonic rejection is achieved without the need for multiple opamps or G_M cells in baseband. The only drawback is the excessive power consumption in the LO path, however this was intentionally designed to overcome the reciprocal mixing, in addition to the incorrectly estimated parasitic capacitances as mentioned earlier and is not the shortcoming of the introduced idea.

* Not in the comparison table because mixer first receivers have no active front-end.

TABLE I. COMPARISON WITH THE STAHE OF THE ART

	This work	***[3]***	***[4]***	***[6]***
Topology	Quantized RX	Noise Cancelling	Transform. -LNA	Voltage-mode[a], HR
Area [mm^2]	0.25	5	0.84 (0.74[a])	0.6
Freq. (GHz)	0.7-1.4	0.6-3	1.8-2.4[a]	0.4-3
Gain [dB]	20.8[b]-36.8	NA	1.8-2.4, 1.8-2.1[a]	70
NF [dB]	1.9-2.8	1.8-3[b]	3.8,1.9[a]	1.8-3.1
NF_{blk} [dB]	6.6-7.9	7-9	7.9	14 (10[d])
IIP3 [dBm]	1-20.5[b]	10-11.5[a]	18,16[a]	3, 8[d]
IIP2 [dBm]	45-75[b]	49.5-55[a]	64,66[a]	55, 80[e]
B_{1dB} [dBm]	-8.5-10.5[b]	-6	-1.5	-13
HR (3^{rd} /5^{th}) [dB]	40-67/ 47-70	52/54	54/65	40 (70)
Supply [V]	0.8, 1, 1.2	1	1.2, 1.8	40 (75)
LO_{path} [mW]	37.5/GHz	13/GHz	3.2/GHz	6.8/GHz +5.4
LNA+BB [mW]	13.7[b]-14	30-46	23.4	14.3
Technology	65nm	28nm	40nm	28nm

[a] Differential, [b] High Linearity (V_{lad} = 1), [c] Low Noise (Vlad = 0), [d] LNA optimized, [e] Calibrated

IV. CONCLUSION

A reconfigurable quantized analog RX front-end is introduced, which increases the compression point and the dynamic range of a power efficient voltage-mode receiver. Voltage mode operation facilitates an easy harmonic rejection. Configurability of the system allows having NF as low as 1.9dB and compression point as high as 10.5dB, while consuming only 14mW in the signal path.

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