# Quantized inverter amplifier

J. Musayev and A. Liscidini

The concept of quantized inverter amplifier is introduced, where the input signal is split and amplified by an array of amplifiers. This strategy expands the dynamic range and relaxes the power demand of the following stages because the total output swing can virtually exceed the supply voltages. Moreover, using multiple amplifiers helps to linearize the input-output transfer characteristic. Simulations results confirm the presented theory.

*Introduction:* In absence of distortion, the dynamic range (DR) of an analog amplifier is limited by the maximum signal-to-noise ratio (SNR) achievable [1]. As shown in many studies [1-4], the maximum SNR for a given bandwidth Δf is ultimately limited to input peak-to-peak voltage $V_{ipp}$ and output peak current $I_{op}$ as follows:

$$SNR \cdot \Delta f = \frac{V_{ipp}^2/8}{4\mathrm{kT}\gamma/g_m} = \frac{V_{ipp} \cdot V_{ipp} g_m/2}{4 \cdot 4\mathrm{kT}\gamma} = \frac{V_{ipp} \cdot I_{op}}{16\mathrm{kT}\gamma} \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, $g_m$ is the amplifier transconductance, and γ is the noise factor of the transconductor. Usually, $V_{ipp}$ is bound by the supply voltage $V_{DD}$, while $I_{op}$ is bound by the supply current $I_{DD}$, therefore (1) can be rewritten as a function of the power drawn from the supply (P) as follows:

$$SNR \cdot \Delta f = \frac{V_{DD}\eta_v \cdot I_{DD}\eta_c}{16\mathrm{kT}\gamma} = \frac{P \cdot \eta_v \eta_c}{16\mathrm{kT}\gamma} \qquad (2)$$

where $\eta_v = V_{ipp}/V_{DD}$ and $\eta_c = I_{op}/I_{DD}$. A similar relationship is derived in [5], with instantaneous frequency instead of Δf, for the cases where the noise is band-limited by the output capacitor. It is clear from (2) that maximizing voltage swings, increases the voltage efficiency $\eta_v$ for each stage along the signal processing chain. Therefore the wanted signal is typically amplified to the rails as early as possible and maintained at this level. Unfortunately, a rail-to-rail linear amplification is hard to achieve, as devices constituting the amplifier may introduce significant distortion. Moreover, in presence of larger interferers, the maximum amplification is further limited to avoid the saturation of the amplifier. This last issue can be solved by filtering unwanted interferers before the amplification. However, in some applications, especially at RF, this is very difficult due to the lack of sharp filtering profiles and typically the wanted signal can be amplified rail-to-rail only in the base-band, after the down-conversion. In this letter, we propose a quantized inverter amplifier (QA) (Fig. 1), where the amplification is performed by using an array of unit amplifiers, each one dedicated to amplifying only a certain portion of the input signal. In this way, although the output of a single unit is still limited to $V_{DD}$, collectively the total output can exceed the supply. This allows having a voltage swing for the following stage virtually much larger that $V_{DD}$ and to increase the maximum SNR achievable (i.e. DR). Furthermore, the signal quantization allows improving the linearity of the overall transfer function since the voltage transfer characteristic of each element is averaged among multiple units.

*Quantized voltage amplifier (QA):* An amplifier with a voltage gain of A and an output between ground and $V_{DD}$ has an input range that is limited to $V_{DD}/A$ (Fig. 1*a*). In order to extend both input and output voltage ranges, the amplifier is sliced into N identical units, each consuming 1/N of the original current to maintain the same power dissipation and area (Fig. 1*b*). The output of each unit is still limited by the supply (i.e. $V_{DD}$) but now, each of them is responsible for amplifying only one portion of the input signal. To do that, an offset equal to $V_{DD}/A$ is added between the inputs of adjacent amplifiers. In such way, the characteristics are shifted by $V_{DD}/A$ so that the overall input range becomes $N \times V_{DD}/A$. At the output of QA, all the signals are added together, which leads to a virtual output range equal to $N \times V_{DD}$. One way to perform this sum without exceeding the supply is to recombine the N paths in the digital domain. This translates the burden of having a larger supply to having more bits in the output register. Since the maximum input/output signal swings have been increased by N while keeping the same power consumption, form (1) it follows that maximum SNR achievable (i.e. DR) by the QA (Fig. 1*b*) is N-times larger than for the single amplifier (Fig. 1*a*). Increasing signal power $N^2$-times and having N-times better SNR suggests that the input referred noise of QA is N-times larger than the input referred noise of the original amplifier. This is because, each unit amplifier in QA consumes N-times less current, and injects noise only when it is not saturated.

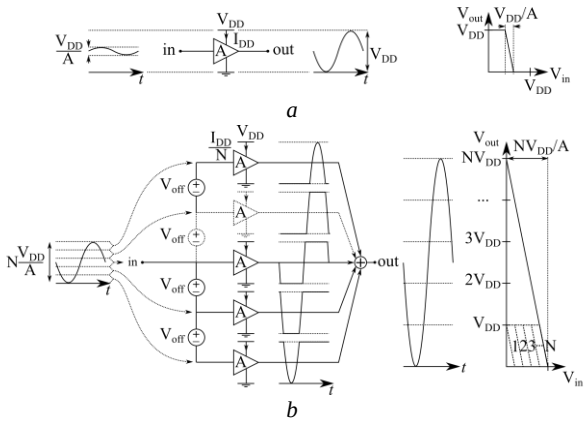


**Fig. 1** *Concept of quantized amplifier*

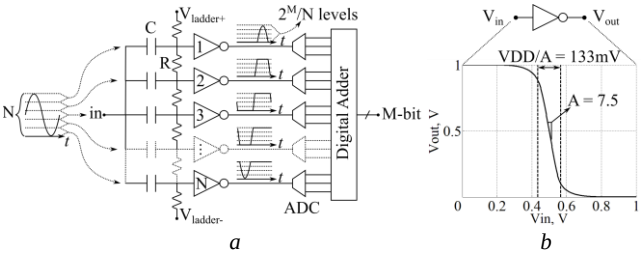


**Fig. 2** *Implementation of a quantized inverter amplifier.*
*a* Circuit diagram.
*b* DC transfer characteristics of the inverter.

*Implementation of a quantized inverter amplifier*: The proposed concept has been verified by implementing a QA through an array of inverter amplifiers in 65nm CMOS with 1V of supply, followed by an ADC to quantize and recombine the signals (Fig. 2*a*). Notice that, it is not necessary to directly quantize the outputs of inverters. Further analog signal processing (e.g. filtering or even signal down conversion) can be performed between inverters and ADCs since the recombination is a linear operation. Required dc offsets among the inverters are generated through a resistive ladder by ac-coupling the input signal. To make the noise and power dissipation of biasing negligible for a given input frequency range, the cut-off frequency of the RC bank can be reduced at the expense of area. This makes the proposed bias scheme more suitable for RF applications. Given the simulated CMOS inverter characteristic shown in Fig. 2*b*, the input range is assumed to be $V_{DD}/A$ = 133mV, where A = 7.5 is the gain of the inverter at the midpoint. Fig. 3*a* and Fig. 3*b* show the voltage transfer characteristics and gain of the inverter QA for the number of slices N from 1 to 8, where the offset is set to $V_{DD}/A$ (i.e. 133mV). Compared to the single inverter, the input range increases by N. Fig. 3*c* shows the simulated SNR×Δf for the QA as a function of N, computed at the output, in response to a 1GHz signal of the largest amplitude ($V_{ipp} = N \times 133$mV). As expected SNR increases with N, and corresponds closely with the linear relation of $SNR_{QA} = N \times SNR_{INV}$, shown with dashed lines. Notice that, this would correspond to the increase in DR, if the distortion introduced by the gain ripple observed in Fig. 3*b* was neglected. Moreover, ADCs are assumed to be ideal, with a number of bits large enough to make their quantitation noise negligible. The impact of distortion and ADCs will be discussed in the next sections.

Fig. 3*d* shows also the total current dissipation which decreases as N increases. The overall power dissipation should not depend on N for a 100% current efficient amplifier (i.e. $\eta_c = 1$), however, in this case, the inverter is not 100% efficient, since it operates in class-AB by having a direct-path current between $V_{DD}$ and ground, when both transistors operate in saturation. When N is increased each unit saturates faster,

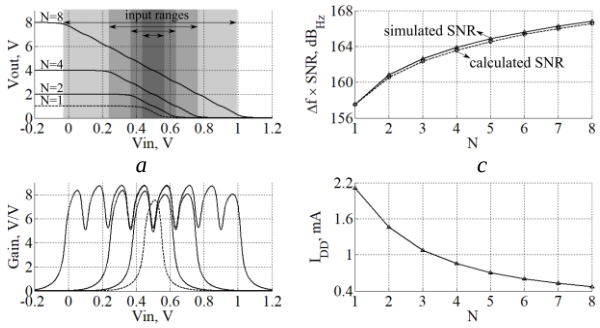


**Fig. 3** *QA implementation with inverters, for N values from 1 to 8.*
*a* $V_{out}$ vs. $V_{in}$, for an inverter (N = 1) and QA with N = 2, 4, and 8.
*b* Gain vs. $V_{in}$, for an inverter (N = 1) and QA with N = 2, 4, and 8.
*c* SNR vs. N, for a signal with $V_{ipp}$ = N×133mV at 1GHz.
*d* $I_{DD}$ vs. N, for a signal with $V_{ipp}$ = N×133mV at 1GHz.

being driven by a large input signal, and spends less time in the region where the direct-path current is consumed. This is another advantage of the QA, in the minimization of the power consumption in practical implementations.

*Linearity improvement:* The gain ripple observed in Fig. 3*b* can be greatly reduced by allowing the gain characteristics to overlap more than $V_{DD}$/A, through reducing the offsets between the inverters ($V_{off}$) by a factor of α (i.e setting $V_{off}$ = α×$V_{DD}$/A). Since this operation would decrease the input range by α, N has to be increased by the same factor to maintain the original input range. This was done in simulations of Fig. 4*a*, where a larger overlap was obtained by reducing α and increasing N to keep the same input range. The gain ripple is improved from 0.9% (α = 7.5/32, N = 32) to 0.0001% (α = 7.5/128, N = 128). Notice that, a greater overlap of the characteristics (i.e. smaller α and larger N) also increases the effective gain by 1/α, because the input range is kept constant (i.e. α×N×$V_{DD}$/A) while the virtual output range increases, being equal to N×$V_{DD}$. However, since in presence of an overlap, signals in adjacent paths are partially correlated, this increment of gain is redundant and does not lead to a benefit in terms of SNR. This explains why the comparison is Fig. 4*a* has been done by normalizing the gains by 1/α.

The linearity improvement can be appreciated by evaluating the total harmonic distortion (THD) produced as a function of the input signal amplitude $V_{ipp}$ (Fig. 4*b*). For small signal amplitudes (i.e. $V_{ipp}$ = 1mV) the THD of QA improves up to 8dB compared to the one generated by a single inverter. This improvement reaches a maximum of 64dB for larger signal amplitudes (i.e. $V_{ipp}$ = 200mV) where the single inverter is almost saturated while the QA takes advantage of larger input/output ranges.

*Digital output recombination:* The need for ADCs to perform the signal reconstruction does not represent a particular problem for applications where an analog-to-digital interface is ultimately required (e.g. wireless/wireline receivers or sensor interfaces). Indeed, because of the virtual expansion of the output range beyond $V_{DD}$, the ADCs required to recombine the QA outputs can consume less power than a single ADC driven by a single amplifier. This can be intuitively understood considering the case when the signal is sliced into N pieces without an overlap (i.e. α = 1). In this case, to reach the same DR as a single M-bit ADC, each ADC of the QA needs $2^M$/N quantization levels. As shown in [6] for the same figure-of-merit (FoM), the reduction of the DR of ADC by N times demands $N^2$ times less power. However, since in this case N

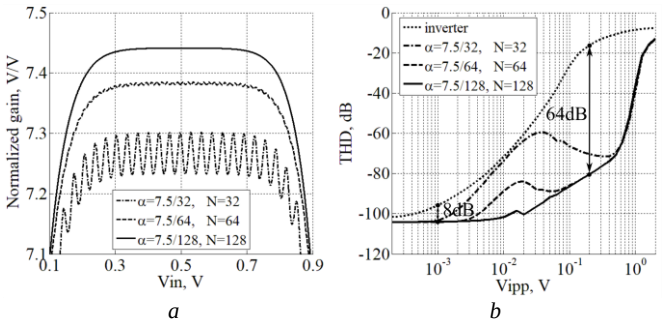


**Fig. 5** *Linearity improvement of QA with decreasing α.*
*a* Gain vs. $V_{in}$ for a QA with α = 7.5/32, 7.5/64, and 7.5/128.
*b* THD vs. $V_{ipp}$ for the inverter and a QA.

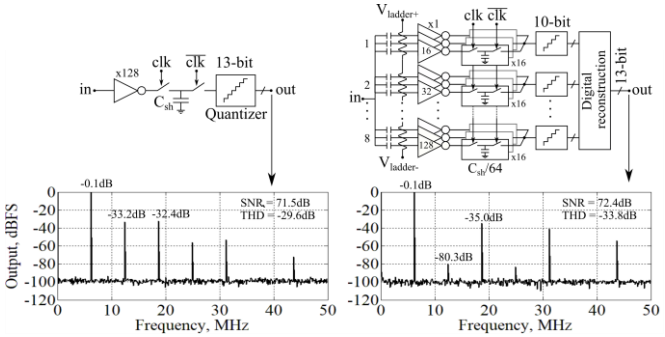


**Fig. 4:** *Transient noise simulations with a behavioral ADC model.*

ADCs are required, the overall power consumed for the analog to digital conversion will be only N times smaller compared to traditional approach. In presence of an overlap (i.e. α < 1) it is possible to verify that ideally, the power dissipation would scale down by a factor of N×α instead of N. Such benefit has been verified by a transient noise simulation of the two cases shown in Fig. 5: the cascade of a single inverter amplifier with a 13-bit ADC, and a 128-unit QA (with an overlap factor α = 1/16) followed by eight 10-bit ADCs. The resolution of each ADC in the case of the QA was relaxed by 3-bits, since N×α ≈ 8. The redundancy due to α = 1/16 allowed to recombine the QA outputs in groups of 16, while keeping a virtual expansion of the $V_{DD}$ by 8 (i.e. N×α). This allowed to use only 8 ADCs instead of 128. The recombination occurred in the sample-and-hold (SH) by merging the 16 sampling capacitors coming from the 16 QAs, as shown in Fig. 5.

The ADCs were modelled by the cascade of a noisy SH circuit and an ideal quantizer. The sampling capacitor of SH was sized to make the ADCs thermal noise limited for an overall effective number of bits (ENOB) equal to 12 [7]. In particular, the sampling capacitor of the 13-bit ADC is 64 times larger than the one of each 10-bit ADC (formed by 16 sampling capacitors in parallel). For a given FoM, such sizing would make the total power dissipation of the QA ADCs 8 times less than the power dissipation of 13-bit ADC, while keeping the same DR (or ENOB). This was confirmed by the simulation results shown in Fig. 5, where similar SNRs (72dB) were obtained in both cases for a full-scale input signal at 6.25MHz sampled at 100MHz. Notice that in this case, while the SNR is set to be dominated by the ADCs to appreciate the impact in reduction of the number of bits of QA ADCs, the linearity of the system is limited by the analog amplifier. In this case the THD is 4.2dB better in the case of the QA with an input signal N×α ≈ 8 times larger than the one feeding the single amplifier. This is an additional proof of the superior linearity of the QA, previously discussed.

*Conclusion:* Quantized analog amplification concept has been introduced. Simulations demonstrated that the SNR and linearity of an amplifier can be improved, for the given power, and that stages following the QA can benefit from the virtually expanded output voltage.

J. Musayev and A. Liscidini (*The Edward S. Roger Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, Canada*)

E-mail: javid.musayev@mail.utoronto.ca, antonio.liscidini@utoronto.ca

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