

IBM Crams Power2 onto Single Chip

P2SC Offers Incredible Memory Bandwidth, Strong FP Performance

by Linley Gwennap

While putting most of its emphasis on PowerPC products from its partnership with Motorola, IBM continues to maintain its own line of POWER processors. A relatively small team, in less than a year, took the eight-chip Power2 design (see [071301.PDF](#)) and collapsed it into a single die, delivering a powerful new product. The phenomenal integration provides manufacturing cost savings and, more important, improved performance by eliminating the overhead of chip-to-chip communication.

The new device, dubbed P2SC, is the most complex single-chip processor yet announced. It can issue and execute six instructions per cycle, two of which can be floating-point multiply-add instructions. It supports register renaming and out-of-order execution, although only for floating-point code; also, the P2SC's out-of-order design uses a primitive technique compared with the reorder buffers of more modern processors. The chip includes 160K of on-chip cache, more than any other microprocessor, for a total transistor count of 15 million.

Putting so much onto one chip requires an advanced IC process: the P2SC is the first processor to take advantage of IBM's 0.29-micron CMOS-6S process (see [090905.PDF](#)).

Even so, the die is quite large; at 335 mm², it outsizes all other microprocessors but HP's PA-8000. Although the integration effort nearly doubled the clock speed compared with the Power2, the P2SC still runs at only 135 MHz, far less than other high-performance processors. At 14.5 SPECfp95 (base), the chip outscores all competitors except the PA-8000 and Digital's 500-MHz 21164. IBM hopes to increase the performance of the P2SC with higher clock speeds in the future.

The company expects to ship P2SC systems early in the fourth quarter. Like other POWER processors, the P2SC will not be sold on the merchant market, but it may be shared with other POWER system vendors, such as Groupe Bull.

Highly Leveraged from Power2

The microarchitecture of the P2SC, shown in Figure 1, is nearly identical to that of its predecessor, the Power2. By retaining the same design, the team was able to accelerate the design effort, taking just nine months from initial concept to tape out. The most significant change is a halving of the size of the data cache and data TLB, which are 128K and 256 entries, respectively, in the P2SC. This choice was required to fit the eight-chip processor onto a single die. To support the higher clock speed, the memory and I/O buses run at half the

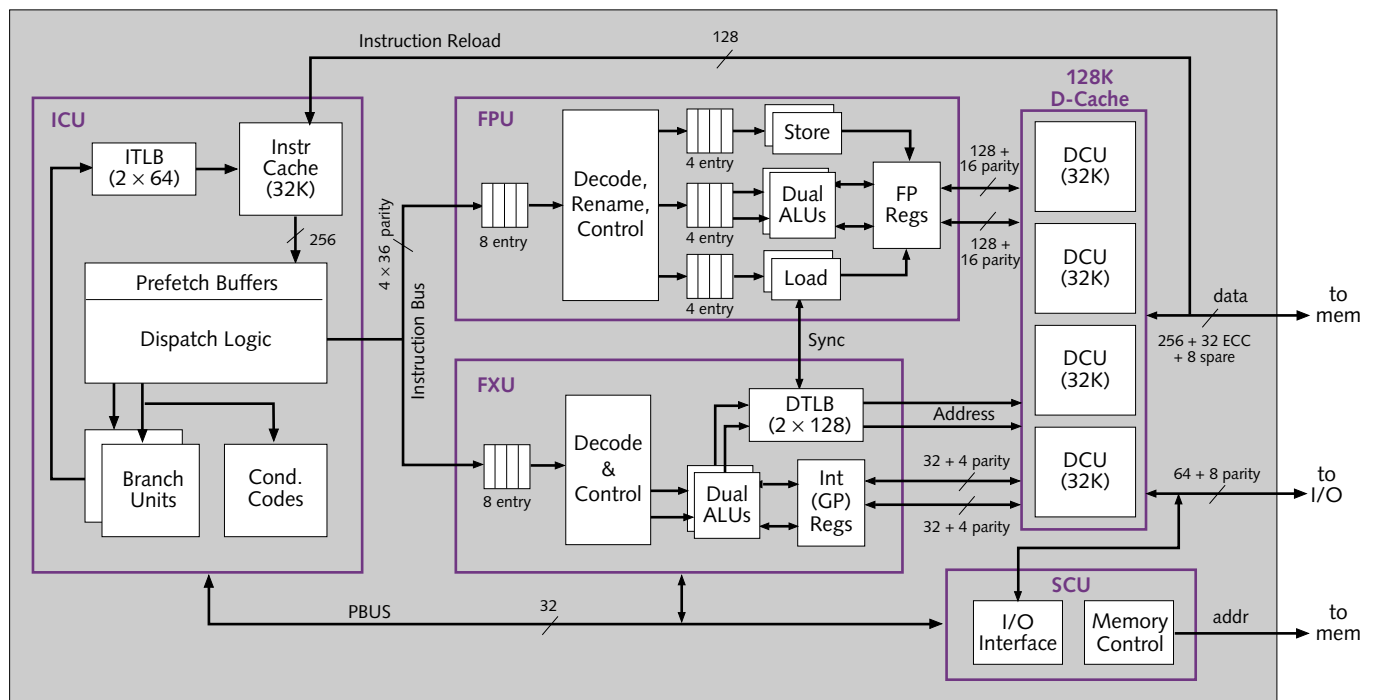


Figure 1. IBM's P2SC processor integrates a six-issue CPU with dual integer ALUs and dual FP multiply-add units; 32K of instruction cache with predecode bits; 128K of data cache; and direct interfaces to memory and I/O.

CPU core clock speed. A rarely used feature to lock TLB entries was excised.

For those unfamiliar with the Power2 microarchitecture, a quick review is in order. Instructions are fetched eight at a time from the 32K instruction cache, which also stores seven predecode bits per instruction. Up to six consecutive instructions can be dispatched per cycle, consisting of up to four integer or FP instructions and two branch or condition-code instructions. Instructions can be dispatched in the same cycle even if there is a register dependency.

The FXU (integer unit) and FPU are decoupled from the instruction-issue process by eight-entry queues. Once instructions reach the front of these queues, they are decoded, paired, and executed. Integer instructions, which include FP loads and stores, are always executed in order, but the queues allow the FPU to get out of sync with the FXU. Furthermore, each FP ALU has a single reservation station that allows a stalled instruction to wait while subsequent instructions execute out of order. In total, five instructions can be stalled (one integer, four FP) before the processor is forced to halt. On integer-only code, however, a single stalled instruction will tie up the entire processor.

The FXU can execute two instructions per cycle, which can be any combination of integer arithmetic, loads, or stores. The FPU can execute two floating-point instructions per cycle. FP add, multiply, and multiply-add are all fully pipelined with only two-cycle latencies. With dual branch units, the P2SC can also execute two branches per cycle, although one must be not taken. The chip has no dynamic branch prediction, but there is only a single-cycle penalty for a taken conditional branch, and this penalty can be avoided with adequate separation between the condition-code instruction and the associated conditional branch.

The data cache is triple-clocked to handle two CPU accesses (loads or stores) plus a cache refill (write to cache from main memory). In a sense, this part of the chip operates at 500 MHz, the speed of a competitive Alpha processor.

The key to the P2SC's performance is its direct connection to up to 2G of DRAM across a 256-bit-wide interface. This interface plugs the processor directly into a byte stream of up to 2.2 Gbytes/s, nearly twice the memory bandwidth of any other microprocessor. The chip also integrates a 64-bit I/O bus for peripheral interconnect.

15 Million Transistors Set Record

The P2SC is most impressive from a physical standpoint. The Power2 processor, built in a 0.72-micron five-layer-metal process (CMOS-4), required eight die with a total area of 1,215 mm². Even with half the cache, the design takes about 900 mm². IBM's 0.29-micron five-layer-metal CMOS-6 process shrinks that circuitry onto a 335-mm² die, shown in Figure 2. Some of the area reduction was achieved by eliminating redundant drivers from what were previously chip-to-chip signals. This change improved performance in one case by trimming a cycle from the instruction-cache reload time.

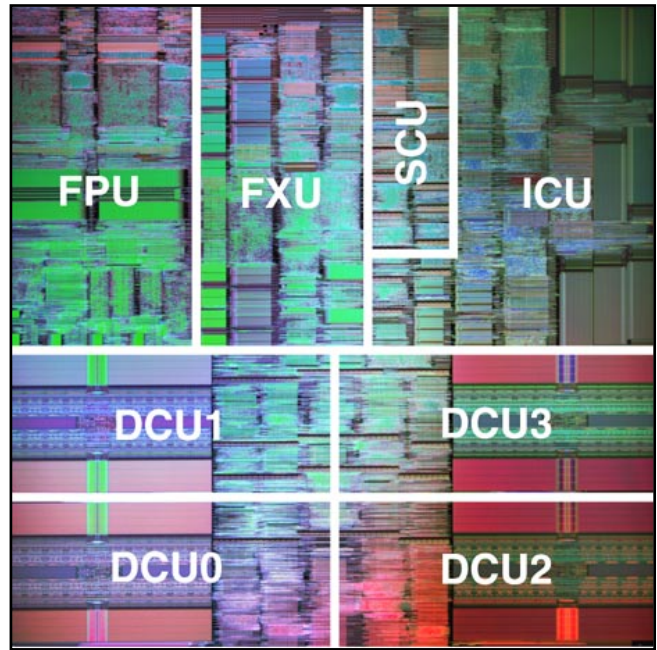


Figure 2. IBM's P2SC crams 15 million transistors on a die measuring 18.2 × 18.4 mm using a 0.29-micron five-layer-metal CMOS process. The chip includes the instruction cache unit (ICU), floating-point unit (FPU), integer unit (FXU), four data cache units (DCU), and the system control unit (SCU).

As the die photo shows, the actual cache SRAM arrays take up remarkably little space due to IBM's five metal layers and local interconnect. Most of the DCU (data cache unit) blocks are taken up by control circuitry, multiplexers, and sense amps. The dual FPUs take up about 15% of the P2SC, versus 17% for the PA-8000's dual FPUs. The PA-8000, however, is built in a 0.5-micron process, so the relative complexity of the P2SC's FPUs is clearly greater.

The previous champion for largest transistor count was the Alpha 21164, at 9.3 million. The P2SC contains 15 million transistors, of which 9.3 million are for the cache arrays. These arrays require slightly more transistors than one might expect at six transistors per cell because of the extensive redundancy. These redundant lines allow bad entries to be mapped out, improving the yield of the processor. With 5.7 million logic transistors, the P2SC is ahead of Pentium Pro, the PA-8000, and other complex microprocessors.

The package is also impressive, requiring 1,088 leads. The ceramic package, which measures 42.5 mm on a side, has an array of solder columns on the bottom. The attachment is similar to that of a BGA, but the columns provide more flexibility as the board and package expand. At 2.5 V, the P2SC has a maximum power dissipation of 30 W, about the same as other high-performance microprocessors.

The MDR Cost Model estimates the manufacturing cost of the P2SC to be a hefty \$375. The enormous die, costly package, and leading-edge IC process all drive up the cost. As the CMOS-6 process matures, the model shows the P2SC cost falling to about \$250. By contrast, the eight-chip Power2

costs an estimated \$500 to build, showing the advantages of integration. The PA-8000, on the other hand, costs about \$290 according to our model, due to its low-cost IC process and flip-chip packaging, while the compact 21164 has a build cost of just \$150, much less than the P2SC.

Optimized for Large Data Sets

Compared with other high-end microprocessors, the performance of the P2SC is lopsided, as Figure 3 shows. On integer code, the P2SC is a 135-MHz four-issue microprocessor with no register renaming or out-of-order capability. At 5.5 SPECint95 (base), it delivers no better performance than a 200-MHz dual-issue Pentium. The P2SC performance is estimated, and IBM believes it will improve slightly by the time of system shipments.

SPECint95, however, does not stress the memory subsystem. The P2SC has nearly twice the memory bandwidth of Sun's UltraSparc, which at 1.3 Gbytes/s held the previous record for a single-chip processor. Integer applications that can take advantage of this memory bandwidth will fare better than the relatively poor SPECint95 score would indicate. Such applications include transaction processing, financial simulations, and large database analysis ("data mining").

On floating-point code, the P2SC turns into a monster. It can perform two floating-point operations per cycle with minimal latency, plus two floating-point loads or stores as well as a branch and a condition-code instruction to handle loop processing. On the SPECfp95 suite, the P2SC outcores all shipping processors but the PA-8000, reaching an estimated 14.5. Digital's 500-MHz 21164, however, is also likely to surpass the P2SC and is due to ship this fall.

The full power of the P2SC is seen on applications that combine floating-point math with huge data sets, unlike the

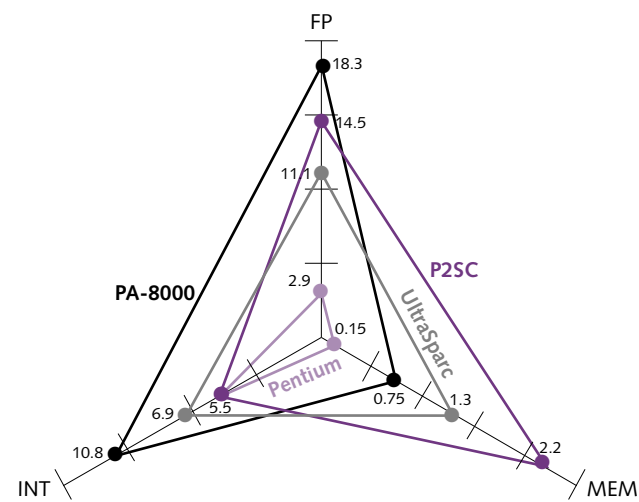


Figure 3. A comparison of the 135-MHz P2SC with the 200-MHz PA-8000, the 200-MHz UltraSparc, and the 200-MHz Pentium shows the IBM chip leads in memory bandwidth (Gbytes/s), does well on floating point (represented by SPECfp95_base), but fares poorly on integer code (SPECint95_base). (Source: vendors)

For More Information

The P2SC will not be sold as a standalone product. Systems using the P2SC will ship in 4Q96. For more information, contact your local IBM sales office.

SPECfp95 benchmarks. For these applications, which include electrical, mechanical, air flow, oil field, chemical, and meteorological simulations, caches are not useful, and high memory bandwidth is required. The P2SC should outrun all competitors for these types of programs.

P2SC Fills a Gap

The P2SC addresses a problem with the current lineup of PowerPC chips, all of which offer less than half the SPECfp95 performance of the P2SC. For those applications that require floating-point math, IBM must maintain its POWER line. In addition, the PowerPC 60x chips have poor memory bandwidth, no better than Pentium's. The PowerPC 620 will help this situation significantly, but even that processor has about half the bandwidth of the P2SC.

IBM will use the P2SC in its RS/6000 workstations to address high-end technical and scientific users. It may also be used in some transaction-processing systems. For maximum performance, the P2SC will appear in IBM's SP2 parallel-processing machine, which supports up to 512 processors and up to one terabyte (1,024G) of main memory.

IBM's plans include faster versions of the P2SC. The company believes there is some clock-speed headroom in the current design, and the chip can be easily ported to IBM's forthcoming 0.25-micron process for additional performance. IBM continues to work on the PowerPC 630, an internal design that is likely to be similar to the P2SC in system design but will include a new CPU core with a faster clock as well as more parallelism and out-of-order execution. The 630 is expected in systems in early 1998. After that, IBM may be able to shift over to the mainstream PowerPC line with Somerset's G4 (see 101103.PDF), which will hopefully offer adequate floating-point performance for IBM's needs.

Many processor designers (see 101004.PDF) are beginning to realize that memory bandwidth, not superscalar execution, is the chief performance bottleneck for large applications. Next-generation processors are likely to require 2 Gbytes/s of memory bandwidth to be competitive. IBM has reached this level well ahead of the pack, giving it an advantage over current competition on large applications.

The P2SC is a costly device, and much of the circuitry of the chip is wasted unless the application requires extensive FP math. On cache-bound integer programs, performance is relatively poor. But the P2SC is well designed for high-end scientific applications, and IBM's ability to deliver this product with a small design effort will make it a fruitful device, enabling the company to sell many expensive systems. □