Improved Delay and Current Models for Estimating Maximum Currents in CMOS VLSI Circuits

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Abstract *Excessive voltage drops in power and ground (P&G) buses of CMOS VLSI circuits can severely degrade both design reliability and performance. Maximum current estimates are needed in the circuit to accurately determine the impact of these problems. In [1], a pattern-independent, linear time algorithm (*`iMax`*) is described that is very effective in estimating the maximum current waveforms at various contact points in the circuit. In [1], the algorithm was demonstrated for simple gate delay and current models. In this paper, we first derive expressions for modeling delays and current waveforms for a general gate and then describe how the algorithm can be extended under more general models.*

1 Introduction

In the design and analysis of high performance VLSI circuits, reliability considerations are extremely important and should be considered early in the design phase. Excessive currents in power and ground (P&G) buses of CMOS circuits affect both circuit reliability and performance by causing excessive voltage drops. Voltage drops in P&G buses slow down the speed of operation of the circuit besides leading to logic errors in some cases (see [2]). Severity of the voltage drop problems worsen as the density of integration on chip increases and the supply voltage is scaled down. In order to study the impact of these problems, estimates on *maximum currents* that are drawn from the P&G buses by a circuit are needed.

The current drawn by a CMOS circuit is a complex function of input excitations. For each input pattern applied to the circuit, a transient current waveform is drawn from the P&G buses. In the presense of such input dependent waveforms, we define the maximum current at a contact point as the maximum envelope of various transient current waveforms that result by the application of all possible input patterns to the circuit [1]. This maximum current is called the *maximum envelope current* waveform, or simply `MEC` waveform.

Accurate estimation of the `MEC` waveforms at all the contact points in a circuit is an NP-complete problem [2]. In [1], we have proposed a pattern-independent `iMax` algorithm that estimates upper bounds on the `MEC` waveforms. The algorithm, being linear in time as well as memory space requirements, is extremely efficient, as has been demonstrated by extensive experimental results. In the algorithm, the delay of each gate is assumed to be a fixed, user-specified number. Furthermore, for every transition at the output of a gate, the current waveform drawn from the power or ground bus, called the *transition current waveform*, is represented by a right angle triangle. Such a model, however, is overly simplistic and does not effectively model the dependence of delay and transition current waveform on several factors, such as, specific input excitations, slew rates of inputs, the output capacitance and various transistor parameters. The contribution of this paper is firstly, to present analytical expressions for the delay and transition current waveform of a general static CMOS gate and secondly, to demonstrate how the `iMax` algorithm can be extended under such general models.

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2 Delay and Current Models

In this section, we derive analytical expressions that can be used to approximate the delay and current waveform for a static CMOS gate. These expressions are fairly easy to evaluate and provide acceptable agreement with SPICE in terms of accuracy. In CMOS, whenever a gate switches, it can be reduced to an equivalent inverter. Therefore, we begin our modeling by presenting expressions for an inverter. The case of a general gate is discussed later.

2.1 Models for an inverter

For an inverter driven by a step input, it is straightforward to derive expressions for its delay [3]. The *high* to *low* (*hl*) and *low* to *high* (*lh*) delays, denoted as t^s_{dHL} and t^s_{dLH} respectively, are given by:

$$t^s_{dHL} = \frac{C_L}{k_N} A_N, \quad t^s_{dLH} = \frac{C_L}{k_P} A_P \tag{1}$$

where k_N and k_P are the N- and P- channel transistor transconductances and A_N and A_P are two (process dependent) constants. The transition current waveform of the inverter is an exponentially decaying waveform. In order to simplify the modeling, we approximate it by a right angle triangle. The peak value of this current, for an *hl* transition at the gate output, is given by the saturation current of the N-channel transistor when its gate voltage is V_{DD}, i.e. (also see Eq. (1)),

$$I^s_{peak} = k_N \frac{(V_{DD} - V_T)^2}{2} = \frac{C_L A_N}{t^s_{dHL}} \frac{(V_{DD} - V_T)^2}{2} \tag{2}$$

A similar expression exists for the *lh* current. Thus, knowing the output capacitance (C_L) and the step delay of an inverter, the peak values of its transition current waveforms can be calculated. The duration of this

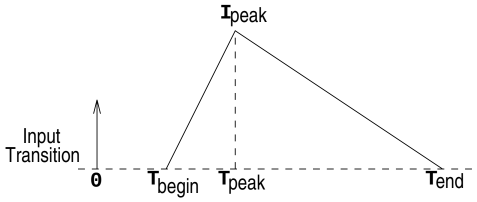


Figure 1: Transition current waveform: non-step input.

waveform can be calculated from charge conservation, i.e., $C_L V_{DD} = \frac{1}{2} I^s_{peak} \times Duration$.

In real circuit applications, however, a gate is usually driven by another gate and therefore, instead of step inputs, *characteristic waveforms* are present at its inputs. Characteristic waveform is the definite voltage waveform towards which the waveform converges in a series of identical inverters [4]. We now discuss how the delays and current waveforms of an inverter change when characteristic waveforms are present at its input, i.e. the inverter is fed by another input. For delay, we have adopted the results proposed by Hedenstierna and Jeppson (H&J) [4]. The expressions for the current waveform is a contribution of this paper. A similar derivation of current waveform expressions in the context of probabilistic simulation has been proposed in [5].

H&J use the step delays (t^s_{dHL}, t^s_{dLH}) of an inverter to characterize its output rise/fall slew rates. Under this model, the *hl* and *lh* delays of an inverter, denoted t_{dHL} and t_{dLH}, are given by the following expressions [4] :

$$t_{dHL} \;=\; t^s_{dHL} \;+\; B\frac{B_N}{A_P} t^s_{dLH,in} \qquad (3)$$

$$t_{dLH} \;=\; t^s_{dLH} \;+\; B\frac{B_P}{A_N} t^s_{dHL,in} \qquad (4)$$

where B_P and B_N are two (process dependent) constants and B is another constant whose value is empirically determined so as to provide best fit with the SPICE simulations. Parameters $t^s_{dHL,in}$ and $t^s_{dLH,in}$ are the step delays of the inverter on the input side.

For the calculation of the transition currents, we again assume that they can be approximated by triangular waveforms, as shown in Fig. 1. For this figure, we have assumed that the 50% point of the input voltage waveform occurs at time zero and we need to calculate T_{begin}, T_{peak}, T_{end} and I_{peak}. For simplicity of notation, we denote the *hl* (*lh*) step delay of the inverter by t^s_d and the *lh* (*hl*) step delay of the inverter on the input side by $t^s_{d,in}$. Various parameters of the *hl* (*lh*) transition current waveform can then be calculated from the following expressions. The details on the derivation of these equations are given in [2].

$$T_{begin} \;=\; a_1\, t^s_{d,in}, \quad I_{peak} \;=\; I^s_{peak}\left(1 - a_2 \frac{t^s_{d,in}}{t^s_d}\right) \qquad (5)$$

$$T_{end} \;=\; T_{begin} \;+\; \frac{2 C_L V_{DD}}{I_{peak}} \qquad (6)$$

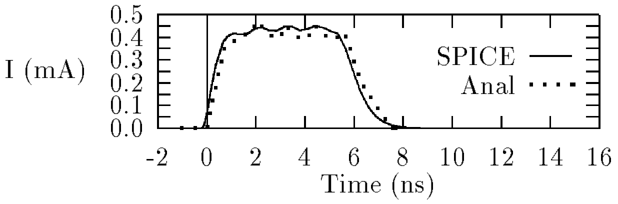


Figure 2: Comparing analytical expressions with SPICE for a chain of inverters.

$$T_{peak} \;=\; T_{begin} \;+\; \frac{t^s_{d,in}}{(t^s_{d,in} + a_3\, t^s_d)}(T_{end} - T_{begin}) \qquad (7)$$

where a_1, a_2 and a_3 are three constants and I^s_{peak} is the peak value of the current waveform for a step input, as given by Eq. (2). The delay and current waveforms calculated from these equations provide an acceptable match with the ones observed from the SPICE simulations, as shown in Fig. 2. In this figure, we have plotted the two waveforms for a chain of five inverters. Each waveform is the sum of the current waveforms of individual inverters.

2.2 Models for general gates

We now discuss how the delays and current waveforms for a general static CMOS gate are calculated. A general gate differs from an inverter in that depending upon which input(s) is excited, its delay and current waveform change significantly. As will become clear in the next section, in pattern-independent analysis, since we simulate the circuit for all possible input patterns in one sweep, it is very expensive to maintain information at each gate about the specific inputs that lead to a transition at its output. Rather, one maintains information about a set of inputs that could *possibly* lead to a transition at the output. Thus, for each transition at the output, a range of input and gate step delay values are possible. We capture this behavior of the gate by maintaining delay intervals and by accounting for all possible transition current waveforms, as explained below. This kind of worst case analysis, however, gives rise to somewhat loose estimates on voltage drops and therefore, we also support simpler models. In particular, in this work, delay values and transition current waveforms are represented at three levels of detail, as explained below:

2.2.1 Model one (m1)

In the first and the simplest model, delay and transition current of each gate are represented by one number and one triangular waveform, respectively. These represent the typical delay and typical transition current waveform of the gate under most operating conditions. They are calculated as follows.

To each gate, a typical *step* delay value is assigned. Such a value is either obtained from the gate level library supplied by the manufacturer, or is calculated from the SPICE simulations beforehand. The actual delay of the gate in its real operation is calculated by appropriately modifying its step delay value by the typical step delay value of gates feeding it (Eqs. (3) or (4)). Once all the gates in the circuit have been assigned their step delay values, the step delay values on all the input lines to every gate are known. Input step delay for each gate is calculated by simply averaging the step delay values on all of its input lines. Similarly, from the gate step delay and the input step delay values, the transition current waveform of the gate is calculated from Eqs. (2), (5)-(7).

2.2.2 Model two (m2)

The *lh* and *hl* delay values for some gates in a circuit could be significantly different, and it is difficult to approximate them by the same number. In the second model, for each gate, the *lh* and *hl* delays (t_{dHL} and t_{dLH}) and the corresponding transition current waveforms are represented separately. They are calculated in a similar fashion as above.

2.2.3 Model three (mI)

In the third and the most general model, the delay of each gate is specified by two intervals, one interval for the *hl* delay and another for the *lh* delay. Each interval begins at the corresponding minimum delay value and ends at the corresponding maximum delay value for the gate. Similarly, the transition current for each type of transition at the gate output is specified by the worst case current waveform, which is an *envelope* of all current waveforms that could exist for any of the input and gate step delay values. The delay intervals and worst case current waveforms are calculated as follows.

For each of *hl* and *lh* transitions at every gate, its minimum and maximum *step* delay values are specified by the user. Thus, the user specifies $t^{s,min}_{dHL}$, $t^{s,max}_{dHL}$, $t^{s,min}_{dLH}$ and $t^{s,max}_{dLH}$. The minimum and maximum input step delay values for a gate are calculated by finding the minimum and maximum of the corresponding step delay values on all of its input lines. Thus, we know $t^{s,min}_{dHL,in}$, $t^{s,max}_{dHL,in}$, $t^{s,min}_{dLH,in}$ and $t^{s,max}_{dLH,in}$. The actual minimum and maximum delay values for the gate are determined from the following equations (see Eqs. 3 and 4).

$$t^{min/max}_{dHL} = t^{s,min/max}_{dHL} + B\frac{B_N}{A_P}t^{s,min/max}_{dLH,in} \quad (8)$$

$$t^{min/max}_{dLH} = t^{s,min/max}_{dLH} + B\frac{B_P}{A_N}t^{s,min/max}_{dHL,in} \quad (9)$$

The transition currents for the gates are calculated as follows. We will only explain the process for the *lh* current. The *hl* current waveform is calculated likewise. From Eqs. (2), (5)-(7), two triangular current waveforms are calculated. The first waveform is calculated by treating $t^{s,min}_{dLH}$ as the gate step delay and $t^{s,min}_{dHL,in}$ as the input step delay. The second waveform is calculated by treating $t^{s,max}_{dLH}$ as the gate step delay and $t^{s,max}_{dHL,in}$ as the input step delay. We call these waveforms W_{max} and W_{min}. The convex hull of W_{min} and W_{max}, as shown in Fig. 3, is taken as the worst case *lh* transition current waveform. It can be argued that under most typical operating conditions, the duration of W_{min} and the height of W_{max} are the largest such numbers possible. Thus for any gate and input step delay pair, the corresponding waveform will be 'almost' completely contained within the envelope, see [2].

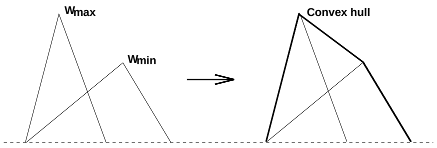


Figure 3: Transition current calculation for model mI.

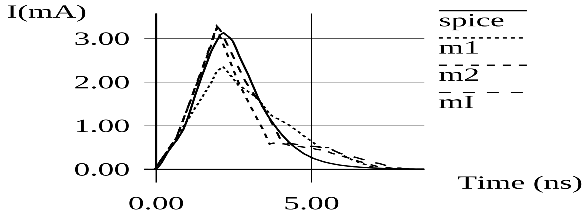


Figure 4: Comparing the three models for BCD-to-Decimal decoder circuit.

2.2.4 Example

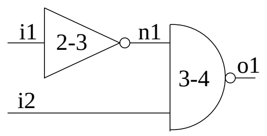
We now compare the three gate delay and current models for a BCD-to-Decimal decoder circuit. The current waveforms obtained from the SPICE simulations and from models m1, m2 and mI when a specific input pattern is applied to the circuit, are shown in Fig. 4. From this figure, it is seen that the current waveforms from models m1 and m2 closely follow the waveform obtained from SPICE. As expected, the SPICE waveform is 'almost' completely contained within the waveform from model mI. Similar results have been obtained for other circuits.

3 Main Ideas of the iMax Algorithm

In this section, we briefly summarize how the `iMax` algorithm can be extended under the more general gate delay and transition current models. For details on `iMax`, the reader is referred to [1, 2].

The `iMax` algorithm begins with the gate level description of the combinational circuit under consideration. Unless specified otherwise, the algorithm assumes that nothing is known about the specific excitations at the primary inputs except that they may transition at time zero. This ambiguity about signal specification is called an *uncertainty*. Here is an example to explain the algorithm in detail.

Information about specific excitations at internal circuit nodes is stored in the form of time intervals [1]. For the circuit in Fig. 5, in the worst case, each of the primary inputs could switch *lh* or *hl* at time zero or stay at *low* (*l*) or *high* (*h*) for all time. Given this at the input of the inverter and if its delay interval for both *lh* and *hl* transitions is [2, 3], then its output could switch *lh* or *hl* anytime during [2, 3], or stay at *low* or *high* for all time. Similarly, if the delay interval for both *lh* and *hl* transitions for the NAND gate is [3, 4], then its output could switch *lh* or *hl* anytime during the time interval [3, 4] due to the primary input *i*2, or could switch anytime during [5, 7] due to the output of the inverter; or could stay at *low* or *high* for all time. In this fashion, `iMax` computes the set of all possible transitions and their associated timing information at the output of every logic gate. The contribution of each gate to the maximum current waveforms is calculated



Input Description : i1, i2 $\in \{l, h, hl, lh\}$ at time 0.
Uncertainty Intervals :
i1, i2: $lh[0, 0]$, $hl[0, 0]$, $l[0, \infty)$, $h[0, \infty)$
n1: $lh[2, 3]$, $hl[2, 3]$, $l[0, \infty)$, $h[0, \infty)$
o1: $lh[3, 4][5, 7]$, $hl[3, 4][5, 7]$, $l[0, \infty)$, $h[0, \infty)$
Key : Excitation[Interval Begin, Interval End]

Figure 5: An example illustrating the `iMax` algorithm.

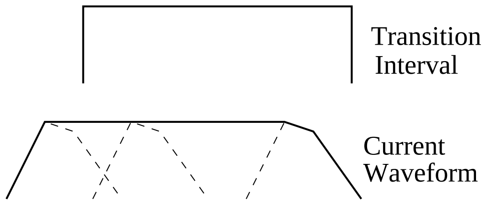


Figure 6: Calculation of current waveform due to a transition interval.

from this set of all possible transitions as explained below.

In Fig. 6, we consider an interval during which a gate could possibly switch and show how its corresponding worst case current waveform is calculated. Since the gate can switch at any time during the interval, therefore, a piece-wise linear current (the transition current) waveform could be drawn at any time during the interval, as shown in Fig. 6. Thus, by taking an upper bound envelope of all such waveforms, we obtain the worst case current waveform due to the transition interval. By repeating the process for every transition interval, we obtain the worst case current contribution of the gate. Contact point current waveforms are computed by combining the current waveforms of the gates that are tied to it. It can be proved that the current waveform obtained from this process at a contact point is a point-wise upper bound on the corresponding MEC waveform (see [2]). Further, using these current waveforms, the maximum voltage drop estimated in the bus is an upper bound on the worst case voltage drop [2]. Worst case voltage drop is the maximum voltage drop that occurs in the bus over all possible input patterns.

4 Experimental Results

In Fig 7, the results of running the `iMax` algorithm for a 2-input, 4-gate EX-OR circuit are shown. For this circuit, all the gates are tied to a single contact point and in the figure, the maximum current waveforms at the contact point are shown. The solid curve (`MEC`) is the maximum envelope of all the 16 current waveforms obtained from SPICE simulations by trying out all possible input patterns. The other three curves are obtained from `iMax` when models m1, m2 and mI are used. In Fig 8, we show a similar plot for a 4-input, 48 gate BCD-to-Decimal decoder circuit. These two figures indicate that the `iMax` algorithm is very effective in calculating the maximum current waveforms and thereby maximum voltage drops in power and ground

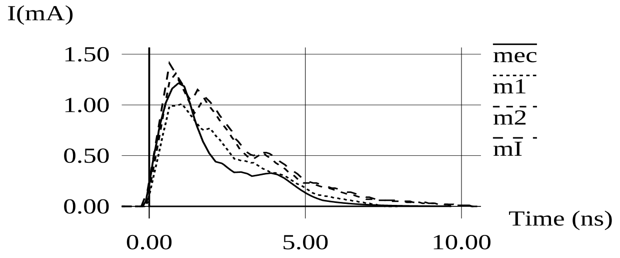


Figure 7: `MEC` and `iMax` currents for an EX-OR circuit.

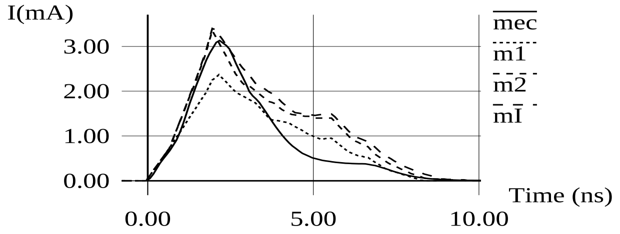


Figure 8: `MEC` and `iMax` waveforms for BCD-to-Decimal decoder circuit.

buses of CMOS circuits. We have experimented with circuits of upto 27,000 gates and the results of these simulations can be found in [2].

5 Conclusions

In this paper, we have presented analytical expressions for calculating the delay values and transition current waveforms of an inverter. We have also shown how these models for an inverter can be used to calculate the delay values and transition current waveforms for a general static CMOS gate. Finally, we have described how the pattern-independent, linear time `iMax` algorithm, for the calculation of maximum voltage drops in power and ground buses of CMOS VLSI circuits, can be extended under such models. The effectiveness of the algorithms has been demonstrated with the help of experimental results. For an extensive analysis of the approach, the reader is referred to [2].

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