Worst Case Voltage Drops in Power and Ground Buses of CMOS VLSI Circuits

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Abstract: *This paper summarizes the main developments of our on going study at University of Illinois on the maximum voltage drop estimation in power and ground buses of CMOS VLSI circuits. Voltage drops occurring in the supply lines depend upon the specific input patterns applied to the circuit and it is prohibitively expensive to enumerate all possible input patterns. Our proposed solution methodology consists of two parts. In the first part, maximum current waveforms at every contact point in the circuit are estimated by the linear time, pattern independent algorithm, called* `iMax`. *The algorithm is extremely efficient in time as well as space, and produces good results for most circuits. The accuracy of the results obtained from the* `iMax` *algorithm can be further improved by resolving the signal correlations that exist inside a circuit. In the second part of the voltage drop estimation process, we iteratively resolve these correlations by a novel partial input enumeration* (`PIE`) *technique and thus improve the bounds on the maximum voltage drop. We establish with extensive experimental results that these algorithms are extremely efficient and are applicable to VLSI circuits.*

1 Introduction

Excessive voltage drops in the power and ground (P&G) lines of CMOS VLSI circuits affect both circuit reliability and performance by causing erroneous logic signals and degrading the switching speed. Furthermore, these voltage drop problems become worse as the minimum feature size on chips shrinks and the supply voltages are lowered. Therefore, in order to avoid design changes in its final stages [1, pp. 490-492], excessive voltage drop problems should be detected and corrected early in the design cycle.

Voltage drop problems in the P&G buses arise due to the finite resistance, capacitance and inductance of the lines. The inductive drops ($L\frac{di}{dt}$) could be significant when a large number of circuit components switch simultaneously. This usually happens when the clock trigger causes several flip flops to change states simultaneously. Various gates in the circuit seldom switch simultaneously and therefore the inductive drops arising due to them can be neglected. In this research, we assume that the transition times at various flip flops are appropriately staggered such that the inductive drops arising due to them are taken care of. Therefore, we focus on the estimation of maximum voltage drops arising due to the finite resistance and capacitance of the lines.

An exhaustive way of estimating maximum voltage drops is to repeat the following procedure for every input pattern applied to the circuit. Estimate the current waveforms at the contact points by simulating the circuit and then report the maximum voltage drop occurring at any node in the bus by analyzing its equivalent R/RC network, as shown in Fig. 1. However, because of the combinatorial nature of this problem, heuristic solution methods which speed up the estimation process at a slight loss in accuracy are necessary.

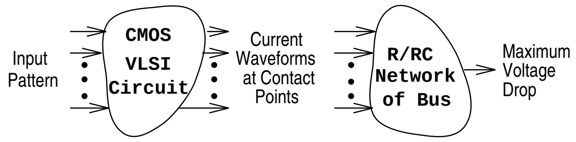

Figure 1. Estimating Maximum Voltage Drops.

We propose to divide the estimation process into the following two parts. In the first part, we estimate *maximum currents* (over all possible input patterns) at every contact point in the circuit. In the second part, using these maximum currents, we estimate the maximum voltage drops in the buses. The effectiveness of this process depends upon how the maximum currents are modeled at various contact points and how efficiently they are estimated. Secondly, some of these maximum currents might be correlated, i.e., they may not correspond to a single input pattern, and this may result in an overestimation of the maximum voltage drop. In this research, we have tried to address some of these problems. In particular, we have proposed an effective measure for representing maximum currents at the contact points. We have also developed an efficient, pattern independent algorithm, called `iMax`, for estimating upper bounds on the maximum currents [2] at every contact point in the circuit. The `iMax` approach is linear in time as well as space.

In order to maintain reasonable execution times, the `iMax` approach neglects various signal correlations that exist inside a circuit. While in most cases, `iMax` produces good results, in some cases, the loss due to signal correlations can be significant. We have also developed a new *partial input enumeration* (`PIE`) algorithm that efficiently resolves some of these correlations and leads to significant improvements in results [3].

This paper is organized as follows. In the next section, we discuss the class of circuits that this work is focused on. After that, we describe the proposed maximum current estimate that we have used in this research. In section 4, we briefly describe how this problem was addressed by researchers in the past. In section 5, we present the main ideas of the linear time `iMax`

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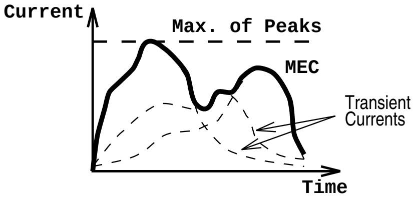

Figure 2. The Maximum Current Estimate.

algorithm. The details of this algorithm can be found in [2, 4]. In section 6, we briefly discuss the signal correlation problem and discuss the salient features of the partial input enumeration algorithm that efficiently resolves these correlations and further improves the results obtained from the `iMax` algorithm. Finally, in section 7, some concluding remarks are provided.

2 Circuit Assumption

In this research, we focus on a specific but very common design style, namely edge-triggered, latch-controlled synchronous digital circuits. These circuits consist of combinational blocks separated by latches such that inputs to each block switch simultaneously. As a result, we focus on the analysis of a single combinational block all of whose inputs switch simultaneously.

Given the specific clocking scheme of the synchronous circuit, the maximum currents from different combinational blocks can be appropriately shifted in time depending upon the individual clock trigger, and used to find the maximum voltage drops in the buses.

3 Maximum Currents

The current drawn by a CMOS circuit is a complex function of input excitations. For each input pattern applied to the circuit, different transient current waveforms are drawn at the contact points. At a specific contact point, different current waveforms result from the application of different input patterns. Instead of representing maximum current at a contact point by a single dc value (the maximum of the peaks), as proposed by [5], we represent it by a waveform whose value at any time is the maximum current value that the circuit can draw at that time, as shown in Fig. 2. We call it the *maximum envelope current* (`MEC`) waveform. As Table 1 shows, the (normalized) maximum voltage drop results obtained by estimating the `MEC` waveforms at the contact points are significantly better than the results when just the maximum of peaks is estimated. For this table, close bounds to the respective maximum currents were estimated, as the exact maximum estimation problem is NP-complete.

Table 1. Max. Vol. Drops

Circuit	Peak	MEC
c432	2.20	1.79
c499	4.54	3.24
c880	4.11	2.22
c1355	6.11	4.86
c1908	8.48	3.22
c2670	8.79	3.97
c3540	11.64	5.26
c5315	13.85	6.22
c6288	12.65	10.07
c7552	20.80	12.93

4 Previous Work

Chowdhury et. al. have addressed the problem of maximum current estimation in [5]. Devadas et. al. have addressed a similar problem of maximum power dissipation estimation in [6]. Both of these works solve the respective NP-complete maximum estimation problems by either an exact search technique i.e., a branch and bound algorithm or some heuristic technique. Both of these techniques are based on searching for a specific input pattern that leads to the desired maximum. However, the number of possible input patterns for a circuit is exponential in the number of inputs. Their solution methods are very slow for large circuits, as shown by their experimental results. In contrast, we have developed a linear time algorithm that avoids search by adopting a pattern independent approach.

5 Main Ideas of the `iMax` Algorithm

The `iMax` algorithm operates at the gate level description of the circuit. Unless specified by the user, the algorithm assumes that nothing is known about the specific excitations at the primary inputs, except that they may transition at time zero. We call this an *uncertainty* about these input signals. The basic idea of the proposed algorithm is to propagate the uncertainty present at the primary inputs, inside the circuit so that at the output of every logic gate, we know the set of all possible excitations and their associated timing information. From this information, the worst case current waveforms are calculated by accounting for the current arising due to every possible transition at every gate. The details of this approach can be found in [2, 4].

At every contact point, `iMax` outputs a current waveform that is a point-wise upper bound over the corresponding `MEC` waveform. As a result, the maximum voltage drop calculated in the bus when using the current waveforms obtained from the `iMax` algorithm, is an upper bound on the maximum voltage drop calculated for any input pattern applied to the circuit.

In order to access the quality of the solution obtained from the `iMax` algorithm, we need to know the *actual* maximum voltage drop that occurs at some node in the bus over all possible input patterns. However, since such an exhaustive enumeration is practically impossible for most circuits, we have estimated a lower bound for the maximum voltage drop by enumerating a small subset (about 100,000) of input patterns. We have used simulated annealing (`SA`) algorithm for the selection of different input patterns during the above enumeration process. In Table 2, we report the respective upper bound and the lower bound on voltage drop obtained from the `iMax` and `SA` algorithms for the ISCAS-85 benchmark circuits, along with the CPU times taken by them on a sun SPARC station ELC. The linear time `iMax` algorithm takes only a few seconds of CPU time compared to several hours of time needed by the `SA` algorithm for trying 10,000 input patterns. Secondly, the ratio reported in the table are only an upper bound on the true error. Clearly, for most circuits, the results obtained from `iMax` are quite acceptable.

Table 2. iMax Results for ISCAS-85 Circuits					
	Max. Vol. Drops			CPU Times	
Circuit	iMax	SA	Ratio	iMax	SA (10k)
c432	1.79	1.10	1.63	1.2s	13m 11s
c499	3.24	1.79	1.81	4.6s	30m 10s
c880	2.22	1.29	1.72	4.4s	31m 37s
c1355	4.86	3.34	1.46	7.0s	34m 25s
c1908	3.22	2.49	1.29	10.0s	1h 28m
c2670	3.97	3.13	1.27	12.1s	2h 30m
c3540	5.26	2.01	2.62	19.3s	4h 15m
c5315	6.22	3.51	1.77	24.9s	6h 42m
c6288	10.07	7.24	1.39	35.3s	26h 40m
c7552	12.93	6.51	1.99	40.5s	14h 5m

Table 3. Results of PIE			
Circuit	PIE (100)	PIE (1k)	Time (100)
c432	1.62	1.62	3m 57s
c499	1.80	1.78	7m 44s
c880	1.72	1.67	8m 6s
c1355	1.46	1.46	14m 26s
c1908	1.24	1.23	22m 32s
c2670	1.27	1.27	23m 15s
c3540	2.01	1.88	31m 30s
c5315	1.77	1.76	48m 38s
c6288	1.39	1.39	1h 30m
c7552	1.88	1.86	1h 20m

6 Partial Input Enumeration

In general, signals at various nodes of a circuit are mutually correlated and this limits the number of transitions that can occur at the outputs of various gates. In this study, we have identified two types of signal correlations, namely *spatial* correlations, which are the correlations present among various nodes of the circuit and *temporal* correlations, which reflect how the signal values at any node at any time are correlated with its values at previous times. The **iMax** approach completely ignores both spatial and temporal correlations and therefore, overestimates the supply currents. The advantage of ignoring correlations in the algorithm is its desirable, linear time performance.

The bound produced by the **iMax** algorithm can be improved by enumeration. Further, few nodes in the circuit contribute more to signal correlations than others. Based on these observations, we have developed a partial input enumeration algorithm that intelligently selects a few critical inputs and enumerates a limited number of cases at them. The algorithm follows a *best first search* strategy [7] and leads to an *iterative improvement* in the maximum voltage drop results. Secondly, significant amount of improvement occurs in the first few iterations of the algorithm. Because of these properties, the algorithm produces excellent results for large circuits in reasonable amounts of CPU time. The results of running the *PIE* algorithm on the ISCAS-85 circuits are documented in Table 3. In this table, under various PIE columns, we report the ratio of the respective upper bound to the lower bound. The PIE results were obtained after running the algorithm for 100 and 1000 iterations. CPU times taken by the algorithm for the 100 iterations case are shown in the last column. From the table, we observe that for cases where the **iMax** algorithm does not produce good results, the PIE algorithm produces good results in reasonable amounts of CPU time. Similar results are obtained for much larger ISCAS-89 circuits and are documented in [3, 4].

7 Summary

In this paper, we have summarized the main results of our on-going study on the worst-case voltage drop estimation in power and ground lines of CMOS VLSI circuits. We have proposed to divide the maximum voltage drop estimation process into two parts. In the first part, the maximum current waveforms, and thereby maximum voltage drops, are estimated by the linear time, pattern independent **iMax** algorithm. In the second part, the upper bound obtained from the **iMax** approach is iteratively refined by the novel partial input enumeration approach. These algorithms are applicable to large circuits as is established by experimental results on circuits with up to 22,000 gates.

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