A Design Methodology for Power Electronics*

Luis E. Amaya, Philip T. Krein, Farid N. Najm
Coordinated Science Laboratory,
University of Illinois at Urbana-Champaign

1308 West Main Street
Urbana, IL 61801
Tel.: (217) 244-6395, Fax.: (217) 244-1946
e-mail: amaya@uivlsi.csl.uiuc.edu

September 30, 1996

Abstract

Currently there are no computer-aided-design (CAD) tools dedicated to the design and synthesis of power electronic circuits. The design process has not been formalized, and most of the effort in computer aid has been oriented towards simulation, neglecting other stages of the design process that can also benefit from the use of computer tools. This paper present an outline of the structure of an automated power electronics design CAD tool. The different parts of this tool are described along with the problems that make them difficult or interesting. Current progress in the development of some of those part is also presented.

1 Introduction

The circuit synthesis problem represents the entire sequence of design operations starting from a set of specifications and desired functions and leading to a complete unit. This ultimate objective of a CAD system is served to a large degree for digital applications and, more recently, in some analog design contexts. In power electronics the available CAD tools tend to address circuit analysis rather than the synthesis problem. Although improvements continue in computer tools for circuit design the process for power electronics is still difficult without extensive bench testing. In this paper a description is given of a design and synthesis methodology intended for power electronics applications. Based on recent progress, it is expected that most major steps of such methodology will become implemented as parts of a CAD tool within the next few years.

*This Reasearch was supported by the Semiconductor Reasearch Corporation under Contract SRC-DP-109

2 A Design Methodology

Several steps can be identified in the process of design and synthesis of a power electronic converter. The most general steps are *converter selection*, *component specification*, *parasitic estimation*, *simulation*, and *optimization*. Although these steps can be identified separately, they interact with each other as shown in figure 1.

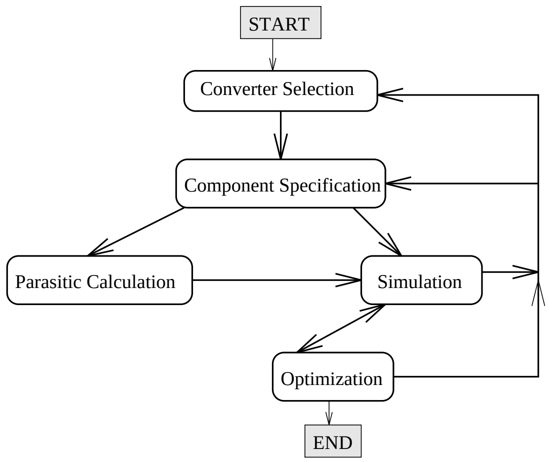

Figure 1: The design process for a power electronic converter.

The same steps can be applied to design in other areas such as analog electronics. The differences between the design process in power electronics and analog electronics are in how difficult each task is and in how much effort has been dedicated to solving each of them; in any case, there are no automated tools to help a designer along the complete design process.

In analog electronics the most difficult tasks are the selection of a configuration and the selection of specific components; these tasks are not performed automatically and there is no method to be implemented in a computer tool. In power electronics these two tasks are relatively simple, and could be automated. It has not been done because they would only be really useful as part of a complete design environment.

Considerbale effort has been directed toward the simulation task, both in analog electronics and in power electronics. The results are satisfactory for analog electronics, but there is still a long way to go in power electronics in bypassing the problems caused by very stiff systems and the lack of good parasitic extraction and modeling methods, especially magnetics. Simulation could be regarded as an easy task in analog electronics compared to power electronics.

Design optimization can be done in analog electronics by means of simulation varying the values of some parameters in the circuit. In principle this could be done in power electronics, but the long simulations and the lack of good models for some of the parasitic effects prevents obtainig appropriate results.

The purpose of a synthesis tool is to guide the designer in each of the main steps of the design process in order to help improve design quality and reduce design time. Therefore, the description given above for the design process should also match the top level description of a good design and synthesis tool. Since the final design of a converter can not always be generated automatically by a computer, a synthesis tool should always allow the user to make the final decision in any aspect of the converter. A valid user option can be to let the tool decide.

2.1 Converter selection.

The first step in designing a power converter, or any electronic circuit, is to decide which circuit configuration is going to be used. A method for selecting an appropriate configuration is a procedure that takes as input a general description of the desired converter, i.e., the answers to the following questions: what type of conversion is needed, what are the relations between input and output voltage and current ratings, is isolation required, is a common reference allowed or required for the input and the output? and produces as output a topological description of a circuit that can perform the required conversion, if properly operated.

It is usually the case that more than one circuit can perform the required conversion, each one having certain advantages and disadvantages compared to the others. Selecting from those final circuits is sometimes a subjective process; therefore, a computer selection method should provide the designer with a menu of different circuits that meet the requirements, leaving to the user the final decision of which specific circuit to use.

The list of configurations to be shown to the user can be generated in three different ways. The first approach is the hard-coded method, where all the necesary information is stored inside the selection system. The user-menu will show a list of the most common converter topologies; then, the user decides which topology to use and the system can take the specified circuit and proceed to the next steps in the design process. In this case, the user-menu includes converters that may not be appropriate for the specific requirements, and it is really the user who performs the selection process.

A second method makes use of a database where all possible topologies are stored. The selection system takes the user requirements as search indices to find the topologies that would be able to perform the required power conversion. The user-menu will show only the configurations selected from the database, as opposed to the hard-coded method, where all configurations are shown.

Before hard-coding the configurations or storing them in a database, they must be generated either by a human designer or by a computer. If only the most popular converters are to be considered, the configurations can be created by a designer. If the selection process is designed to allow new circuit configurations to be considered very often, a computer generated set of circuits can be used. The third generation method is implemented by a circuit builder, which builds a set of circuits based on the user-specified input. Instead of storing old circuits for reuse, they are generated every time they are needed. This approach is viable only if the generation process is not very time consuming compared to a database search. This is the approach we take, keeping the database method as a very good alternative. Some work can be found in the literature in the area of automated synthesis of DC-DC power converters–see [1], [2], [3], and others. The method we use differs basically in the way we view the building process. At each stage we have a converter that can perform some function and we try to enhance it (by adding circuit elements) to produce a different functionality. In previous works, the approach tends to be just an exhaustive analysis of the possible interconnections of switches, inductors and capacitors. The results, at any rate, will be similar, although our process may be more intuitive for a designer.

A basic power converter can be seen as two power sources, one at the input and one at the output, interconnected by a matrix of switches that operate in a certain time pattern [4], as shown in figure 2. Complex converters can be built by cascading two or more of these basic stages.

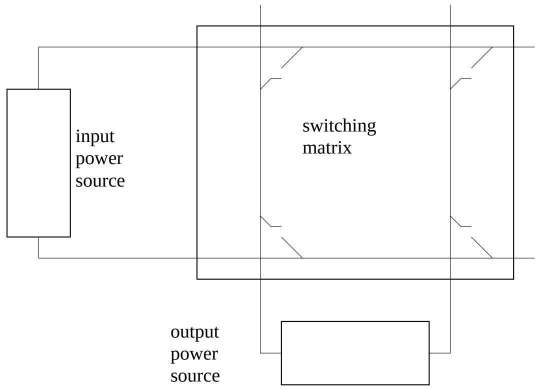

Figure 2: Basic representation of a power converter.

A quick look to Kirchoff's rules shows that in the basic one-stage converter, one of the power sources must be a voltage source and the other one a current source. The building process starts by placing a voltage source at the input and finding the different switch configurations that are acceptable for conecting the input source to the output current source. In the DC-DC case, the obvious results are the buck converter and some variations that may have redundant switches and/or common positive node instead of common ground. Then a new stage is added, which will be terminated by a voltage source; the results are the buck-boost and some variations with redundant switches and/or positive common connection. This process will repeat up to a predefined maximum number of stages. Then, the process is initiated again with a current-fed converter.

The whole process seems a bit complicated for generating the very well known DC-DC topologies, but this same process with some different restrictions is capable of finding configurations for DC-AC, AC-AC, and AC-DC converters. In addition to the circuit topologies, the process determines what the switch operation sequence is. It can also determine the type of switch required, i.e., uni- or bi-directional blocking, uni- or bi-directional conduction.

2.2 Component specification.

The next step after determining the circuit configuration to be used, is to determine the values of the different components, i.e, inductors, capacitors, switch sizes, and operation duty cycle. This step does not depend in any way on the type of procedure used for finding the configuration.

The precise specification of component sizes is the result of the optimization process, but some initial conditions must be given to the optimizer. An appropriate set of values is built with the critical inductances and capacitances, the minimum sizes for the switches, and the duty cycle of the switches. This section shows a procedural method for finding this set of values. At the present, we only have results for the DC-DC case, but we plan to extend the procedure to the other type of converters.

Inductor and capacitor critical values are functions of the operating frequency, which is assumed to be known, the duty cycle, which, as said before, is unknown, and the DC currents and voltages in the transfer sources, which are also unknown. A variation of the modified nodal analysis (MNA) formulation combined with averaging techniques will be used to determine the duty cycle for the switches and the DC values of currents and voltages in all transfer sources. Energy equations can then be used to determine critical values for inductors and capacitors, and, if ripple factors are known, more accurate values for these components can also be determined.

Before formulating the equations for a converter some implementation characteristics must be stated:

1. The important input and output variables are voltages. Input (output) current sources are implemented by an input (output) voltage source in series with an inductor of an appropriate size.
2. Transfer current sources are implemented by inductors of appropriate sizes.
3. Transfer voltage sources are implemented by capacitors of appropriate sizes.
4. Input voltage sources are implemented by real voltage sources.
5. Output voltage sources are implemented by a capacitor of an appropriate size.

A Modified Nodal Analysis (MNA) formulation of the form $\mathbf{A_i x} = \mathbf{b_i}$ can be found for each switch configuration i of a power converter, where $\mathbf{A_i}$ is the MNA system matrix during the ith part of the operating cycle, $\mathbf{x}$ is the vector of node voltages, voltage supply currents and inductor currents, and $\mathbf{b_i}$ is the vector of independent voltage and current sources. In the average, a circuit with two different states can be represented as [5]

$$[d(\mathbf{A_1} - \mathbf{A_2}) + \mathbf{A_2}]\mathbf{x} = d(\mathbf{b_1} - \mathbf{b_2}) + \mathbf{b_2} \qquad (1)$$

where d is the duty cycle–indicating how long the first part of the operation cycle lasts, as a fraction of the period, $\mathbf{A_1}$ is the MNA matrix for the circuit during the first part of the operation cycle, and $\mathbf{A_2}$ is the MNA matrix of the circuit during the rest of the cycle. The problem with ideal switched networks and MNA is that the different switch configurations produce different circuit topologies, requiring totally different MNA matrices–different in size and in the meaning of the rows and columns. In particular, whenever a switch is closed, two nodes become identical, and since the system becomes singular, one of the nodes is dropped. Comparison and averaging techniques don't make any sense then, since the subsystems are different. The solution to this inconvenient is to build the matrices for all the switch states keeping all the original nodes of the circuit. The information contained in those matrices is right, althogh the matrices are singular. After averaging the matrices, the resulting system is non-singular. For example, the MNA equations for the buck converter of figure 3, when switch #1 is closed are

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ -1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} -I \\ I \\ 0 \\ v_i \\ v_o \end{bmatrix} \qquad (2)$$

and when switch #1 is open, they are

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} -I \\ I \\ 0 \\ v_i \\ v_o \end{bmatrix}. \qquad (3)$$

In the average, the circuit can be represented as

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ -d & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} -dI \\ I \\ 0 \\ v_i \\ v_o \end{bmatrix}. \qquad (4)$$

The particular problem of converter design has some differences with the above formulation

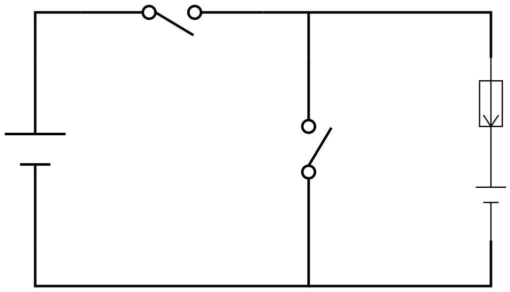

Figure 3: Circuit variables in a buck converter.

1. The current in the output voltage source is known, because the load for the converter is known.
2. All current sources are unknown.
3. Except the input and output voltage sources, all voltage sources are also unknown.

The equations need to be reformulated as

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & -1 \\ -1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ I \end{bmatrix} = \begin{bmatrix} 0 \\ -i_2 \\ 0 \\ v_i \\ v_o \end{bmatrix}, \qquad (5)$$

for the case of switch #1 closed,

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ I \end{bmatrix} = \begin{bmatrix} 0 \\ -i_2 \\ 0 \\ v_i \\ v_o \end{bmatrix} \qquad (6)$$

for the case of switch #1 open, and in the average

$$\begin{bmatrix} 0 & 0 & 0 & 1 & d \\ 0 & 0 & 0 & 0 & -1 \\ -d & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_1 \\ I \end{bmatrix} = \begin{bmatrix} 0 \\ -i_2 \\ 0 \\ v_i \\ v_o \end{bmatrix}. \qquad (7)$$

At this point, the system has more unknowns than equations and seems impossible to solve. Fortunately, in the average representation, there are more equations that can be used: the power dissipated in each transfer source is zero (only in the average). This can be stated by saying that the voltage across a current source is zero and the current through a voltage source is also zero. In the case of figure 3, the new equation is $v_2 - v_3 = 0$.

In the general case, the original MNA formulation for a converter with k transfer sources gives a system with n equations and n unknowns. The new average formulation drops the output current unknown, adds the duty cycle as a new unknown, adds k unknowns for the transfer sources values, and adds k equations for the ideal effect of these sources. The system has now $n + k$ equations and $n + k$ unknowns and can be solved. The system is nonlinear because of the way in which d appears in the equations, but it is still easy to solve, though, because the matrix is made mostly of $1's$ and $0's$.

To make all this process easy to carry, averaged stamps can be found for the different elements in the ideal representation of a power converter.

Once this system of equations is solved and the values of all dc currents and voltages for transfer sources are known, as well as the duty cycle d, critical values for the capacitors and inductors in the real circuit can be found. In the example above, the critical inductance is $L = (v_i - v_o)d/2If$, where f is the operating frequency of the circuit.

2.3 Smart layout parasitic calculation.

As in all other electronic circuits, parasitics are an important issue in power electronics, because they usually represent power losses in a converter. One of the parasitic effects that is of special interest at the present is inductance. We propose that magnetic parasitic effects be classified in two parts, that can be modeled and analyzed in different ways: 1. Effects intrinsec to magnetic devices, i.e., core and wire losses. Modeling of these effects is an active area of research and some models can be found in the literature [6], [7], [8]. 2. Effect produced by the circuit as a system, i.e., wiring parasitics. A relatively easy way to handle magnetic parasitics created by interconnections is to create a set of standard interconections and carefully study their magnetic properties. Then, a set of tables can be included in the optimization process, such that losses caused by different physical configurations of the circuit can be analyzed.

2.4 Simulation interface.

Once the parasitics are estimated, the next step in the design process is simulation, to anticipate the real behavior of the chosen configuration and test conformance to established requirements. A major issue in power electronics simulation is the fact that power converters are stiff systems, for which traditional SPICE-like simulations are very slow if an accurate solution is desired. A good simulator for power electronics should be able to find the steady state operation of a converter in a fast and efficient way. New variations of shooting methods especially intended for power electronics applications are being investigated [9].

2.5 Optimizer.

Before the final implementation of the converter, its component values must be tuned to the best level of performance. This will be done by an optimizing system that needs initial guesses for the variables, a set of performance parameters, and a cost function. The initial guesses are the critical values found in the *component specification* section. The different performance parameters must be defined by the designer and are different for each particular application. Some of them include cost, efficiency, transient performance, steady-state performance, size and weight. From those parameters, all the electrical ones will be evaluated by the simulator; the non electrical ones must be calculated based on additional physical information about the circuit elements. Finally, the cost function and the relative weights of the various parameters must be determined by the user before performing the optimization.

3 Current and future work

At the present, progress is being made in the converter and component specification stages. In both cases, the methods to be used have been successfully tested on several dc-dc converters and the computer implementation of both is underway.

Possible techniques to avoid long simulations for steady-state operation are being investigated for the simulation stage. Appropriate modeling of power electronic components, especially magnetics and parasitics will be incorporated into this work. As a start, the simulation effort is being concentrated on basic DC-DC converters, but it is expected that the results can be generalized to resonant DC converters, rectifiers and inverters.

References

[1] D. Maksimović and S. Ćuk, "General properties and synthesis of pwm dc-to-dc converters", *IEEE Power Electronics Specialists Conference*, pp. 515–525, 1989.

[2] R. Tymersky and V. Vorpérian, "Generation, classification and analysis of switched-mode dc-to-dc converters by the use of converter cells", *Proceedings IEEE INTELEC*, pp. 181–195, 1986.

[3] R. W. Erickson, "Synthesis of switched-mode converters", *IEEE Power Electronics Specialists Conference*, pp. 9–22, 1983.

[4] P. Wood, *Switching Power Converters*, Van Nostrand, New York, NY, 1981.

[5] S. R. Sanders and G. C. Verghese, "Synthesis of averaged circuit models for switched power converters", *IEEE Transactions on Circuits and systems*, vol. 38, no. 8, pp. 905–915, August 1991.

[6] F. D. Tan, J. L. Vollin, and S. M. Ćuk, "A practical approach for magnetic core-loss characterization", *IEEE Transactions on Power Electronics*, vol. 10, no. 2, pp. 124–130, Mar 1995.

[7] J. G. Zhu, S. Y. R. Hui, and V. S. Ramsden, "A generalized dynamic circuit model of magnetic cores for low- and high-frequency applications–part i: Theoretical calculation of the equivalent core loss resistance", *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 246–250, Mar 1996.

[8] J. G. Zhu, S. Y. R. Hui, and V. S. Ramsden, "A generalized dynamic circuit model of magnetic cores for low- and high-frequency applications–part i: Circuit model formulation and implementation", *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 251–259, Mar 1996.

[9] U. Ekambaram and R. A. Saleh, "An improved steady-state method applying broyden's technique to the shooting method", *Proceedings of the Midwest Symposium on Circuits and Systems*, 1996.