DESIGN OF AN A/D CONVERTER USING COMPLEMENTARY THREE-INPUT AMPLIFIERS

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1. Introduction

This paper present a technique that allows the implementation of analog-to-digital converters using mainly active components. While total elimination of passive components is not possible, we have successfully removed the need for linear and well-matched ones. Capacitors in our circuits are solely for the purpose of voltage storage; the precision of voltage scaling is totally dependent on the matching of *active* components. While the resistive-ladder technique requires the matching of 2^N resistors, the technique introduced here requires matching only of MOSFETs in groups of four, one group for each amplifier used. Any improvements in active-device technologies will naturally lead to improvement in the performance of circuits described here.

2. An algorithmic A/D converter

The proposed A/D converter is shown in figure 1. The algorithmic A/D conversion technique is used. Voltage multiplication by two and voltage subtraction are performed by the complementary three-input amplifier (CTIAMP)[1]. When the CTIAMP is connected in a simple feedback configuration, as shown in figure 2, the output voltage can be expressed as

$$V_o=(1+\gamma)V_i-2\gamma V_{ref} \tag{1}$$

where γ is the ratio of d.c. gains of the two channels of the CTIAMP. If perfect matching of the two channels of the CTIAMP is achieved, then $\gamma=1$. In this case equation (1) reduces to its ideal form

$$V_o=2(V_i-V_{ref}) \tag{2}$$

3. Closed-loop-gain-error consideration

A basic schematic of the CTIAMP is shown in figure 3. Mismatches of the four critical transistors, n_1 and n_2 within each CTIAMP may lead to gain errors. The gain errors of the CTIAMP will cause differential and integral nonlinearities in the conversion characteristic of the A/D converter.

To determine at which point on the conversion-characteristic curve (or where the differential nonlinearity) is most sensitive to the closed-loop-gain error of the CTIAMP, we must identigy which input-voltage interval associated with two consecutive digital values is most sensitive to closed-loop-gain error of the CTIAMP:

If $k+1$ and k digital values have equal $i+1^{th}$ to N^{th} (or most) significant bits, then the first (or LSB) to the i^{th} bits of each digital value should be the complement of one another. It follows that the input-voltage interval associated with the $k+1$ and k digital values has the form

$$\frac{\Delta V}{V_{ref}}=2\gamma a_i(1+\gamma)^{i-1-N}-2\gamma a_{i-1}(1+\gamma)^{i-2-N}$$

$$-\cdots-2\gamma a_2(1+\gamma)^{1-N}-2\gamma a_1(1+\gamma)^{-N} \tag{3}$$

In deriving equation (3), equation (1) has been used.

Since the constants $a_i,\ldots,a_1$ in equation (3) must be 1, the equation can be simplified to

$$\Delta V=2\left\{(1+\gamma)^{(i-N)}-2(1+\gamma)^{(i-1-N)}+(1+\gamma)^{-N}\right\}V_{ref} \tag{4}$$

where $N\geq i>0$.

Differentiating equation (4) with respect to γ and setting γ equal to its nominal value of 1, equation (4) becomes

$$\frac{\delta\Delta V}{\delta\gamma}=\left\{2^i-N\right\}\frac{V_{ref}}{2^N} \tag{5}$$

Since $N\geq i>0$, the magnitude of $\delta\Delta V/\delta\gamma$ reaches its maximum value when $i=N$, that is when

$$\max\left|\frac{\delta\Delta V}{\delta\gamma}\right|=\left|\frac{\delta\Delta V}{\delta\gamma}\right|_{i=N} \tag{6}$$

Equation (6) shows that the nonlinearity of the first major carry is most sensitive to the closed-loop-gain error of the CTIAMP. This fact greatly simplifies the testing of an A/D converter using the CTIAMPs because only one measurement is needed to establish its maximum nonlinearity. Moreover, it also allows optimization of the design of the CTIAMP as discussed below:

If $V_i=V_{ref}+\varepsilon$ ($\varepsilon<V_{LSB}$), then the correct output digital value of the A/D converter should be 100...0. In this case, the output voltages of each CTIAMP are

$$V_1=2(V_i-V_{ref})=2\varepsilon,\ V_2=2(2\varepsilon)=4\varepsilon$$

$$\ldots,\ V_i=2^i\varepsilon,\ \ldots,\ V_N=2^N\varepsilon$$

As the value of ε approaches V_{LSB}, $2^N\varepsilon$ approaches $2V_{ref}$. It follows that for a correct output digital value,

$$V_1>0 \tag{7}$$

[1] A related circuit, the three-input amplifier, which has two positive and one negative input terminals, has been used in the implementation of a D/A converter reported earlier [2].

and

$$V_N<2V_{ref} \tag{8}$$

If the condition expressed by equation (7) is not met then the output digital value becomes 011...1; however, if the condition expressed by equation (8) is not met then the output digital value becomes 100...01. Since the transition (011...1, 100...0) is more sensitive to the closed-loop-gain error of the CTIAMP than the transition (100...0, 100...01) (see equation (6)), the condition expressed by equation (7) dominates.

Similarly, for an output digital value of 011...1, we have

$$V_1=2(V_i-V_{ref})<0 \tag{9}$$

$$V_N=2V_{ref}-2^N\varepsilon > 0 \tag{10}$$

given that

$$V_i=V_{ref}-\varepsilon;\ \varepsilon<V_{LSB} \tag{11}$$

Following a similar argument, the condition expressed by equation (9) dominates.

The voltage across each input of the CTIAMP for input voltages in the range $0<V_i<2V_{ref}$ is plotted in figure 4. Under both conditions expressed by equations (7) and (9), the input voltage is in the range

$$V_{ref}-\varepsilon<V_i<V_{ref}+\varepsilon \tag{12}$$

Therefore, to minimize the nonlinearity of the A/D converter, the CTIAMP should be designed such as to minimize the closed-loop-gain error for input voltages in the range expressed by equation (12). In another words, the closed-loop-gain error of the CTIAMP in the two configurations shown in figure 5 should be kept to a minimum. Note that in both of these configurations, the voltage across each pair of input terminals is V_{ref}, which is the largest possible input value. In order to minimize the closed-loop-gain error for large input voltages, the biasing current of the CTIAMP should be large [2], [3].

The discussion above has established the fact that the nonlinearity at the first major carry is most sensitive to the closed-loop-gain error of the CTIAMP; however, we have not yet quantified the minimum closed-loop-gain error of the CTIAMP required for a given accuracy of A/D conversion. Figure 6 shows the ideal and practical conversion characteristics of an A/D converter. From the figure, we may deduce that the integral nonlinearity of the A/D converter is given by

$$INL=\tfrac{1}{2}\left\{\left[k_U+k_L\right]-\left[k_U+k_L\right]\right\} \tag{13}$$

where k_U, k_U, k_L and k_L are the ideal and practical upper and lower input-voltage boundaries, respectively.

Consider the case of an output digital value of 100...0, for which the output voltage of the last CTIAMP can be expressed as

$$V_N=kV_{ref}(1+\gamma)^N-2\gamma(1+\gamma)^{N-1}V_{ref} \tag{14}$$

for

$$V_i=kV_{ref}\ . \tag{15}$$

The practical upper input-voltage boundary is given by

$$V_N-2\gamma V_{ref}=0 \tag{16}$$

It follows that

$$k_U=2\gamma(1+\gamma)^{-1}+2\gamma(1+\gamma)^{-N} \tag{17}$$

The ideal upper input-voltage boundary can be found by setting $\gamma=1$ in equation (17), giving

$$k_U=1+2^{1-N}\ . \tag{18}$$

The practical lower input-voltage boundary is given by

$$V_N=0, \tag{19}$$

which leads to

$$k_L=2\gamma(1+\gamma)^{-1}\ . \tag{20}$$

Setting $\gamma=1$ gives

$$k_L=1\ . \tag{21}$$

Combining equations (13), (17), (18), (20) and (21), we get

$$INL=2\gamma(1+\gamma)^{-1}+\gamma(1+\gamma)^{-N}-1-2^{-N}\ . \tag{22}$$

For integral nonlinearities (INL) of +0.5 LSB and -0.5 LSB, the corresponding polynomial equations are respectively,

$$2\gamma(1+\gamma)^{-1}+\gamma(1+\gamma)^{-N}-1-2^{1-N}=0 \tag{23}$$

and

$$2\gamma(1+\gamma)^{-1}+\gamma(1+\gamma)^{-N}-1=0 \tag{24}$$

Equations (23) and (24) can be solved numerically. Results are provided in Table 1 for $N=4$ to $N=12$. The table also shows INLs for other output digital values. It is obvious that the requirement on γ is most stringent for the output digital value of 100...0.

The differential nonlinearity (DNL) of an A/D converter is a measure of the deviation of the spacing between two consecutive output digital values and thus it is associated with a pair of output digital values. Referring to figure 7, the input-voltage interval between i and $i+1$ digital values is given by

$$V(i,i+1)=\tfrac{1}{2}(k_U(i+1)-k_L(i)) \tag{25}$$

For a DNL lower than 0.5 LSB,

$$V(i,i+1)\ <\ 1.5\,\frac{V_{LSB}}{V_{ref}}\ . \tag{26}$$

It follows that

$$k_U(i+1)-k_L(i)\ <\ 3\,\frac{V_{LSB}}{V_{ref}}\ \ or\ \ 3(2^{1-N})\ . \tag{27}$$

Similarly, for a DNL higher than -0.5 LSB,

$$k_U(i+1)-k_L(i)\ >\ LSB\ \ or\ \ 2^{1-N}\ . \tag{28}$$

Combining (27) and (28), we get

$$2^{1-N}\ <\ k_U(i+1)-k_L(i)\ <\ 3(2^{1-N}) \tag{29}$$

For the case of (011...1, 100...0),

$$DNL(011...1,\ 100...1) =$$

$$\tfrac{1}{2}\left\{k_U(100...0) - k_L(011...1)\right\} \tag{30}$$

where

$$k_U(100...0) = 2\gamma(1+\gamma)^{-1}+2\gamma(1+\gamma)^{-N} \tag{31}$$

and

$$k_L(011...1) = 2\left\{(1+\gamma)^{-1}-(1+\gamma)^{-N}\right\} \tag{32}$$

Using equations (30), (31) and (32), for the cases of $DNL < 0.5\ LSB$ and $DNL > -0.5\ LSB$, we get

$$2(\gamma-1)(1+\gamma)^{-1}+2(1+\gamma)^{-N}(1+\gamma)-6(2^{-N})=0 \tag{33}$$

and

$$2\gamma(1+\gamma)^{-1}+2\gamma(1+\gamma)^{-N}-2(1+\gamma)^{-1}+2(1+\gamma)^{-N}-2^{1-N}$$

$$=0 \tag{34}$$

respectively.

Equations (33) and (34) can be solved numerically. Some results are listed in Table 2. Table 2 also shows the case of (100..0, 100...01). Clearly, the DNL for (011...1, 100...0) dominates.

4. Input offset-voltage considerations

Due to the relatively small size of the differential-pair transistors used in the CTIAMP, the worst-case-input-offset voltage has been measured to be as high as 0.1V. This input-offset voltage will lead to nonlinearity in the conversion characteristic.

For nonlinearity less than 0.5 LSB, the output-offset voltage of the CTIAMP must be less than $\frac{1}{2} V_{LSB}$. Thus, without offset-voltage compensation, our CTIAMP design, with a 0.1V output-offset voltage, limits the accuracy of the A/D converter unacceptably to fewer than 5 bits (for $V_{ref} = 1.5V$).

The output-offset voltage of the CTIAMP can be cancelled by using a double-differential-pair-offset-cancellation technique described in [3]. After the offset-cancellation circuit is incorporated the output-offset voltage can be reduced to less than 1mV.

6. Operating speed considerations

There are two important time delays that the designer must consider when estimating the operating speed of the CTIAMP A/D converter. One time delay, t_{s1}, is the time for the output voltage of the CTIAMP to settle to its correct polarity (while the amplitude might still be growing) and the other time delay, t_{s2}, is the time taken for the output voltage of the CTIAMP to settle to within $\frac{1}{2} V_{LSB}$ of its final value. The time delay, t_{s1}, establishes when to sense the polarity of the output voltage of the CTIAMP after both V_i and V_{ref} are applied. For the two cases, $V_i \gg V_{ref}$ or $V_i \ll V_{ref}$, t_{s1} is not of major concern. However, t_{s1} becomes important when $V_i \simeq V_{ref}$, or more precisely,

$$V_i=\frac{2\gamma}{1+\gamma}V_{ref}\pm\varepsilon_v \tag{35}$$

where $\varepsilon_v \le \frac{1}{2} V_{LSB}$.

For the CTIAMP circuit shown in figure 3, SPICE simulation indicates the output voltage to be 0.7 mV when $V_i=V_{ref}=1V$. This gives $\gamma=0.9993$, and equation (35) becomes

$$V_i=0.99965\pm\varepsilon_v$$

For an 8-bit system with $V_{ref}=1V$, $V_{LSB}=7.8\ mV$, thus $\varepsilon_v=3.9\ mV$. It follows that

$$V_i = 0.99575V \text{ or } 1.00355V$$

SPICE simulation shows that t_{s1} is less than 50 ns for both cases of $V_i = 0.99575V$ and $1.00355V$. It also shows that the time taken, t_{s2}, for the output voltage to settle to within $\frac{1}{2} V_{LSB}$ of its final value is 330 ns. Thus, the total time taken for the conversion of one bit is nominally 380 ns.

When pipelining is used, to eliminate the extra time taken for the output voltage of the S/H to settle to its final value, two S/Hs are needed per each stage of the A/D converter. The two S/Hs are clocked at a rate equal to $\frac{1}{2}$ the bit-conversion rate. While the one S/H is holding the output voltage of the previous stage of the previous bit-conversion cycle, the other is tracking the current output of the previous stage. This allows the overlapping of the settling times of both the CTIAMP and the S/H.

Allowing 50 ns each for offset-cancellation of the CTIAMP and the voltage comparison, the period for the bit-conversion is less than 500 ns. It follows that the frequency of sampling of the pipelined A/D converter is approximately 2 MHz. A higher frequency of sampling can be achieved by using faster CTIAMP designs or at the expense of using more CTIAMPs and S/Hs.

7. Conclusion

This paper has described the design of an A/D converter using a building block called the Complementary Three-Input Amplifier (CTIAMP). The closed-loop gain of the CTIAMP is solely dependent on the matching of active devices, while passive devices are used only for voltage storage or frequency compensation.

The technique of conversion described in the paper may be used to implement 8-bit A/D converters having a DNL of less than 0.5 LSB. The speed of conversion is 2 MHz if pipelining is used.

8. References

[1] C.C. Shih and P.R. Gray: "Reference-refreshing cyclic analog-to-digital and digital-to-analog converters," IEEE J. of Solid-State Circuits, Vol. SC-21, Aug. 1986, pp. 544-554.

[2] C.P. Chong, K.C. Smith, and Z.G. Vranesic: "Using active components to perform voltage division in digital-to-analog conversion," Proc. 1988 Symposium on VLSI Circuits, Tokyo, Japan, pp. 119-120.

[3] C.P. Chong, and K.C. Smith: "A high-resolution CMOS comparator," International J. Electronics, Vol. 64, 1988, pp.409-415.

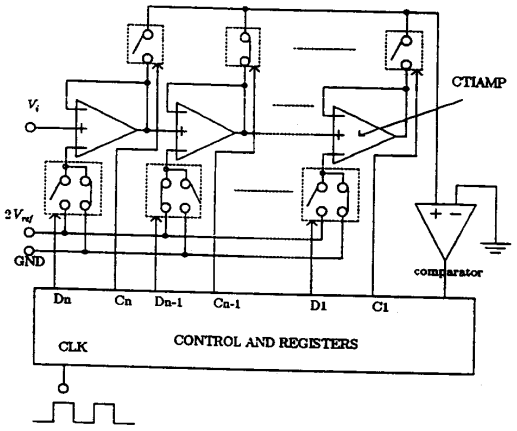

Figure 1: An A/D converter using complementary three-input amplifiers

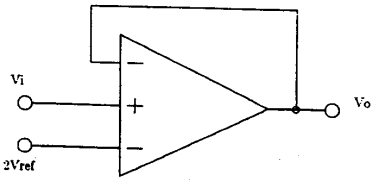

Figure 2: The complementary three-input amplifier in a simple feedback configuration

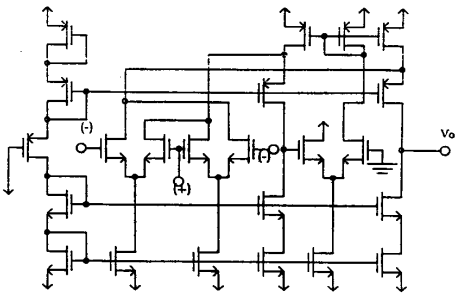

Figure 3: The schematic of the CTIAMP

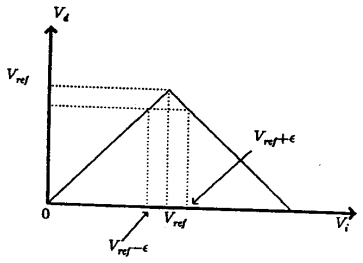

Figure 4: The voltage across each of the input pairs of the CTIAMP

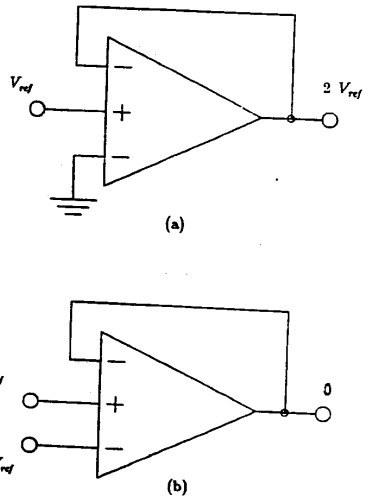

Figure 5: The configurations of the CTIAMP when input voltage (a) is slightly lower, and (b) is slightly higher than the reference voltage

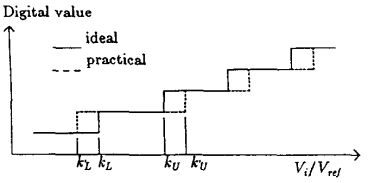

Figure 6: The INL of an output digital value

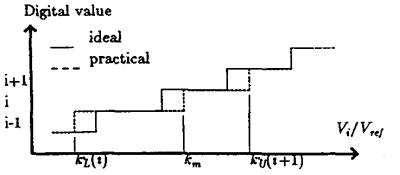

Figure 7: The DNL of two consecutive digital values

For integral nonlinearity lower than 0.5 LSB										
N	4	5	6	7	8	9	10	11	12	γ
100...0	15.3%	7.1%	3.3%	1.6%	0.8%	0.3%	0.2%	0.1%	0.05%	>1
0100...0	-	-	-	-	-	-	-	-	-	-
00100...0	33.7%	17.6%	9.8%	5.3%	2.8%	1.5%	0.6%	0.4%	0.2%	<1
00...01	29.3%	18.9%	14.1%	11.3%	9.4%	8.1%	7.1%	6.3%	5.7%	<1
1010...10	28.9%	14.4%	7.1%	3.6%	1.8%	0.9%	0.4%	0.2%	0.1%	>1
1010...101	23.1%	12.3%	6.5%	3.3%	1.7%	0.8%	0.4%	0.2%	0.1%	>1
For integral nonlinearity higher than -0.5 LSB.										
100...0	13.3%	6.7%	3.2%	1.6%	0.8%	0.4%	0.2%	0.1%	0.05%	<1
0100...0	62.8%	54.3%	43.3%	31.8%	22.1%	15.1%	10.3%	7.1%	4.9%	<1
0100...0	68.4%	44.5%	30.4%	21.4%	15.2%	10.9%	7.9%	5.7%	4.1%	>1
00100...0	36.5%	19.1%	10.3%	5.5%	2.9%	1.5%	0.8%	0.4%	0.2%	>1
00...01	41.3%	27.8%	20.8%	16.6%	13.8%	11.8%	10.3%	9.2%	8.3%	>1
1010...10	20.6%	12.3%	6.7%	3.5%	1.8%	0.9%	0.4%	0.2%	0.1%	<1
1010...101	17.5%	10.7%	6.0%	3.2%	1.7%	0.9%	0.4%	0.2%	0.1%	<1

Table 1: Integral nonlinearities of the A/D converter. This table shows for example that gain matching of the two channels of the CTIAMP should be better than 0.797% if an integral nonlinearity of less than 0.5 LSB and an accuracy of 8 bits are required

For a differential nonlinearity lower than 0.5 LSB										
N	4	5	6	7	8	9	10	11	12	γ
011...11, 100...00	20.9%	8.5%	3.7%	1.7%	0.8%	0.4%	0.2%	0.1%	0.049%	>1
100...00, 100...01	42.9%	26.7%	19.8%	15.9%	13.2%	11.4%	9.9%	8.9%	8.0%	<1
For a differential nonlinearity higher than -0.5 LSB.										
011...11, 100...00	19.4%	8.2%	3.7%	1.7%	0.8%	0.4%	0.2%	0.1%	0.05%	<1
100...00,100...01	72.7%	48.7%	36.4%	29.0%	24.0%	20.5%	17.9%	15.9%	14.3%	>1

Table 2: Differential nonlinearities of the A/D converter. This table shows for example that gain matching of the two channels of the CTIAMP should be better than 0.824% if a differential nonlinearity of less than 0.5 LSB and an accuracy of 8 bits are required