SC AND PASS TRANSISTOR COMBINED CIRCUITS

Indexing terms: Logic and logic design, Circuit theory and design

The pass-transistor structure provides a powerful tool for the implementation of binary and multiple-valued logic (MVL). Circuit realisation of any general MVL function using literals, MAX and MIN is easy. However, the resulting circuits have certain limitations. A combination of pass transistors (PT) with switched-capacitor (SC) circuits is shown to provide useful improvements.

Introduction: The conventional pass-transistor (PT) scheme for the creation of logic functions is a simple and straightforward idea in either binary or multiple-valued logic (MVL). It uses strings of transistors as switches, controlled by a bank of literals, to connect the desired logic value to the output. The basic structure for multiple logic values is shown in Fig. 1, where X indicates a switch (or simply a single pass transistor), controlled by an input through a literal gate or threshold function.

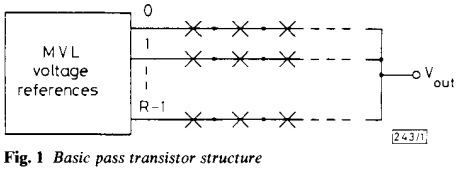

Fig. 1 *Basic pass transistor structure*

The realisation of a MVL function expressed by literals, MIN and MAX, is possible with this circuit structure.[1-3] However there are some restrictions. In the following, limitations of the PT scheme and possible improvements with SC[4] are discussed in more detail.

Limitations of PT: There are several limitations associated with the conventional pass-transistor circuits. There is the necessity of mutually exclusive conduction of PT strings. Taking a particular four variable quaternary function, as an example, where the superscript on each X_i indicates the range of value of input X_i over which the switch is closed (the literal function).

$$\begin{aligned} F(x) &= f_0 + f_1 + f_2 + f_3 \\ &= f_0 + 1({}^0X_1^{1\,2}X_2^{2\,1}X_3^{3\,2}X_4^2) \\ &\quad + 2({}^1X_1^{1\,3}X_2^{3\,2}X_3^{3\,1}X_4^2) \\ &\quad + 3({}^0X_1^{2\,2}X_2^{3\,1}X_3^{1\,2}X_4^2) \end{aligned} \tag{1}$$

It can be observed that f_1 and f_3 both contain the term

$$({}^0X_1^{1\,2}X_2^{2\,1}X_3^{1\,2}X_4^2)$$

Two transistor paths will conduct simultaneously for this particular input combination if the formula is directly implemented by a pass-transistor circuit without any modification. The resulting output would be ambiguous. Since (in eqn. 1) the plus sign (+) indicates a MAX function, the desired output value at this particular input should logically be 3. Therefore, the term

$$1({}^0X_1^{1\,2}X_2^{2\,1}X_3^{3\,2}X_4^2)$$

must be changed to the term

$$1({}^0X_1^{1\,2}X_2^{2\,2}X_3^{3\,2}X_4^2)$$

to correspond.

For more complex expressions, detection of every overlap is difficult to guarantee. One simple technique employed to avoid this problem is to use only base literals (${}^aX^a$), this restriction can greatly increase the circuit complexity.

The second limitation is the requirement for the provision of an explicitly defined f_0. An MVL formula normally does not contain the term f_0 because a MIN gate provides a zero logic value in default, when any literal in a product is zero. The MVL function would assume a zero if all the product terms are zero. For the pass-transistor scheme the zero must be supplied separately since there is no other mechanism by which the output can assume a logic value of zero when all the strings are at the high-impedance state (indicating that all the product terms are zero). To resolve this an expensive zero term must be added explicitly

$$\begin{aligned} f_0 = 0(\overline{{}^0X_1^{1\,2}X_2^{2\,1}X_3^{3\,2}X_4^2}) \,.\, (\overline{{}^1X_1^{1\,3}X_2^{3\,2}X_3^{3\,1}X_4^2}) \\ .\, (\overline{{}^0X_1^{2\,2}X_2^{3\,1}X_3^{1\,2}X_4^2}) \end{aligned} \tag{2}$$

The third point to note concerns the complexity of providing multiple reference values from which the output value is established by the pass-transistor network. Voltage references can be generated locally by a voltage divider, perhaps a stack of diode connected MOS transistors, as suggested by Current for the binary-to-quaternary decoder circuit.[5] One disadvantage of this method is the large biasing current required by the large MOS devices necessary to ensure sufficient driving capability. Another drawback is the limited number of voltage signals that can be generated by a MOS stack in a single threshold technology. This restricts its use in high radix operations.

The fourth limitation is the undesirable effects of large stray capacitances. The limited operational speed and signal deterioration of a pass-transistor circuit are largely caused by the series impedances and stray capacitances of the transistor paths. In the worst case, a voltage reference must charge or discharge not one, but all, the paths connected to the same output nodes. If the radix used is high, and more paths are required, the total charge required can be very large. Signal restoration may also be needed at some points in a circuit, and a signal restorer in any MVL technology is typically non-trivial.

Improvements possible with SC: The addition of techniques available from switched-capacitor (SC) technology allows us to overcome the difficulties listed. In contrast to MOS stacks as voltage sources, SC circuits provide virtually no limit in the creation, at low impedance, of any desired voltage. In particular, the low output impedance of the operational amplifiers used by SC circuits in a feedback loop ensures a much greater driving capacity than does a MOS stack.

Because, at any moment, only one logic value is needed for connection to the output, one operational amplifier would suffice. But in that case, for a simple implementation, the pass-transistors would not be in the signal path. They would become part of the control circuit. The nodes that were once used to connect to various voltage references are now used to control an SC adder. The node that was the output is now connected to the power supply. A quaternary circuit illustrating this idea is shown in Fig. 2. Binary logic gates, between the PT network and the SC input, implement the MAX function. The left ends of the unit capacitors C are lowered from the upper binary value to zero as the upper, middle, or lower pass paths are energised.

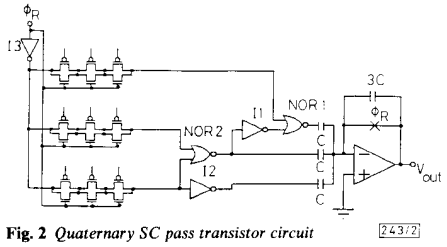

Fig. 2 *Quaternary SC pass transistor circuit*

This design does not require the explicit term f_0 because every time the output of the operational amplifier is reset to zero it remains at zero if no charge transfer is provoked. Through the OR gates, the paths of lower logic value are masked by the higher logic-value paths to effect the MAX

function. Overlapping of product terms, as in a normal MVL formula, is therefore allowed. This relaxation can lead to fewer logic gates and a simpler structure for the literal gates. For instance, the MVL function

$$f(x) = 1({}^0X_1^1\,{}^0X_2^2\,{}^3X_3^3) + 2({}^0X_1^2\,{}^3X_2^3\,{}^3X_3^3) + f_0 \quad (3)$$

can be converted to

$$f(x) = 1({}^0X_1^1\,{}^3X_3^3) + 2({}^0X_1^2\,{}^3X_2^3\,{}^3X_3^3) \quad (4)$$

Regarding the speed of operation for the conventional pass-transistor scheme, the output node must be directly charged to the intended logic reference value through the switch string, where the transfer of the last few percent of charge is always the most time-consuming. On the other hand, in the case of the SC version, the voltage at the end of each path needs only reach the threshold of the corresponding inverter. As these thresholds are usually in the vicinity of the middle of the power supply range, the time required is expected to be quite short.

Further circuit simplification can be obtained by using three diode-connected NMOS and three inverters to replace the two NOR and two inverters needed in the direct scheme for MAX function implementation. The circuit is shown in Fig. 3.

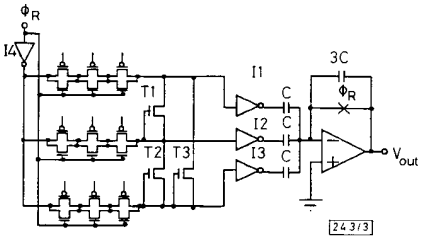

Fig. 3 *Simplified quaternary SC pass transistor circuit*

Conclusion: Several improvements to conventional pass-transistor structures for multiple-valued schemes are possible by combining SC and pass-transistor structures. They are

(*a*) The direct implementation of MVL functions expressed in literals, MAX and MIN, without the strict requirements of nonoverlapping of product terms.

(*b*) The elimination of the explicityly defined f_0.

(*c*) The use of single voltage source instead of a multiplicity of explicit MVL voltage references.

(*d*) The inherent restoring effect of the SC adder.

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MICROCHANNEL PLATE INTENSIFIER RESPONSE IN TRANSVERSE MAGNETIC FIELD

Indexing terms: Magnetic devices, Field effect devices

Gain and image shift measurements are presented for a proximity-focussed microchannel plate (MCP) image intensifier as a function of magnetic field (to 0·12 T) transverse to the optical axis. A simple model involving the angle of electron deflection, end-spoiled channel length and effective open area is described which agrees with the experiment.

Microchannel plate (MCP) image intensifiers are finding increasing uses in astronomy, high energy physics, biology and medicine. Some situations require operation in a large magnetic field,[1–3] and the resulting gain degradation is greatest when the MCP optical axis is oriented perpendicular to the field.[1,3] The present work provides a simple model, verified by experiment, that predicts gain as a function of transverse magnetic field.

In the absence of a magnetic field, electrons originating from the photocathode are directed by an electric field into the microscopic pores of the MCP where gain producing collisions with the inner walls occur. An orthogonal magnetic field deflects the electrons from the intended path. The higher the field strength, the larger the cycloidal curvature of electrons as illustrated in Fig. 1. Electrons enter the channel plate at angle

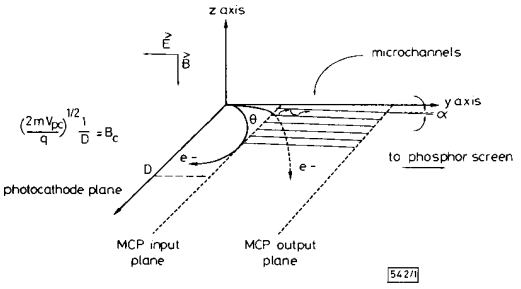

Fig. 1 *Electron trajectory in MCP*

Θ. The MCP output will be extinguished when electrons emitted by the photocathode do not reach the microchannel plate. As others[1,3] have shown, the value of this 'cutoff' magnetic field, B_c, is obtained from the Lorentz equation

$$\boldsymbol{F} = m_e(d^2\boldsymbol{r}/dt^2) = q[\boldsymbol{E} + (\boldsymbol{v} \times \boldsymbol{B})] \quad (1)$$

for a free electron moving in crossed electric, $\boldsymbol{E}$, and magnetic, $\boldsymbol{B}$, fields.

The solution yields the time dependence of the position of a given electron. For a photocathode voltage V_{pc}, and photocathode-to-MCP distance, D, this is

$$x = (E/\Omega B)[\Omega t - \sin(\Omega t)] \quad (2)$$

$$y = (E/\Omega B)[1 - \cos(\Omega t)] \quad (3)$$

where $\Omega = qB/m_e$ is the usual cyclotron frequency and $E = V_{pc}/D$. The electron charge to mass ratio is $q/m_e = -1{\cdot}75881962(53) \times 10^{11}$ C/kg. The field value necessary to induce a cycloidal motion with the maximum y value equal to D

$$B_c = [(2m_e V_{pc}/q)^{1/2}]/D \quad (4)$$

Significant gain loss will occur at field strengths less than B_c. To investigate gain decrease, we measured light output as a function of transverse magnetic field for an ITT model 4112 proximity focussed MCP image intensifier for several photocathode and MCP voltages. The value of $D = 250\,\mu$m was determined using an optical microscope. Channel diameter was $d = 12{\cdot}5\,\mu$m. The channels are biased at an angle $\alpha = 5°$.