# THE DESIGN OF A HIGH-RESOLUTION CMOS COMPARATOR

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**Abstract**

This paper describes the design of a high resolution CMOS comparator. Equations for the tradeoff among parameters such as offset-cancellation time, comparison time and input-voltage resolution are given. The cross-multiplexed technique (XMT) described in this paper has been used in the design of a CMOS comparator with an input-voltage resolution of 70 $\mu$V and a maximum comparison time of 1.8 $\mu$s.

## Introduction

Many techniques have been introduced in the literature for implementing high-speed high-resolution CMOS comparators. In general, during setup time, capacitors are used to store the input offset-voltage of the comparator, which is then subtracted from the input voltage during comparison time. Conventional single-ended CMOS comparators suffer from the large error voltage caused by the charge-pumping effect of the associated CMOS switch. While a differential CMOS comparator is able to cancel the error voltage partially due to its differential-input configuration, the effectiveness of such cancellation is very much dependent on the matching of the two channels of the comparator both electrically and physically. This puts additional constraints on the layout of the CMOS comparator.

Currently, a popular technique for reducing the charge-pumping effect employs two differential-input pairs [1], [2]. One differential pair performs the function of voltage comparison, while the other with a lower transconductance gain, performs the function of offset cancellation. This results in a great reduction in the effective error voltage caused by the charge-pumping effect.

In this paper, we study two CMOS comparators using the offset-cancellation technique described above. One of the two CMOS comparators analyzed uses a technique, called cross-multiplexed (XMT) to increase the effective input voltage [2]. The results of our analysis may be used to optimize the performance of these CMOS comparators for any given application.

## A CMOS comparator without the cross-multiplexed technique

Figure 1 shows the input stage of a CMOS comparator. One differential pair, $N_1$ with $N_2$, performs the function of voltage comparison, while the other differential pair, $N_3$ with $N_4$, performs the function of keeping the output voltage of the first stage to be approximately at $V_{ref}$. The magnitude of the effective error voltage $V_{os}$ has been shown to be [2]

$$V_{os}=\left(\frac{I_c\beta_{3,4}}{I_o\beta_{1,2}}\right)^{\frac{1}{4}}V_{oz}, \tag{1}$$

where $V_{oz}$ is the actual error voltage produced by the charge-pumping effect and, $\beta=W\mu C_{ox}/L$. Thus, $V_{os}$ may be made as small as possible by choosing $I_o\beta_{1,2}$ as large as possible.

The closed-loop gain of the differential pair, $N_3$ with $N_4$, after the switch is closed may be expressed as

$$\left(A_f\right)_{3,4}=\frac{A_{fm}}{1+\frac{s}{P_f}}, \tag{2}$$

where

$$A_{fm}=\frac{g_{m3,4}R_o}{1+g_{m3,4}R_o}\approx 1,\ P_f=\frac{1+g_{m3,4}R_o}{R_oC}\approx\frac{g_{m3,4}}{C}$$

and

$$C=C_1+C_1.$$

In the time domain, equation (2) has the form

$$V_c(t)=V_{ref}-\left[V_{ref}-V_c(0^+)\right]e^{\frac{-g_{m3,4}t}{C}} \tag{3}$$

We define the parameter, $\alpha$, the offset-cancellation factor as

$$\alpha=\frac{V_c(t_{oc})}{V_c(\infty)}=1-\left[1-\frac{V_c(0^+)}{V_{ref}}\right]e^{\frac{-g_{m3,4}t_{oc}}{C}}, \tag{4}$$

where $t_{oc}$ is the time allowed for offset cancellation. It follows that

$$t_{oc}=\frac{1}{P_f}\ln\left(\frac{1-\frac{V_c(0^+)}{V_{ref}}}{1-\alpha}\right), \tag{5}$$

From equation (1), we may write

$$\gamma=\frac{V_{os}}{V_{oz}}=\left(\frac{I_c\beta_{3,4}}{I_o\beta_{1,2}}\right)^{\frac{1}{4}}, \tag{6}$$

where $\gamma$ is termed the offset-improvement factor.

Since $P_f\approx\frac{g_{m3,4}}{C}$, we may express

$$P_f\approx\left(\frac{2I_c\beta_{3,4}}{C^2}\right)^{\frac{1}{4}} \tag{7}$$

Combining equations (6) and (7) we get

$$\gamma\approx P_f\left(\frac{C^2}{2I_o\beta_{1,2}}\right)^{\frac{1}{4}} \tag{8}$$

A figure of merit may be obtained by combining equations (5) and (8):



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$$t_{oc}\gamma \approx \left(\frac{C^2}{2I_o\beta_{1,2}}\right)^{1/4} \ln\left(\frac{1-\frac{V_c(0^+)}{V_{ref}}}{1-\alpha}\right) \qquad (9)$$

The three important parameters contained in equation (9) are $\alpha$, $t_{oc}$ and $\gamma$ which determine, respectively, the effectiveness of offset cancellation, the length of time for offset-cancellation and the magnitude of the effective error voltage due to charge pumping effect. Thus, for given values of $C$ and $I_o\beta_{1,2}$, a tradeoff between $t_{oc}\gamma$ and $\alpha$ may be performed using equation (9). A tradeoff between $t_{oc}$ and $\gamma$ may then be done by choosing an appropriate value for $I_o\beta_{3,4}$.

During the comparison phase of an operation cycle, the switch shown in figure 1 is open and the input voltage is applied to the input terminals of the differential pair, $N_1$ with $N_2$. However, the gain of the input stage is usually not high enough, and to increase the output voltage swing, the output of the input stage is coupled through a capacitor to two inverters connected in series, as shown in figure 2 [2]. By adding a third switch, $S_3$, which is turned on close to the end of the comparison phase, the output stage may be converted to a latch.

The a.c. model of the resulting comparator is shown in figure 3. We assume $C_c >> C_i$ and that $C_c$ may be replaced by a wire. The output voltage of the comparator in the time domain may be expressed as

$$V_o(t)=\frac{G_{m1}G_{m2}G_{m3}V_{im}}{6C_LC_i(C_1+C_i)}t^3+\frac{G_{m2}G_{m3}V_2}{2C_iC_L}\left[V_2(0^+)-V_{off1}\right]t^2$$
$$+\frac{G_{m3}}{C_L}\left[V_3(0^+)-V_{off2}\right]t+V_o(0^+), \qquad (10)$$

where $V_{off1}$ and $V_{off2}$ are the input offset voltages of the two inverters, and the input voltage is given by $V_i(t)=V_{im}u(t)$.

According to equation (10) the response time of the comparator is a function of the initial output voltages of each stage. If no offset-cancellation mechanism is employed, the response time of the comparator will be unpredictable, for it is a function of the input voltage in the previous cycle.

As well, the inverters have high frequency-cutoff characteristic, and the offset cancellation time of the output stage is certainly much smaller than that of the input stage. Thus, the offset cancellation time of the comparator as a whole is dominated by that of the input stage. It follows that, with the offset-cancellation mechanism, the response time may be expressed as

$$t_d=\left[\frac{6C_LC_i\left(C_1+C_i\right)\left[V_o(t_d)-V_o(0^+)\right]}{G_{m1}G_{m2}G_{m3}V_{im}}\right]^{1/3}. \qquad (11)$$

The value of $V_o(t_d)$ is dependent on the resolution of the latch. Since the effective offset voltage of the latch is $V_{off1}-V_{off2}$, it follows that $V_o(t_d)>|V_{off1}-V_{off2}|+V_o(0^+)$. If no latch is used ( $S_3$ is eliminated ) then $V_o(t_d)$ will have to be greater than $3V_{DD}/4$. Note that if a square-wave clock signal were to be used, the comparator should be optimized so that $t_{oc}$ is approximately equal to $t_d$.

### A CMOS comparator with the cross-multiplexed technique

When XMT is incorporated into the comparator, the input voltage is applied to the input terminals in both setup and comparison phases of an operation cycle. However, the polarity of the input voltage is reversed between the two phases of operation by the use of switches [2]. It has been shown elsewhere [2] that such reversal of the input-voltage polarity results in an improvement of the resolution of the comparator.

In this case, the output current of the differential pair, $N_1$ with $N_2$, is not zero during the setup phase (as shown in figure 4) and may be expressed as

$$I_{os}=\frac{V_{im}}{2}g_{m1,2} \qquad (12)$$

In order for the output current to be zero after an infinite interval of time, the final voltage across the capacitor ($C_1+C_i$) must be

$$V_c(\infty)=\frac{2I_{os}}{g_{m3,4}}+V_{ref} \qquad (13)$$

It follows that the output voltage may be expressed as

$$V_c(t)=\frac{2I_{os}}{g_{m3,4}}+V_{ref}-\left\{\frac{2I_{os}}{g_{m3,4}}+V_{ref}-V_c(0^+)\right\}e^{\frac{-g_{m3,4}}{C}t} \qquad (14)$$

The offset-cancellation parameter, $\alpha$, now becomes

$$\alpha=1-\left\{1-\frac{V_c(0^+)}{\frac{2I_{os}}{g_{m3,4}}+V_{ref}}\right\}e^{\frac{-g_{m3,4}}{C}t_{oc}} \qquad (15)$$

and

$$t_{oc}\gamma\approx\left(\frac{C^2}{2I_o\beta_{1,2}}\right)^{1/4}\ln\left\{\frac{1-\frac{V_c(0^+)g_{m3,4}}{2I_{os}+V_{ref}g_{m3,4}}}{1-\alpha}\right\} \qquad (16)$$

The value of $V_c(0^+)$ in this case is a function of both the leakage current of the capacitor and the input voltage during the previous setup phase. For the circuit shown in figure 1, for an input voltage with zero common-mode component, the value of $V_c(0^+)$ should stay between 0 V and $V_{DD}$ ($\approx 2V_{ref}$). Thus, according to equation (16), possible values of $t_{oc}\gamma$ should be

$$0<t_{oc}\gamma<\left(\frac{C^2}{2I_o\beta_{1,2}}\right)^{1/4}\ln\left(\frac{1}{1-\alpha}\right). \qquad (17)$$

At the end of the setup phase, the output current of the differential pair, $N_3$ with $N_4$, may be expressed as

$$\left|I_{d4}-I_{d3}\right|=\alpha I_{os} \qquad (18)$$

Thus, the total output current of the input stage is

$$i_{o1}=(1+\alpha)G_{m1}V_{im}, \qquad (19)$$

and the effective input voltage has been increased from $V_{im}$ to $(1+\alpha)V_{im}$.

This leads us to the comparison time given by

$$t_d=\left[\frac{6C_LC_i\left(C_1+C_i\right)\left[V_o(t_d)-V_o(0^+)\right]}{(1+\alpha)G_{m1}G_{m2}G_{m3}V_{im}}\right]^{1/3}, \qquad (20)$$

which has been decreased by a factor of $(1+\alpha)^{1/3}$.

Thus we have shown that incorporating the XMT into the comparator will lead to a lengthening of the offset cancellation time, a shortening of the comparison time and an increase in the resolution.

### SPICE simulation

To find out how well the analytical formulae described earlier predict the performance of the comparator, the circuit shown in figure 5 has been simulated using SPICE.

The transconductance of transistors $N_1$ and $N_2$ are $27*10^{-4}$ A/V and that of $N_3$ and $N_4$ are $3*10^{-5}$ A/V. The values for biasing currents $I_o$ and $I_c$ are 43.8 $uA$ and 2.91 $uA$ respectively.

The value of $\alpha$ is chosen to be 0.8. This leads to an increase in the resolution of the comparator by a factor of 1.8. The reference voltage is chosen to be 2.5V. The value of $V_c(0^+)$ is a function of leakage current through the switch and the error voltage

induced by charge-pumping. However, for worse cases, $V_c(0^+)$ is not likely to deviate from $V_{ref}$ by more than 20%. We choose, $V_c(0^+)/V_{ref}$=0.8.

Minimum-size transistors (W/L=6/3) are used in the second and third stages which are simple CMOS inverter. The grounded capacitors, $C_i$, at the inputs of second and third stages are the parasitic capacitors associated with the bottom plates of the input capacitors, $C_c$. The value of the parasitic capacitor, $C_i$ is approximately equal to that of the capacitor itself ($C_c$). The two capacitors at the inputs to second or third stage act as a voltage divider and reduce the effective transconductance gain of the inverter to one half of its original value. The value for the effective transconductance gain of the inverter may be calculated to be $4.82*10^{-5}$ A/V.

The input capacitors, $C_c$ and $C_i$, load the previous stage and the comparison time, $t_d$, will lengthen for larger values of $C_c$ and $C_i$. However, the input capacitors help to reduce the error voltage induced by charge-pumping by providing a larger node capacitance. Therefore, the larger the values of $C_c$ and $C_i$, the smaller the effect of charge pumping becomes.

The differences in comparison times obtained using simulation for the cases with and without XMT and the corresponding values obtained using the analytic formulae are plotted in figure 6. As shown in figure 6, discrepancies between the two values are the largest when $C_i$ is small. However, the discrepancies become smaller as the value of $C_i$ is increased. Note also that, the discrepancies for the case with XMT is also generally smaller.

The main cause of the discrepancies between the analytical prediction and the simulated results is the error voltage induced by charge-pumping, which leads to a shortening of the comparison time for one input-voltage polarity and the lengthening of the comparison time for the other. The effect of charge-pumping is reduced when $C_i$ is increased. The effect of charge-pumping may also be reduced by the use of XMT which increases the effective input voltage by a factor between 1 and 2. This is clearly indicated by the plot shown in figure 6.

Output waveforms of the CMOS comparator without XMT obtained using SPICE simulations for input voltages ranging from 300 $\mu$V to 380 $\mu$V are shown in figure 7. As shown in figure 7, the input-voltage resolution of the CMOS comparator without XMT is better than 380 $\mu$V. The maximum comparison time occurs for negative input voltages and is 1.4 $\mu$s at -360 $\mu$V. After XMT is incorporated, the resolution of the CMOS comparator is 160 $\mu$V and the maximum comparison time is still 1.4 $\mu$s.

To further reduce the input-voltage resolution of the CMOS comparator, the actual error voltage induced by the charge pumped out of the CMOS switch has to be minimized. It can be shown that

$$\frac{|V_e|_p}{|V_e|_n} = \frac{L_p W_n (V_{gsp} - V_{Tp})}{L_n W_n (V_{gsn} - V_{Tn})} \qquad (21)$$

Since the polarity of the error voltage induced by a PMOS device is opposite to that induced by an NMOS device, the magnitude of the two error voltages should be made equal in order to have complete cancellation. Therefore,

$$L_n W_n = 4.2 L_p W_n \qquad (22)$$

Since $L_p = 3\mu m$ and $W_p = 6\mu m$ (see figure 5), $L_n = 6\mu m$ and $W_n = 12\mu m$. In practice, complete cancellation of the error voltages cannot be achieved due to the quantization of the dimensions of the MOSFETs. When a CMOS switch with the optimized MOSFET dimensions is used, the output waveforms of the CMOS comparator with XMT for input voltages ranging from 10 $\mu$V to 70 $\mu$V are as shown in figure 8. As indicated, the input-voltage resolution has been reduced to 70 $\mu$V and the maximum time delay has become 1.8 $\mu$s.

## Conclusion

This paper has presented an analysis of comparators with and without the cross-multiplexed technique (XMT). Analytic formulae for the comparison time and the setup time of the comparator have been derived. The comparison times calculated are very close to those obtained using SPICE simulation for large coupling capacitances between stages. For small coupling capacitances, the effect of charge-pumping becomes significant and leads to a deviation of the predicted comparison times from those obtained using SPICE simulation. However, the use of XMT, which increases the effective input voltage and thus reduces the charge-pumping effect, leads to a closer agreement between the calculated and simulated comparison times, as well a significant reduction in the comparison time for cases with small coupling capacitance, where the magnitude of error voltage due to charge pumping is larger. The design example discussed in this paper has shown that it is possible to implement a CMOS comparator with an input-voltage resolution less than 100 $\mu$V and a maximum comparison time less than 2 $\mu$s, using XMT, the cross-multiplexed technique.

## References


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[2] Chong, C.P. and Smith, K.C.: "A high-resolution CMOS comparator," Int. J. Electronics, Vol. 64, Mar. 1988, pp. 409-415.

[3] Temes, G.C.: "Simple formula for estimation of minimum clock-feedthrough error voltage," Electronics Letters, Vol. 22, Sept. 1988, pp. 1069-1070.

[4] Gregorian, R. and Temes, G.C.: "Analog MOS integrated circuits for signal processing," Wiley-Interscience, New York, 1986.


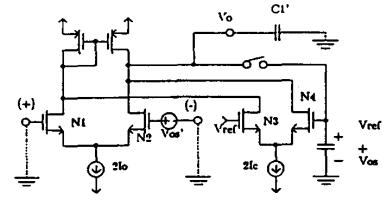


**Figure 1: The input stage of a CMOS comparator**

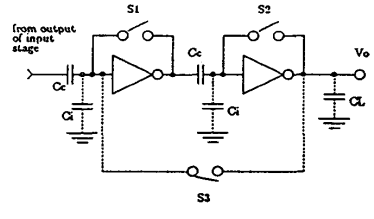


**Figure 2: The output stage of the comparator**



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Further information can be obtained from Dr. W. Kenneth Jenkins.

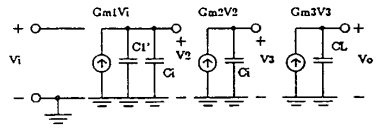


Figure 3: The a.c. model of the comparator

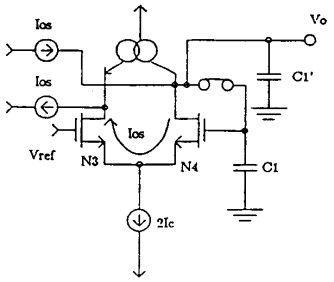


Figure 4: The input stage during the setup phase when the cross-multiplexed technique is employed

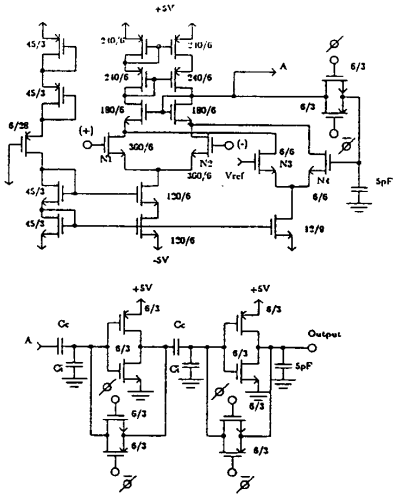


Figure 5: A schematic of the CMOS comparator

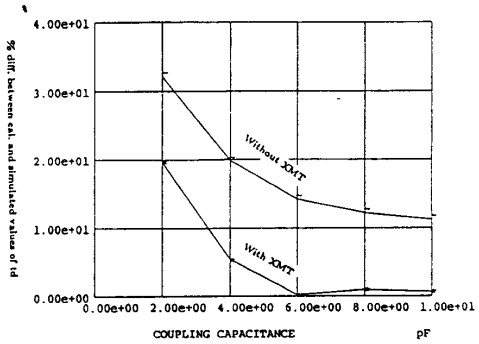


Figure 6: Differences between the calculated and the simulated comparison times

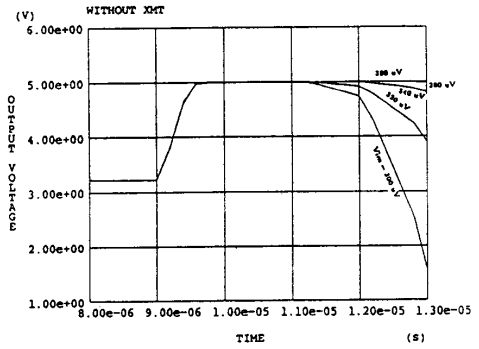


Figure 7: The output waveforms of the CMOS comparator without XMT

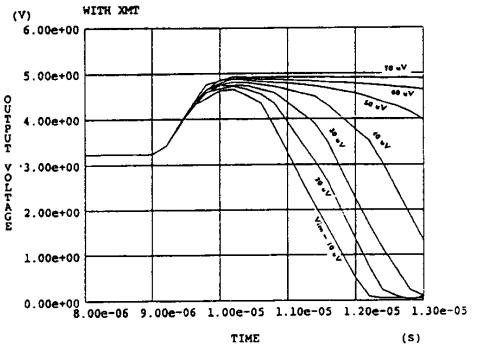


Figure 8: The output waveforms of the CMOS comparator with XMT and using CMOS switches with optimized transistor sizes