A CMOS CURRENT COMPARATOR WITH WELL-CONTROLLED HYSTERESIS

Chu Phoon Chong
Department of Electrical Engineering
University of Toronto and Ryerson Polytechnical Institute
Toronto, Ontario
Canada

Kenneth C. Smith
Department of Electrical Engineering
University of Toronto
Toronto, Ontario
Canada

Abstract

A CMOS current comparator with well-controlled hysteresis is described. The current comparator allows bidirectional input currents. Experimental results show that the current comparator takes approximately 300 ns to resolve a 2 μA difference of input and threshold currents.

Introduction

Signal processing traditionally occurs in the voltage domain. Generally speaking, current signals are generated in intermediate stages only when voltage signals prove to be impossible or inconvenient to process. However, voltage signals are often more susceptible to electromagnetic and thermal-noise interferences than current signals. As a result, digital-signal transmission is commonly done using current signals. Voltage signals are also slow to process generally. Thus at present, for example, high speed D/A converters have current-mode output [1].

The lack of circuit building blocks for current-signal processing makes straightforward conversion from voltage-signal to current-signal processing a difficult or impossible task. However, circuit building blocks such as current amplifiers [2, 3, 4, 5] and current comparators [6] have begun to appear in the literature, and significant attention has been paid recently to the area of current-signal processing. In this paper, we present a novel circuit of current comparator with well-controlled hysteresis.

Basic principle

Current comparison is a relatively simple process. It requires only injecting the two currents into a single node and employing the current flowing out of the node as the algebraic difference of the two input currents. Since most current sources have high output impedance, the nodal voltage generated by the output current is conveniently used to indicate the result of the current comparison.

The speed of comparison is a function of the parasitic nodal capacitance and the magnitude of the difference of the two currents. Assuming that the parasitic nodal capacitance is constant, the comparison time, t_d, can be estimated by

$$t_d = \frac{C_p\,\Delta V}{\Delta i} \tag{1}$$

where ΔV is the change in the nodal voltage, C_p is the parasitic nodal capacitance and Δi is the difference of the two current.

According to equation (1), infinitely small resolution of comparison can be achieved if infinitely long time of comparison is allowed. However, in actual circuit, duplicates of the input current and/or the reference current are required. Any mismatch of transistors used in duplicating these currents is the main source of errors limiting the resolution of the resolution of the current comparator.

Recently two current comparators with hysteresis are described [7, 8]. One current comparator [7] which is reproduced here in figure 1, makes use of a MOSFET, M5, controlled by the output voltage to produce the hysteresis required. The threshold current, I_{th}, is given by [7]

$$I_{th} = I_o + k_5\left[V_{dd} - V_{ss} - \left(\frac{2I_o}{k_2}\right)^{1/2} - |V_{Tp}|\right]\left[\left(\frac{2I_o}{k_3}\right)^{1/2} + |V_{Tp}|\right] - \tfrac{1}{2}k_5\left[\left(\frac{2I_o}{k_3}\right)^{1/2} + |V_{Tp}|\right]^2 \tag{2}$$

Since the threshold current, I_{th}, is a function of process parameters of the MOSFETs used, the hysteresis of this comparator is not well controlled. Moreover, this comparator has the disadvantage of allowing input current of unidirection only.

An improved circuit is described in [8] and is reproduced here in figure 2. The threshold current of the current comparator shown in figure 2 is given by [8]

$$I_{th} = I_l + I_o \tag{3}$$

which is independent of the process parameters of the MOSFETs. However, this circuit still has the disadvantage of allowing unidirectional-input current only.

A novel current comparator with well controlled hysteresis is shown in figure 3. The two diodes limits the input voltage to a reasonable range. Unlike the two previously discussed current comparator, the current comparator shown in figure 3 allows bidirectional-input current.

Referring to the current comparator shown in figure 3, MOSFETs p_1, p_2 and n_1, n_2 are matched pairs. The duplicates of the reference current, I_{ref}, is injected into the node C through the drains of MOSFETs p_2 and n_2 in series with two switches formed by MOSFETs, p_3 and n_3. The two switches (p_3 and n_3) form a complementary pair controlled by the output of the inverter, A_1. Since the loops form by the two switches (p_3 and n_3) and the inverter, A_1, have positive gain, a regenerative action which leads to hysteresis exists in the loops.

If $I_{in} \gg 0$, then a large current is flowing out of node C. This causes the lower input protection diode to turn on and the voltage at node C to be zero. Thus, the inverter senses an input of 0 and produces an output of 1 or $+V_{dd}$. This turns off p_3 and turns on n_3. As a result, another component of current equals to I_{ref} is flowing out of node C. If the input current starts to decrease and finally changes its direction, the voltage at node C will not change until $I_{in} = -I_{ref}$. Thus the negative threshold current of the hysteresis is $I_{th}^- = -I_{ref}$. At this instant, if the input current starts to change in the positive direction, the voltage at node C will not change until $I_{in} = I_{ref}$. Therefore, the positive threshold current is $I_{th}^+ = I_{ref}$. In summary,

$$I_{th}^+ = \left|I_{th}^-\right| = I_{ref} \tag{4}$$

Since the matching of MOSFET sizes on silicon chip can be done with high accuracy, the ratio of I_{th}^+ to I_{th}^- can be varied by changing the sizes of MOSFETs p_2 and n_2 with respect to the sizes of MOSFETs p_1 and n_1 respectively.

For a given sizes of MOSFETs p_3 and n_3, there exists an upper bound on the magnitude of the threshold currents. As the input current is approaching the threshold-current level, the voltage at node C starts to change to the opposite polarity. A large input impedance of node C during the transition of the associated nodal voltage will lead to a sharper transition. Therefore, it is desirable that the MOSFETs p_1 and p_3 (n_1 and n_3) be in saturated region of operation during the negative-edge (positive-edge) transition of the voltage at node C. This requires that $|V_{dsp2}|$, $|V_{dsp3}| \geq |V_{gsp2} - V_{Tp}|$. It follows that

$$\left(\frac{W}{L}\right)_p \geq \frac{2I_{ref}}{\mu_p C_{oxp}\Delta V_{gsp2}^2} \tag{5}$$

where $\Delta V_{gsp2} = V_{gsp2} - V_{Tp}$. Similarly,

$$\left(\frac{W}{L}\right)_n = \frac{2I_{ref}}{\mu_n C_{oxn}\Delta V_{gsn2}^2} \tag{6}$$

where $\Delta V_{gsn2} = V_{gsn2} - V_{Tn}$.

SPICE simulation

The current comparator shown in figure 3 is simulated using SPICE. The transfer curves of the current comparator using a reference current of 1 μA, 1.2 μA and 1.4 μA are plotted as shown in figure 4. The systematic mismatch of the MOSFETs used in the current mirrors lead to a shift in the threshold current by less than 10%. Figure 5 shows the input and output voltages of the current comparator. The reference current is set at 1 μA and

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the input current is a step function of time with step sizes ranging from 1.2 μA to 2 μA. With an input step size of 2 μA, the difference between the reference and the input current is 1 μA. For this case, as shown in figure 5, the response time of the current comparator is less than 200 ns. When the input step size is 1.4 μA and the difference between the reference and the input current is 0.4 μA, the response time increases to approximately 450 ns. When an input step size of 1.2 μA is used, the current comparator does not response correctly within a time interval of less than 0.5 μs.

The main factor that limit the speed of the current comparator is the RC low-pass network formed by the Miller capacitor across the input and the output of the inverter and the input impedance of the current comparator. To shield the effect of the Miller capacitor, which reaches its maximum value when the input voltage of the inverter reaches its threshold level, a buffer formed by MOSFETs p_4 and n_4 is added to the current comparator as shown in figure 6.

Plots of the input and the output voltages of the current comparator shown in figure 6 are shown in figure 7. The input current step sizes are from 1.2 μA to 1.4 μA. Comparing the plots in figure 5 to the plots in figure 6, an improvement of response time by 10% has been achieved after the buffer is incorporated.

In the current comparator shown in both figures 3 and 6, MOSFET p_4 or n_4 is deep in triode region when p_3 or n_3 is turned off by the output of the inverter. This reduces the speed of comparison. To provide an alternative path for the current flowing out of MOSFETs p_4 and n_4, two MOSFETs p_5 and n_5 are added to the current comparator as shown in figure 8. The output impedance of the current mirrors are also increased by using cascaded configuration.

Another function of MOSFETs p_5 and n_5 is to limit the input voltage of the current comparator which is usually done by the input protection diode. If the input voltage becomes excessively negative or positive, MOSFETs n_3 and n_5 or p_3 and p_5 provide a path for the excessive input current to flow. This is illustrated in figures 9(a) and 9(b). The two MOSFETs p_3 and n_3 are in triode region and the current is flowing in the reverse direction. A plot of the input voltage verses the input current obtained using SPICE simulation is shown in figure 10. For a reference current ranging from 1 μA to 1.4 μA, the input voltage is limited to the range of 1V to 4V.

A plot of the output voltage verses the input current is shown in figure 11. As shown in figure 11, the difference between the threshold current and the reference current is less than 1%, significantly smaller than the current comparators without using the cascaded current mirror.

The input and output voltage of the current comparator shown in figure 8 for input step current with step size ranging from 1.2 μA to 2 μA are plotted as shown in figure 12. The response time of the current comparator has been reduced significantly due to the addition of the buffer, to an increase in the input impedance of the current comparator and to the use of the current-steering technique for the current mirrors. The response time is less than 100 ns and 300 ns when the input-current-step size is 2 μA and 1.2 μA respectively.

Note that the output voltage of all current comparators discussed so far has a relatively low slew-rate leading to a less well defined transition edge. If a sharp and well defined transition edge is required, a second inverter connected in series with the first one is added to the current comparator as shown in figure 13.

Plots of the input and the output voltages of the current comparator shown in figure 13 are shown in figure 14. While the input voltage has zero slew-rate for a finite interval of time, the output voltage has a sharp and well defined transition edge. The zero slew-rate for input voltage occurs after n_3 is turned on and its drain-source current starts to increase from zero to the full magnitude of the reference current.

Silicon implementation

A current comparator based on the circuit shown in figure 3 has been designed and implemented on a silicon chip using 3μ-CMOS technology. The improved design of the current comparator shown in figure 8 is in the process of being laid out and no experimental data is available at this moment. The maximum magnitude of the reference current is limited to 80 μA. Using $\mu_p = 265\ cm^2/Vs$, $\mu_n = 785\ cm^2/Vs$, $C_{oxp} = 3.6*10^{-4}\ F/m^2$ and $C_{oxn} = 8*10^{-4}\ F/m^2$, and equations (5) and (6), the values for $(W/L)_p$ and $(W/L)_n$ are found to be 5 and 2 respectively. We choose a channel length of 6 μm, thus $(W/L)_p = 30\mu m / 6\mu m$ and $(W/L)_n = 12\mu m / 6\mu m$.

The complete schematic of the current comparator is shown in figure 15. Instead of using two input-protection diodes to limit the input voltage swing, an input stage based on the first generation current conveyor [5] is used to provide a low input impedance for the input current source. A description of the operation of the input stage can be found in [9].

The simulated output voltage of the current comparator shown in figure 15 is shown in figure 16. The reference current is 2 μA. When the input-current-step size is 5 μA, the response time of the current comparator is shorter than 400 ns. However, the response time is increase to longer than 800 ns when the input-current-step size is reduced to 3 μA.

The layout of the current comparator is shown in figure 17. Experimental results showing the transfer characteristic and the response time of the current comparator can be found in figures 18 to 20. As shown in these figures, the experimental results are consistent with those of the simulated ones.

Conclusion

A CMOS current comparator with well-controlled hysteresis has been reported. The threshold currents of the CMOS current comparator are controlled by a reference current and are independent of the parameters of the MOSFETs used. Unlike the CMOS current comparator reported elsewhere [7, 8], the CMOS current comparator reported here allows bidirectional-input current.

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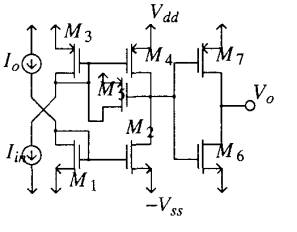

Figure 1: A CMOS current comparator with hysteresis

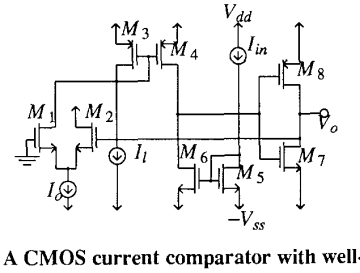

Figure 2: A CMOS current comparator with well-controlled hysteresis

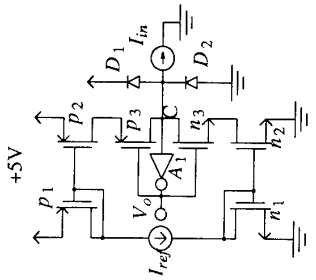

Figure 3: A novel CMOS current comparator with bidirectional-input current

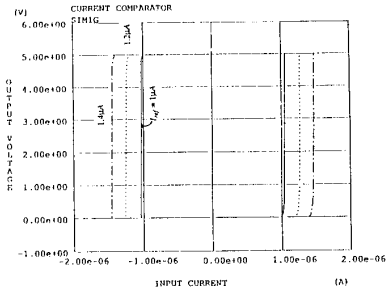

Figure 4: The transfer characteristic of the CMOS current comparator shown in figure 3

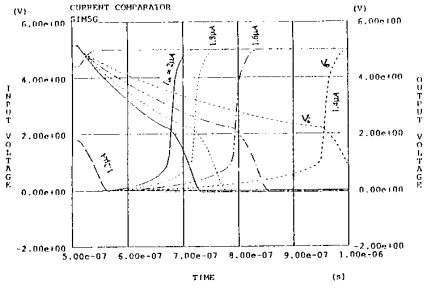

Figure 5: The transient response of the current comparator shown in figure 3

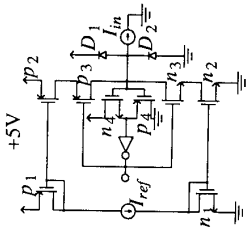

Figure 6: The incorporation of a buffer into the current comparator.

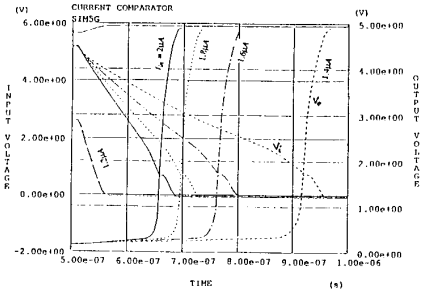

Figure 7: The transient response of the current comparator shown in figure 6

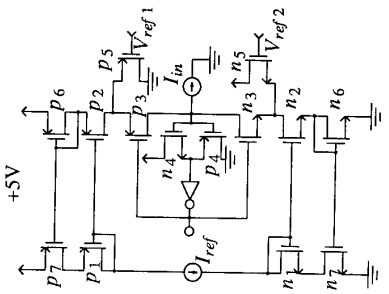

Figure 8: The current comparator after incorporating the current steering technique.

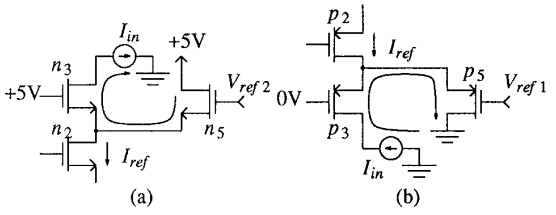

Figure 9: MOSFETs (a) n_5 and (b) p_5 functioning as input protection diodes.

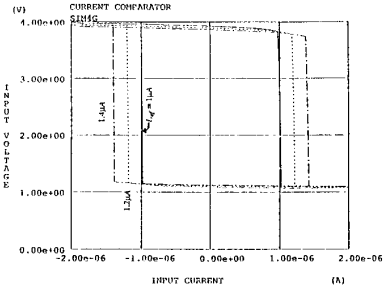

Figure 10: The input voltage of the current comparator shown in figure 8 as a function of the input current.

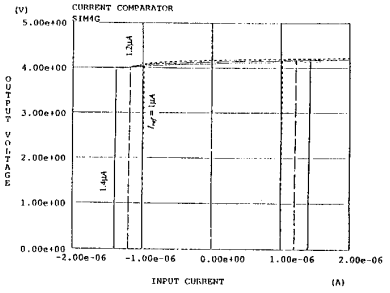

Figure 11: The transfer characteristic of the current comparator shown in figure 8.

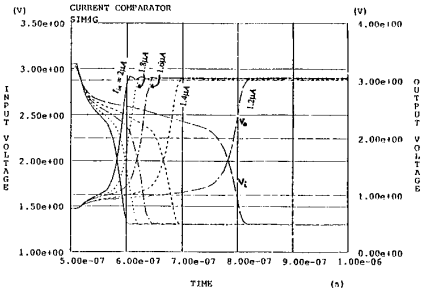

Figure 12: The transient response of the current comparator shown in figure 8

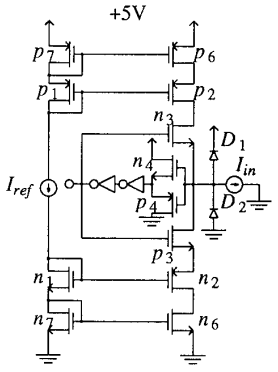

Figure 13: A current comparator with sharp and well defined output-voltage-transition edge.

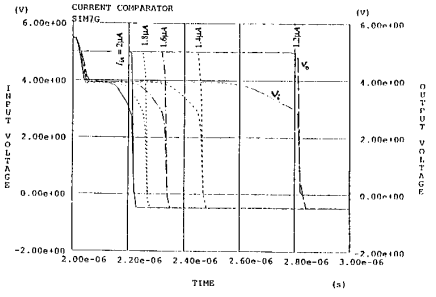

Figure 14: The transient response of the current comparator shown in figure 13.

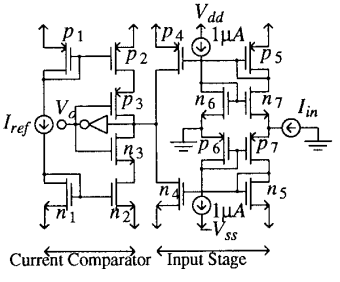

Figure 15: The complete schematic of the current comparator implemented on silicon.

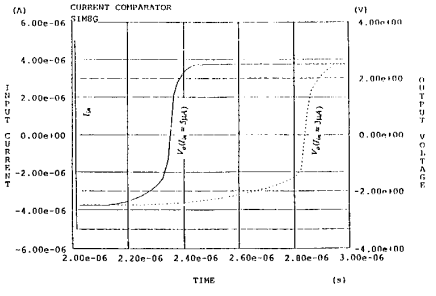

Figure 16: The transient response of the current comparator shown in figure 15

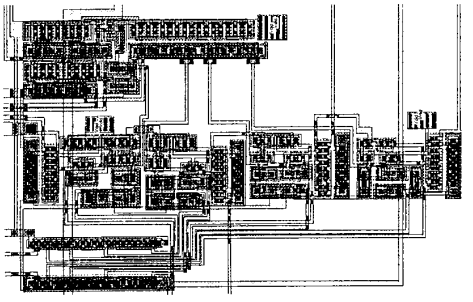

Figure 17: The layout of the current comparator.

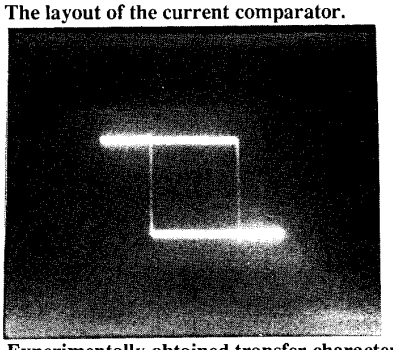

Figure 18: Experimentally obtained transfer characteristic of the current comparator. (Vertical scale: 2V/div, horizontal scale: 2μA/div)

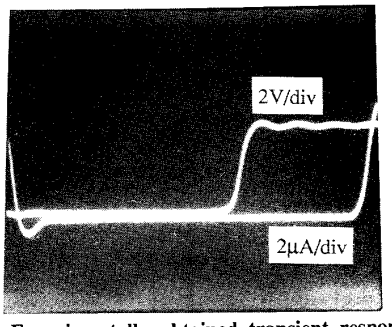

Figure 19: Experimentally obtained transient response of the current comparator. The input-current-step size is 3 μA. (Horizontal scale: 0.1μs/div)

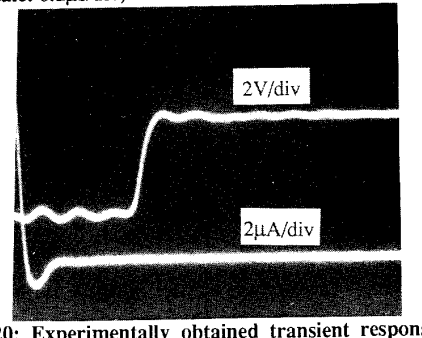

Figure 20: Experimentally obtained transient response of the current comparator. The input-current-step size is 5 μA. (Horizontal scale: 0.1μs/div)