# LATCHED DIFFERENTIAL FET LOGIC

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## ABSTRACT

In this paper, we propose a new circuit topology for creating complex logic circuits in GaAs. Latched Differential FET Logic (LDFL) is a fully differential logic family that provides complex logic function capability, tolerance to threshold voltage variations and complementary, latched-function outputs. LDFL is capable of performing up to eleven levels of logic in one gate, while still giving excellent performance. LDFL also provides improved noise margins due to the use of bootstrapped loads and significantly reduces the load-to-logic ratioing constraint. A nine-level LDFL gate has a delay of 1.7ns and a static power dissipation of 4mW as demonstrated in simulations of 4-bit digital comparator circuits.

## INTRODUCTION

GaAs MESFET circuit technology provides a means of creating high-speed digital logic circuits. One common problem with standard GaAs logic families such as Buffered FET Logic (BFL), Direct-Coupled FET Logic (DCFL) and Schottky-Diode FET Logic (SDFL) is the inability to perform complex logic functions in a single gate. While dynamic Domino Logic [1] provides the ability to perform complex functions, designs are more critical and require complex clocking. As well, domino logic does not provide complementary output signals; hence it cannot be used to implement some logic functions such as comparators and XOR gates.

The differential FET logic style proposed here is motivated by CMOS CVSL [2] and is similar in principle to Enabled/disabled CMOS Differential Logic (ECDL) [3]. Latched Differential FET Logic (LDFL) is capable of implementing complex logic functions with a single differential tree network. Designs are stable and easy to margin. Since both polarities of the result are available, LDFL increases logic flexiblity without extra circuitry. As well, its differential logic style provides tolerance to threshold-voltage variations, which is crucial in current GaAs technologies. LDFL has applications in the area of high speed ALUs, iterative networks [3] and random combinational circuits. Simulations in a 1$\mu$m GaAs E/D process show LDFL is capable of supporting up to eleven series FETs in its logic trees [1]. The latched outputs are stable and have good noise margins.

The proposed LDFL circuit is described in detail in the following sections. Section II describes the topology and operation of DFL. Section III summarizes simulation results and, finally, section IV presents conclusions.

[1] This number is process dependent.

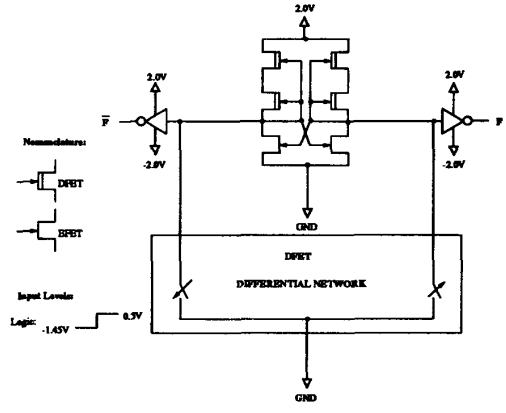


Figure 1. The LDFL Circuit Topology.

| Logic Level | Voltage |
|---|---|
| High | 0.3V |
| Low | -1.45V |

| Power Supply Levels | ±2.0V ground |
|---|---|

Table 1. LDFL Logic Levels and Power Supplies

## TOPOLOGY AND OPERATION

**Topology:**—The topology of a LDFL circuit is shown in figure 1. A gate consists of a differential logic tree that implements the desired function, a cross-coupled amplifier to amplify and latch the imbalance created by the logic tree, and two BFL inverters for buffering and level shifting.

The logic levels used externally in LDFL are shown in table 1. These levels were chosen so that DFETs may be used in the logic tree, and to provide a larger input noise margin. Internally, DCFL levels are used in the cross-coupled amplifier. LDFL requires the use of three power supplies as shown in table 1.

**Circuit Operation:**—An example of an LDFL circuit is shown in figure 2. The circuit operates by utilizing a differential imbalance created on the latch output nodes to flip the state of the DCFL cross-coupled latch. Thus in order to switch, one

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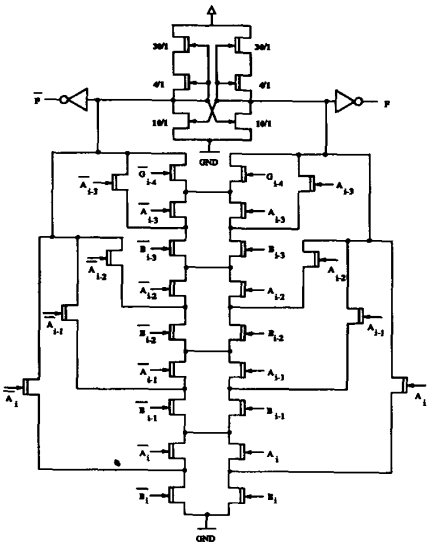

Figure 2. Four-bit comparator. Logic FETs have size 20/1.

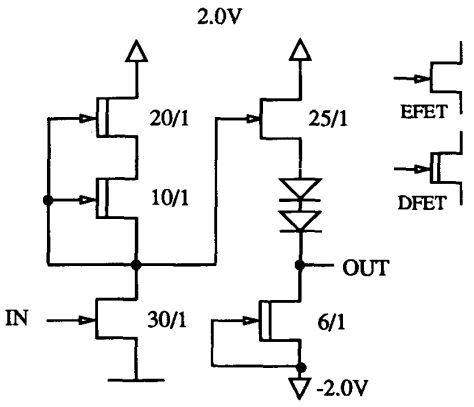


Figure 3. Bootstrapped Inverter.

side of the logic tree must pull the high side of the latch below its switching point. This point can be adjusted to suit the designer's preference for speed or noise margin. The cross-coupled latch provides positive feedback which helps to amplify the initial imbalance created by the logic tree. Once the cross-coupled latch has been set, the circuit is in a stable state, at its maximum noise margin. Modified BFL buffer inverters are used to isolate the cross-coupled latch from high load capacitance and noise. An EFET source follower was used for better follower characteristics. The buffers also give LDFL excellent load-driving capability. As well, the buffers are also used to boost the DCFL levels of the cross-coupled latch to DFET logic levels resulting in higher input noise margins. The BFL circuit used is shown in figure 3.

LDFL is a ratioed logic style, but the ratio constraint is relaxed by the use of the cross-coupled latch since the logic tree need only pull the latching node below its switching point. The gate may be ratioed by adjusting the pull-up load, with the switching point maintained by suitable adjustment of the latch pull-down FETs. This allows up to eleven FETs (or more depending on the technology) to be placed in series in the logic tree. Thus a large amount of logic may be performed by each gate.

**Bootstrapped loads:**—An analog bootstrapping technique is used to improve the switching characteristics of both the cross-coupled latch and the BFL inverters. An additional FET is placed above the load such that the gate-source voltage of this FET regulates the drain-source voltage of the load FET, thus boosting the output resistance of the load. The result is

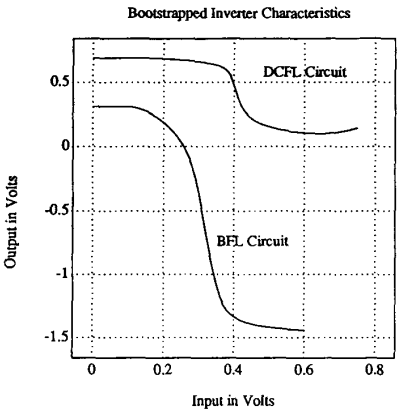


Figure 4. Bootstrapped Inverter Characteristics.

a sharper transfer characteristic of the resulting gate. This is shown in figure 4 for DCFL and BFL inverters.

## CIRCUIT PERFORMANCE

The performance of the Latched-DFL circuit was simulated using the HSPICE simulator and Triquint's [2]. 1$\mu$m QED process parameters, to characterize the new topology. A number of simulations were performed, under varying load conditions; in particular gate delay, rise and fall times were measured as

[2]Triquint Semiconductor, Beaverton, Oregon

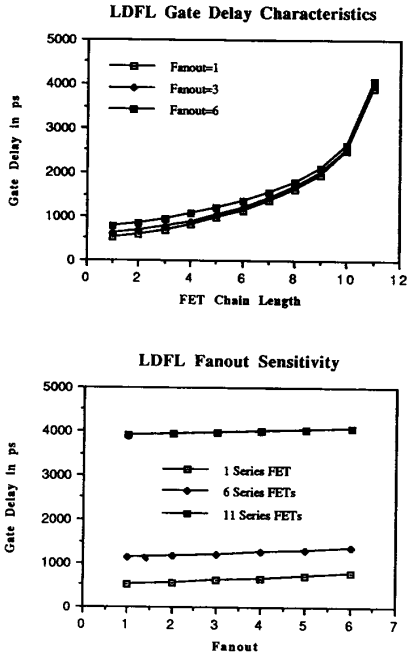


Figure 5. Gate Delay Characteristics.

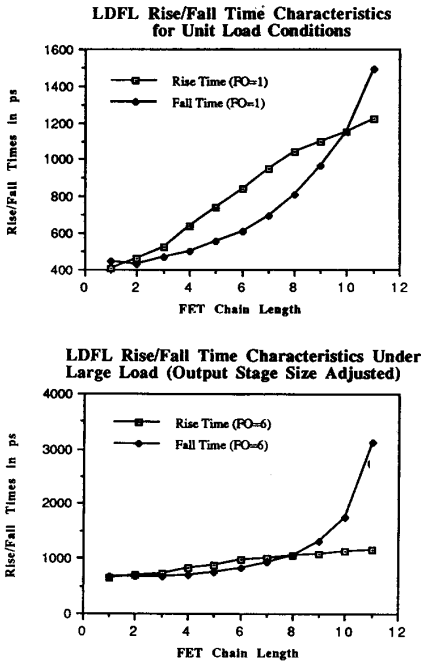


Figure 6. Rise/Fall Time Characteristics.

a function of the number of series-transistor levels. All measurements assume that the last input to switch is closest to the latching node as is common design practice [4]. Gate delays are an average of low-to-high and high-to-low propagation times as measured at 50% swing points.

The results of the characterization are shown in figures 5 and 6. Figure 5 shows excellent delay characteristics over a wide range (from one to nine) of series FET levels. A two-level gate has a delay of approximately 500 ps while a nine-level gate has delay of only 1.9ns. The curve is almost flat between these two points. Figure 5 also shows the excellent load-driving capability of LDFL. The difference in delay between 1 gate load and 6 is only 250ps. The fanout-sensitivity curve shows that fanout loading has little effect on the average gate delay. Figure 6 describes the effects of loading on the rise and fall times of LDFL gates. Both graphs show a similar skew between rise and fall times [3]. The skew reflects the different driving capabilities of the source- follower pull-up versus the diode-connected-current-source pulldown. Simulations show that this skew can be minimized by adjustment of the BFL-output-stage bias and emitter-follower sizing. These optimizations were not made in the gate delay simulations so that data would be consistent for comparison.

**4-bit Comparator:**—A 4-bit digital comparator circuit has also been simulated and has a nominal delay of 1.7ns with power dissipation of 4mW. Power dissipation is not out-of-line, considering the amount of logic being performed in the gate.

[3]It should be noted that the output stage size was increased for the large-load case only when measuring rise/fall performance.

**Noise Margins:**—Noise margins can be defined as they are in CMOS Domino circuits. As in [5], we define the external input noise margins ($V_{ENM}$) to be the voltages between the logic low/high level and the device threshold. The latching-node internal noise margin ($V_{INM}$) is that of the BFL buffer only, since the charge redistribution noted in [5] is not a problem. The noise margins were measured graphically and the results are shown below.

The advantage of the latched style embodied in LDFL is that the pull-down tree does not fight a load device, hence there is no *minimum* drive requirement during static operation. This means that the maximum possible external noise margins are available.

| | Noise Parameter | Value |
|---|---|---|
| External | $V_{ENM_l}$ | 750mV |
| | $V_{ENM_h}$ | 1050mV |
| Internal | $V_{INM_l}$ | 175mV |
| | $V_{INM_h}$ | 270mV |

Table 2. Summary of Critical Noise Margins

## CONCLUSIONS

A new GaAs static-logic family has been proposed. Latched Differential FET Logic (LDFL) is a differential logic family based on CMOS ECDL circuits [3]. The family provides tolerance to threshold variations, high-speed operation and excellent load-driving capability. LDFL has the ability to perform complex logic functions in a single gate and can support up to

eleven series transistors in the differential tree. True and complement function outputs are provided without extra circuitry, increasing logic flexibility and alleviating the inversion problem associated with CMOS Domino logic [6]. The outputs of the gate are latched and have good noise immunity. Noise margins may be traded for speed depending on the application. LDFL is a ratioed logic style but the ratio constraint is significantly reduced. LDFL circuits would be ideal for use in high speed ALU circuits, iterative networks and complex combinational circuit blocks. A 4-bit comparator was designed and simulated to demonstrate the use of LDFL.

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