On Improving the Linearity of DACs Using TIAMPs

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Abstract

Linearity of a D/A converter using TIAMPs is analyzed. Proof of the fact that DNL at the first-major carry is most sensitive to the gain error of the TIAMPs is given. Results of the linearity analysis lead to an optimum D/A converter configuration using non-identical cells. A new TIAMP design with low closed-loop-gain error is described. Experimental results show that accuracy of the TIAMP DAC, limited by channel mismatches of the TIAMPs, has been increased to 11 bits.

1. Introduction

Of all the voltage-mode D/A converters reported in the literature heretofore, a recently reported one using Three-Input AMPlifiers (TIAMPs) is most compatible with standard CMOS processes [1,2,3,4]. The TIAMP-D/A converter is very suitable for applications where multiple D/A converters are needed, or where the output of a D/A converter drives an on-chip internal node, making it very difficult to use externally-connected precise passive components to control the linearity and the accuracy of the D/A converter.

In this paper, we report up-to-date results of our research in achieving highly-linear-TIAMP-D/A converter designs.

2. Linearity analysis of the TIAMP DAC

Using R_v to denote the normalized output voltage (with respect to the reference voltage, V_{ref}) of the TIAMP DAC shown in Fig. 1, the step change in the (normalized) output voltage caused by the transition of two successive input digital values can be shown to be:

$$\Delta R_v = \frac{\gamma^{k-1}(1-\gamma)}{(1+\gamma)^k} + \frac{\gamma^N}{(1+\gamma)^N} \qquad (1)$$

where γ is the channel-gain ratio of the TIAMP, N is the total number of bits of the DAC and k is a parameter dependent on the major carries: For the first-major carry, $k = 1$ and so on.

By differentiating equation (1) with respect to γ and then setting $\gamma = 1$, it can be shown that $\delta \Delta R_v / \delta\gamma$ is largest at $k = 1$. Thus, the step size of the output voltage and equivalently, the DNL, at the first-major carry is most sensitive to the channel-gain ratio, γ.

Using an 8-bit TIAMP DAC as an example, a plot of the maximum channel-gain mismatch required to limit DNL to 0.5 LSB at major carries is shown in Fig. 2. This plot shows that the DNL at the first-major carry is most sensitive to γ and the DNL at the sixth major carry is least sensitive to γ.

The above analysis assumes all TIAMPs have equal channel-gain ratios. However, channel mismatches of all TIAMPs do not contribute equally to the DNL at the first-major carry. Highly-linear TIAMPs are slower and occupy larger area generally. By using highly-linear designs for the TIAMPs which contribute significantly to the DNL at the first-major carry, a highly-linear TIAMP D/A converter can be implemented without using excessively large silicon area.

Reconsider the TIAMP D/A converter shown in Fig. 1. If only the i^{th} stage has a channel mismatch, where the i^{th} stage is not associated with the MSB (i.e. $i \neq 1$), and all other stages are ideal, the DNL at the first-major carry can be shown to be:

$$DNL\,(k=1) = -\frac{1-\gamma}{1+\gamma} \qquad (2)$$

Equation (2) shows that all TIAMPs other than the one associated with the MSB contribute equally to the DNL at the first-major carry.

If only the TIAMP associated with the MSB has a channel mismatch and all other stages are ideal, the DNL at the first-major carry becomes

$$DNL\,(k=1) = \frac{1-\gamma}{1+\gamma}\left[2^N - 1\right] \qquad (3)$$

Comparing equations (2) and (3), we may conclude that the contribution of a channel mismatch of the TIAMP associated with the MSB is approximately 2^N times larger than that of the other TIAMPs. Thus, only the TIAMP associated with the MSB should be designed to have high linearity at the expense of larger area and slower speed of operation. Higher speed TIAMPs with larger closed-loop-gain errors can be used for the other stages.

3. The design of a high linearity TIAMP

The earlier work by C.A. Lader et al at U.C. Berkeley [5] on the 3μm-CMOS analog standard-cell library, inspired us to design the new linear TIAMP shown in Fig. 3. Compared to earlier designs, the TIAMP shown in Fig. 3 has the advantage of a very small systematic output-offset

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voltage (in μV). The systematic output-offset voltage is reduced by the negative feedback loop formed by n_{17}, n_{18}, p_3, p_4 and p_6. Frequency compensation is done by two grounded capacitors, C_c and C_L. Since neither C_c nor C_L have any effect on the linearity or gain of the TIAMP in a closed-loop configuration, they can be implemented using relatively nonlinear capacitors formed by the gate and the channel of an n-MOSFET. This makes the TIAMP completely compatible with the standard digital CMOS process.

High linearity of the TIAMP is achieved by having symmetrical signal paths for both channels, and by using large size MOSFETs for n_1 to n_4. The simulated closed-loop-gain error of the TIAMP is shown in Fig. 4. Note that by increasing the size of n_1 to n_4 while keeping their aspect ratio constant, the closed-loop-gain error can be reduced. However, the associated increase in the input capacitance leads to slower operation.

Fig. 5 shows a 2-bit TIAMP D/A converter. Increasing the size of the input MOSFETs of $TIAMP_1$, has the effect of reducing the glitches in the output voltage due to skew in the input data. For example, when an input MOSFET of size $W/L = 6\,\mu m / 24\,\mu m$ is used for both $TIAMP_2$ and $TIAMP_1$, the output waveforms of the 2-bit D/A converter for different relative delays of the two bit signals appear as shown in Fig. 6. When the input MOSFET size of $TIAMP_1$ is increased to 48 μm / 196 μm, significant reduction of the glitches in the output voltage, shown in Fig. 7, is observed.

4. Implementation and experimental results

6-bit and 12-bit D/A converters have been implemented using a 3μ-CMOS process. The size of the input MOSFETs of all TIAMPs is 24 μm / 96 μm. The improved D/A converter using non-identical cells is currently being laid out and no experimental results are yet available. In the improved design, the input MOSFETs of the first TIAMP are increased in size to 48 μm / 192 μm.

The micrograph of the 6-bit and 12-bit D/A converters is shown in Fig. 8. The area of each TIAMP is 0.15 mm^2 and the total area including the pads is 10.12 mm^2.

The linearity plot of the 6-bit D/A converter is shown in Fig. 9. The maximum *DNL* of the 6-bit D/A converter is approximately 7% of the least-significant-bit voltage.

For the 12-bit D/A converter, the digital noise coupled through the power-supply rails becomes significant. It was experimentally found that the digital noise present at the output of the 12-bit D/A converter is 1 mV.

When the 12-bit D/A converter is configured to have 9 bits only, the output waveform for the first-major carry is shown in Fig. 10(a). For comparison, Fig. 10(b) is the LSB voltage. Without considering the digital noise present in the output voltage, the *DNL* at the first major carry is 18% LSB. After taking into consideration the 1 mV digital noise present in the output voltage, the *DNL* at the first-major carry increases to 29% LSB.

After taking the switching noise into account, the *DNL* of the 10-bit and the 11-bit configurations are 50% and 100% LSB respectively. The 12-bit configuration has a *DNL* greater than 100% LSB.

The characteristics of the DACs reported here are summarized in Table 1.

5. Conclusions

The TIAMP D/A converter is the only voltage-mode D/A converter reported in the literature that is fully compatible with the standard CMOS process. The accuracy of this type of D/A converter has now been improved to over 10 bits. This is done by using a better TIAMP design and larger input-MOSFET size. Future high-linearity TIAMP D/A-converter designs should use non-identical cells to improve accuracy without increasing the area excessively, and should incorporate techniques that reduce digital-noise interference.

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References

[1] Chong, C.P., Smith, K.C. and Vranesic, Z.G.: "Using active components to perform voltage division in digital-to-analog conversion," in Proceedings of 1988 Symposium on VLSI Circuits, Tokyo, Japan, pp. 119-120.

[2] Chong, C.P.: "A/D and D/A converters using no precise or well-matched passive components," M.A.Sc. Thesis, Department of Electrical Engineering, University of Toronto, January 1988.

[3] Chong, C.P., Smith, K.C. and Vranesic, Z.G.: "Using active components to perform voltage division in digital-to-analog conversion," IEEE J. Solid-State Circuits, Vol. SC-24, pp. 999-1002, Aug. 1989.

[4] Chong, C.P., Smith, K.C. and Vranesic, Z.G.: "Three-input amplifiers," in Proceedings of 1990 ISCAS, New Orleans, Louisiana, pp. 3217-3220.

[5] C.A. Lader, C.F. Rahim, S.F. Dreyer, G.T. Uehara, P.T. Kwok and P.R. Gray: "Design considerations for a high-performance 3-μm CMOS analog standard-cell library," IEEE J. Solid-State Circuits, Vol. SC-22, pp. 181-189, April 1987.

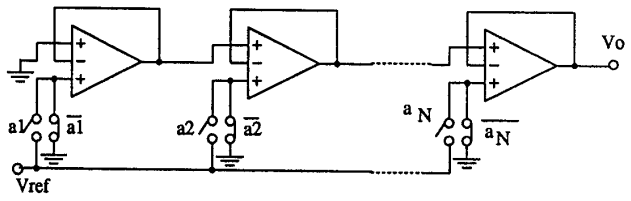

Fig. 1: The D/A converter using TIAMPs.

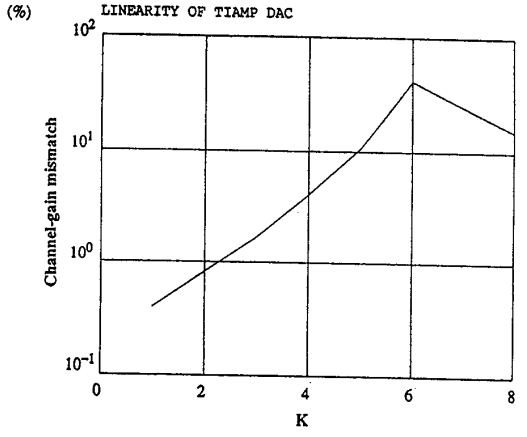

Fig. 2: The maximum channel-gain mismatch required to limit DNL to 0.5 LSB at major carries.

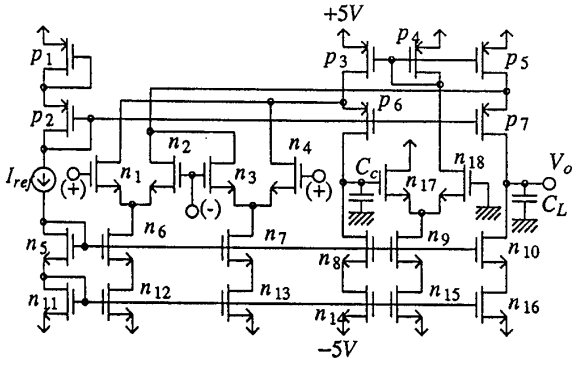

Fig. 3: The schematic of the highly-linear TIAMP.

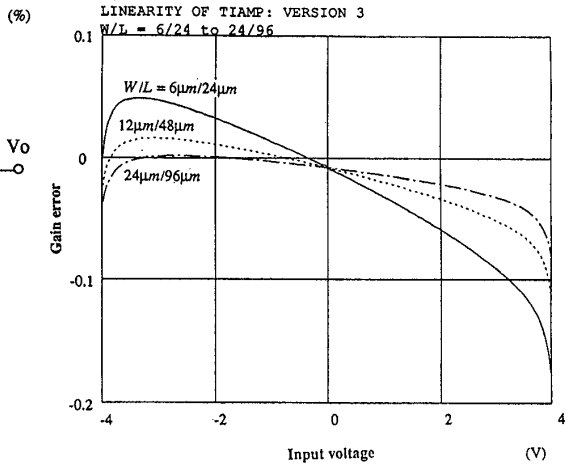

Fig. 4: The closed-loop-gain error of the TIAMPs using input MOSFET sizes of 6 μm / 24 μm, 12 μm / 48 μm and 24 μm / 96 μm.

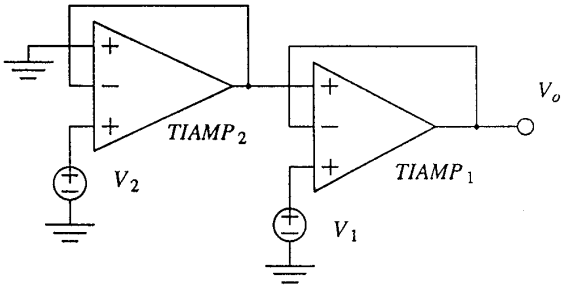

Fig. 5: The 2-bit TIAMP D/A converter.

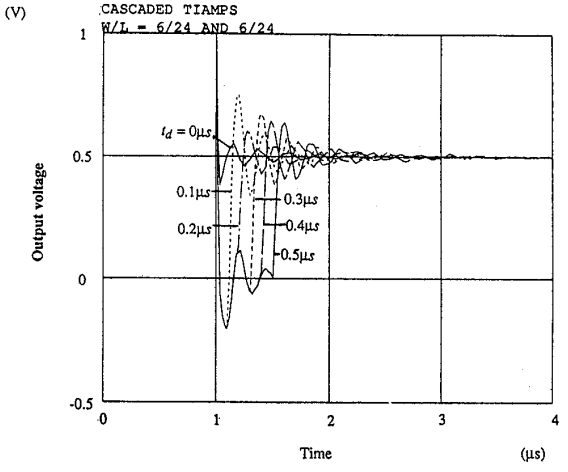

Fig. 6: The output waveforms of the 2-bit DAC with input digits delayed by t_d. The input MOSFET sizes are 6 μm / 24 μm for both $TIAMP_1$ and $TIAMP_2$.

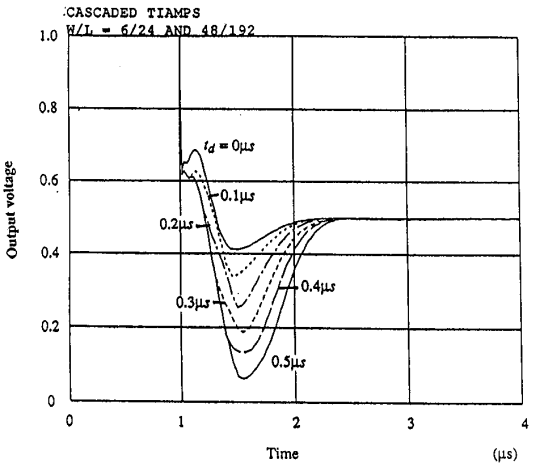

Fig. 7: The output waveforms of the 2-bit DAC with input digits delayed by t_d. The input MOSFET sizes are 6 μm / 24 μm and 48 μm / 192 μm for $TIAMP_1$ and $TIAMP_2$ respectively.

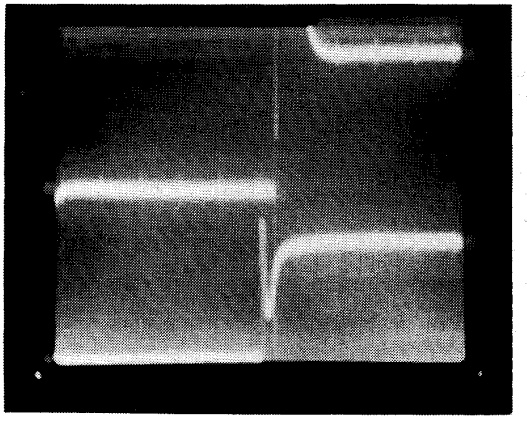

Fig. 10: The output waveforms of the first-major carry (top) and the least-significant-bit voltages (bottom) of the 9-bit configuration. The vertical scale is 2mV/div and the horizontal scale is 20μs/div. The overshoot of the top waveform extends to 50mV.

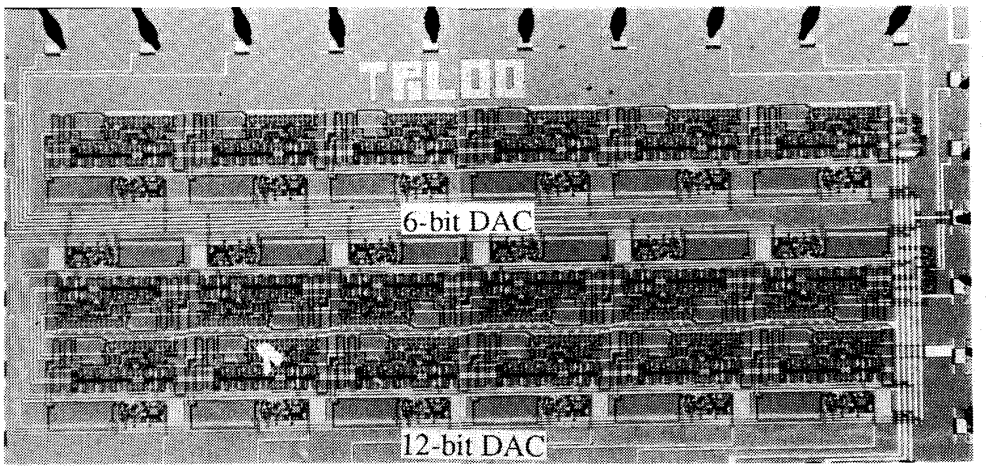

Fig. 8: The micrograph of the 6-bit and 12-bit D/A converters.

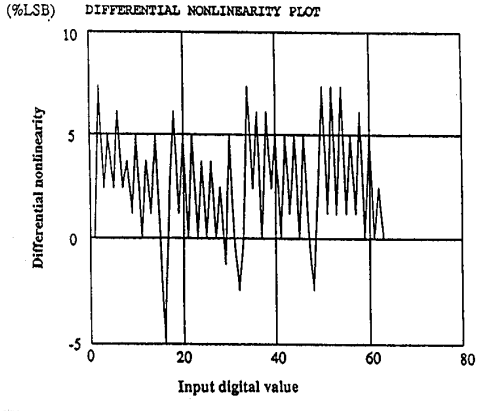

Fig. 9: The DNL of the 6-bit TIAMP D/A converter.

Area	0.15 mm^2 / TIAMP
Accuracy	11 bits
Output swing	3 V (peak-to-peak)
Power supply	± 5V
Sampling rate	50 kHz (11-bit accuracy)
Static power diss.	3mW / TIAMP
Technology	3μ-CMOS

Table 1: A summary of the characteristic of the TIAMP DACs.