

On the Use of Multiple-Valued Switch-Level Algebra to Analyze Binary MOS Bridge Circuits and Dynamic Circuits

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ABSTRACT

This paper presents two new results for multiple-valued switch-level algebra (MSA for short). The first is the use of MSA to describe the bidirectional switching function of MOS transistors and, thereby, to analyze binary MOS bridge circuits. The second is the use of MSA to describe the function of capacitors and, thereby, to analyze binary MOS dynamic circuits. The results presented in this paper greatly widen the application area of MSA.

I. INTRODUCTION

Multiple-valued switch-level algebra (MSA for short) is an algebra with the capacity of modeling binary MOS circuits at the switch-level [1]. It has been used in the analysis and design of MOS static circuits and pass-transistor networks [1, 2, 3].

One of the features of MSA is that it provides a means to transform a MOS circuit into a Boolean expression. That is, MSA can be used as a verification tool for VLSI design. To ensure the completeness of this process, it is necessary to include a bidirectional-switch model and a capacitor model in MSA. For this purpose, some new results for MSA are presented in this paper. The main contents of this paper are: (1) the use of MSA to describe the bidirectional switching function of MOS transistors and a procedure to analyze binary MOS bridge circuits; (2) the use of MSA to describe the function of capacitors and a procedure to analyze binary MOS dynamic circuits.

The results presented in this paper show that MSA has the capability of analyzing a very wide variety of MOS circuits, and thereby provides a powerful tool for the design of MOS-based systems.

II. DESCRIPTION OF THE BIDIRECTIONAL SWITCHING FUNCTION OF MOS TRANSISTORS AND THE ANALYSIS OF BRIDGE CIRCUITS

This Section presents the use of MSA to describe the bidirectional switching function of a MOS transistor. Using the techniques developed here, MSA can be used to analyze bridge circuits.

In [1], a positive switch operation $*$ and a negative switch operation $\bar{*}$ are used to describe the function of an NMOS transistor and a PMOS transistor respectively. For example, for the NMOS transistor shown in Fig. 1, if A is the

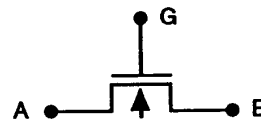


Figure 1. An NMOS-Transistor Switch

source, B the drain, and G the gate, the function can be described as follows

$$B = A * G . \quad (1)$$

For a PMOS transistor, the function can be described as follows

$$B = A \bar{*} G . \quad (2)$$

In real circuits, however, a MOS transistor is a bidirectional switch. In other words, its source and drain are interchangeable.

To describe the bidirectional switching function of MOS transistors, some switch-level models [4, 5] view a MOS transistor as a controlled connector. Using MSA, this idea can be described as follows: For an NMOS transistor,

such as the one shown in Fig. 1, if gate G takes the value H (a high voltage), A and B are connected, with the result notated as $A \# B$; if gate G takes the value L (a low voltage), A and B are disconnected, and the effect of the MOS transistor is that A and B are isolated, with B taking the value Z (high impedance state).

However, a simpler methodology is also available: For an NMOS transistor, instead of using Eq.(1), the following equations can be used.

$$\begin{cases} A = B * G \\ B = A * G \end{cases} \quad (3)$$

In the same way, for a PMOS transistor, we have the following relations:

$$\begin{cases} A = B \bar{*} G \\ B = A \bar{*} G \end{cases} \quad (4)$$

Using this simple idea in the description of a circuit, it is not necessary to distinguish unidirectional switches from bidirectional switches. To describe a MOS circuit completely, one need only list switch-level equations for all nodes in the circuit, thereby producing a set of coupled node-equations.

EXAMPLE 1. Use MSA to describe the MOS bridge circuit shown in Fig. 2.

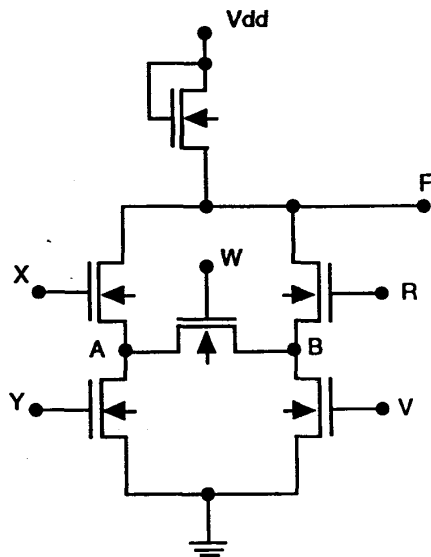


Figure 2. An MOS Bridge Circuit

Solution: The circuit shown in Fig. 2 is an NMOS circuit, so that Eq. (3) can be used to describe it. List equations for nodes F , A , and B . Obtain coupled node-equations for the circuits as follows:

$$\begin{cases} F = \tilde{H} \# A * X \# B * R \\ A = L * Y \# B * W \# F * X \\ B = L * V \# A * W \# F * R \end{cases},$$

where \tilde{H} represents the resistive load connection to the high level and L represents the low level directly.

In this way, the analysis of a MOS circuit is transformed into the process of solving the coupled node-equations of the circuit. A detailed discussion of this process can be found in [6]. The following is a brief introduction:

The procedure for solving the coupled node-equations of a circuit is as follows.

1. Apply the # to * distribution law [1] for node-equations:

Law 1: The # to * distribution law can be expressed as

$$(A \# B) * G = A * G \# B * G$$

2. Apply the connecting-term absorption theorem [6] to simplify node-equations:

Theorem 1: Connecting-term absorption theorem.

If a node signal appears on the right side of its own node equation but not following a * operator, the term containing this node signal can be eliminated.

Thus, equation

$$A = S \# A * C_1 * C_2 * \dots * C_n$$

can be simplified to the form

$$A = S.$$

3. Use substitution to solve the coupled node-equations and to obtain switch-level expressions (S -expressions for short).

4. Use the following rules [1] to simplify the S -expressions.

Rule 1:

$$(A * X_1) * X_2 = A * (X_1 \cdot X_2).$$

Rule 2:

$$A * X_1 \# A * X_2 = A * (X_1 + X_2).$$

5. Use the following rules [1] to transform the S -expressions into Boolean expressions (B -expressions for short).

Rule 3:

For an NMOS circuit, if its S -expression is

$$F_s = L * A \# \bar{H}$$

the B -expression for this circuit will be

$$F_b = \bar{A}$$

Rule 4:

For a CMOS circuit, if its S -expression is

$$F_s = H * A \# L * \bar{A}$$

the B -expression for this circuit will be

$$F_b = A .$$

EXAMPLE 2. Solve the coupled node-equations obtained in Example 1.

Solution: The coupled node-equations obtained in Example 1 are as follows:

$$\begin{cases} F = \bar{H} \# A * X \# B * R \\ A = L * Y \# B * W \# F * X \\ B = L * V \# A * W \# F * R . \end{cases}$$

Using substitution, obtain the following equations:

$$\begin{cases} F = \bar{H} \# A * X \# B * R \\ A = L * Y \# (L * V \# A * W \# F * R) * W \# F * X \\ B = L * V \# (L * Y \# B * W \# F * X) * W \# F * R . \end{cases}$$

Using Law 1 and Theorem 1, we have

$$\begin{cases} F = \bar{H} \# A * X \# B * R \\ A = L * Y \# L * V * W \# F * R * W \# F * X \\ B = L * V \# L * Y * W \# F * X * W \# F * R . \end{cases}$$

Substituting equations for A and B for the values of A and B in the equation for F , we can obtain

$$\begin{aligned} F = \bar{H} \# (L * Y \# L * V * W \# F * R * W \# F * X) \\ * X \# (L * V \# L * Y * W \# F * X \\ * W \# F * R) * R \end{aligned}$$

Using Law 1 and Theorem 1, we get

$$\begin{aligned} F = \bar{H} \# L * Y * X \# L * V * W * X \\ \# L * V * R \# L * Y * W * R \end{aligned}$$

Using Rule 1 and Rule 2, we get a simplified S -expression as follows:

$$F = \bar{H} \# L * [(Y + V * W) * X + (V + Y * W) * R]$$

Using Rule 3, we can transform the S -expression for F into a B -expression for F as follows:

$$F_b = \overline{(Y + V * W) * X + (V + Y * W) * R} .$$

Although for the purpose of illustrations, the circuit explored in Examples 1 and 2 is very simple, the model and procedure proposed in this section can be used to solve any complex bridge circuit.

III. DESCRIPTION OF CAPACITORS AND ANALYSIS OF DYNAMIC CIRCUITS

Capacitors are not negligible in the analysis of MOS dynamic circuits, neither in the time analysis of circuits, nor in the fault analysis of circuits.

In switch-level models, there are traditionally two different ways to model capacitors. One method is to introduce an explicit digital charge-storage element, such as the "well" in CSA theory [5]. The other is to imply the function of capacitors in the charge storage state of the circuit, such as in LOGIS [7] and MOSSIM [8]. Both methods have the disadvantage of involving a complex and time-consuming computation for circuit states. Our method is to view signals stored in capacitors as dynamic signals with weak current-driven capabilities [9] and to build S -expressions for these signals.

We will limit our discussion to circuits having capacitors all of the same size. For a discussion of the approach to be used with capacitors of different sizes, refer to reference [10].

Fig. 3 depicts a capacitor to be described by MSA.

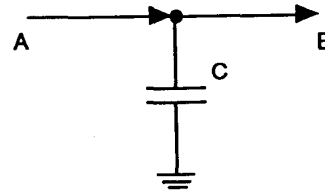


Figure 3. A Node Capacitor

In Fig.3, A is a signal loaded by a capacitor and forced to charge or discharge it. C is a signal stored on the capacitor. B is the output signal provided by the capacitor.

The signal stored on a capacitor will have the lowest current-drive capability except that provided by signal Z (high impedance state). If there are m level attenuators (representing resistors with m different values of resistance)

in a circuit, the logic strength of the signal stored on a capacitor will be at the $(m+1)$ value, that is, the weakest value in the circuit.

Suppose that before the time t_n , signal A is stable at a state denoted A_{n-1} , and that signal C is stable at a state denoted C_{n-1} . Signal B can then be expressed as

$$B_{n-1} = A_{n-1} \# C_{n-1}$$

If at time t_n , signal A changes to A_n , signal C will keep the value C_{n-1} for the instant because the signal of a capacitor cannot change suddenly. Subsequently, the capacitor will charge (or discharge) to a higher (or lower) voltage. Assume that at time t_{n+} , charging (or discharging) is complete, and signal C becomes C_n . C_n can be expressed as

$$C_n = A_n \# C_{n-1} \quad (5)$$

where \mathcal{N}_{m+1} indicates an $(m+1)$ -value attenuation operation whose function is to place the logic strength of C_n at the $(m+1)$ value, as the logic strength of the signal stored on a capacitor should be. Signal B is

$$B_n = A_n \# C_n$$

Eq. (5) can be used both in the time analysis and the fault analysis of any circuit. As well, it can be used to analyze MOS dynamic circuits. The following is an example of its use with dynamic MOS.

EXAMPLE 3. Analyze the two-phase dynamic inverter circuit [11] shown in Fig. 4.

Solution: Use MSA to list node-equations for all nodes of the first inverter (at the left). Note (1) that all MOS transistors in the circuit are NMOS; (2) that no attenuator exists in the inverter itself, so that in Eq. (5), value $m = 0$; (3) that capacitors C_1 and C_2 are very important in the analysis of the circuit.

The coupled node-equations for node E and node B of the first inverter are:

$$\begin{cases} E_n = A * \Phi_{1n} \# E_{n-1} \\ B_n = \Phi_{1n} * \Phi_{1n} \# \Phi_{1n} * E_n \# B_{n-1} \end{cases}$$

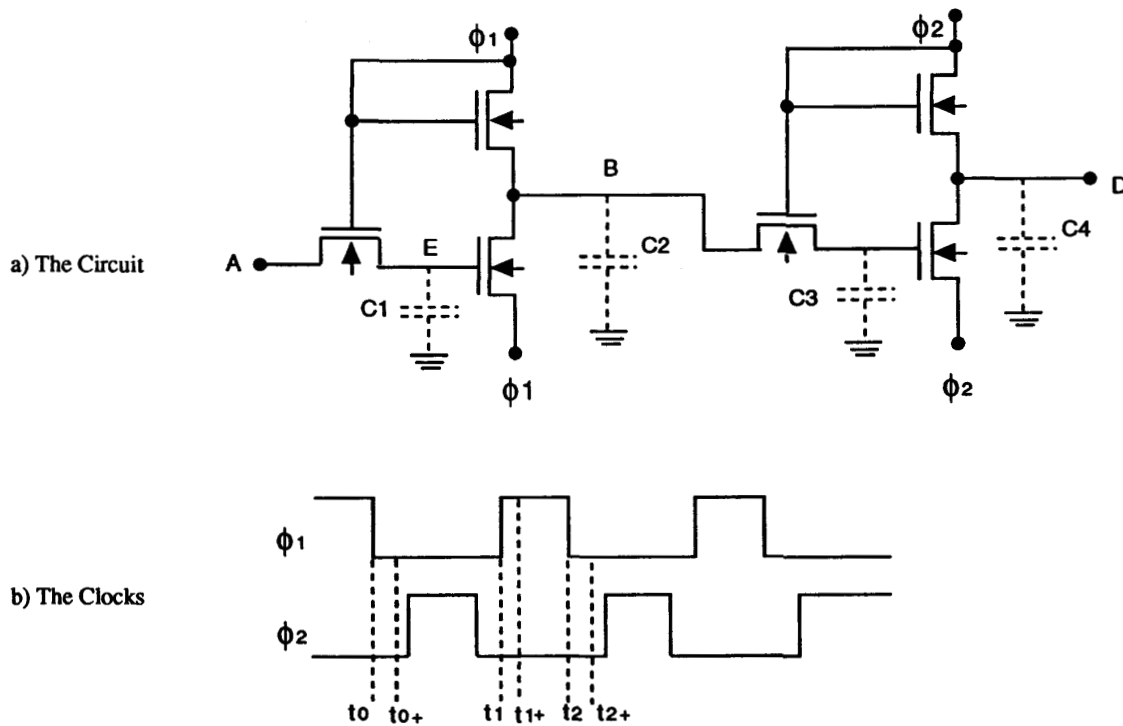


Figure 4. Two-Phase Dynamic Inverters

According to the timing diagram presented in Fig. 4(b), analyze the coupled node-equations above as follows.

When $t = t_0$, $\Phi_{10} = L$, and the original values of C_1 and C_2 are unknown (denoted \tilde{U}), so at $t = t_{0+}$, we have

$$E_0 = A * L \# \tilde{U} = \tilde{U}$$

$$B_0 = \tilde{L} * L \# L * \tilde{U} \# \tilde{U} = \tilde{U}$$

when $t = t_1$, $\Phi_{10} = H$, so at $t = t_{1+}$, we have:

$$E_1 = \tilde{A} * H \# \tilde{U} = \tilde{A}$$

$$B_1 = H * H \# H * \tilde{A} \# \tilde{U} = \tilde{H}$$

when $t = t_2$, $\Phi_{12} = L$, so at $t = t_{2+}$, we have:

$$E_2 = \tilde{A} * L \# \tilde{A} = \tilde{A}$$

$$B_2 = \tilde{L} * L \# L * \tilde{A} \# \tilde{H} = L * \tilde{A} \# \tilde{H}$$

According to Rule 3, the S -expression for B_2 is equivalent to the following B -expression:

$$B = \tilde{A}.$$

In summary, if at t_1 signal A is stable, at t_{2+} signal B is the inversion of signal A .

The same analysis can be done for the second inverter.

IV. CONCLUSIONS

Two new results for MSA are given in this paper. They are (1) a method to describe the bidirectional switching function of MOS transistors and a procedure to analyze binary MOS bridge circuits; (2) a model to describe the charge-storage function of capacitors and the corresponding analysis of binary MOS dynamic circuits.

These new results extend the application of MSA from the design and analysis of standard MOS gates to the design and analysis of MOS bridge circuits, and from the design and analysis of MOS static circuits to the design and analysis

of MOS dynamic circuits. Furthermore, the switch-level model of capacitors presented in this paper can also be used to solve the timing-analysis problem, the charge-sharing problem, and the fault-analysis problem in MOS circuits. As well, if additional logic values (such as M representing the middle level in a ternary circuit) are introduced, it is possible to extend MSA to the analysis and design of multiple-valued circuits.

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VI. ACKNOWLEDGEMENTS

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