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USING ACTIVE COMPONENTS TO PERFORM VOLTAGE DIVISION IN DIGITAL-TO-ANALOG CONVERSION

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The need for special processing steps for implementation of passive components on a VLSI chip has been a major stumbling block in integration of analog and digital circuits on the same chip. For example, the need for double polysilicon layers in implementing high-quality capacitors makes integration of switched-capacitor circuits with digital circuits, which do not require double polysilicon and usually occupy the largest area on a silicon chip, not ideally cost-effective. Thus, it is most desirable to develop techniques that allow implementation of analog circuits without using precise, well-matched or highly-linear passive components. This paper address this issue within the realm of D/A converters.

All the voltage-mode D/A converters reported in the literature thus far use passive components to perform voltage division. In this paper, we describe a D/A conversion technique which eliminate the need for using passive components to perform voltage division. The resultant D/A converters have voltage-mode output and require a voltage reference which can be implemented on the chip [1]. Any process designed for digital circuits may be used to implement the proposed D/A converter with a reasonable degree of accuracy.

The new D/A converter is based on cascading a number of voltage summers which have a gain of one-half as shown in figure 1. While it is clearly possible to implement such a scheme using conventional opamps, such an implementation would require the use of a large number of well-matched resistors. These resistors may be implemented using polysilicon (or nickel-chrome alloy if extra processing steps are used), which have low resistance and put additional drive requirements on the opamps. A more feasible approach is to use the three-input amplifier shown in figure 2 [2].

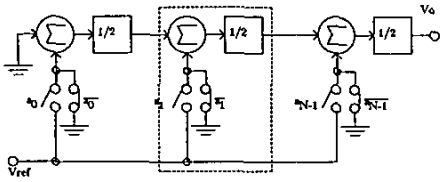

Fig. 1: D/A converter using voltage summers

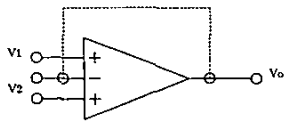

Fig. 2: The three-input amplifier

When the simple feedback connection shown is established, the output voltage of the three-input amplifier is the average of two input voltages, V_1 and V_2 [2]. When compared to similar circuits implemented using conventional opamp, the closed-loop-gain error of the three-input amplifier is at least two times less sensitive to the open-loop gain [2]. This allows the use of less complex circuits which occupies less area on silicon chip. Moreover, the closed-loop 3dB-bandwidth is twice that of the open-loop unity-gain bandwidth [2]. (In all opamp circuits, closed-loop 3dB-bandwidth never exceeds the unity-gain frequency of the opamp.)

The three-input amplifier may be realized as shown in figure 3. To accommodate the large input voltage swing inherent in its operation, the biasing gate-source voltages of the differential pairs must be large. This requires the use of MOSFETs having a small width-to-length ratio. The use of large gate-source biasing voltage improves the matching of transistors [3]. By splitting the connection between the gates of P_2 and P_3 to form two additional input terminals, a four-input amplifier known as "Differential difference amplifier" has been proposed independently elsewhere [4].

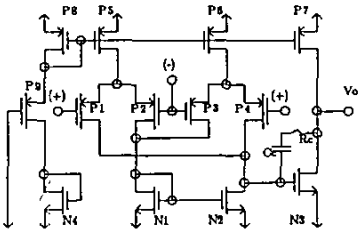

Fig. 3: A three-input amplifier implementation

Analysis, which is too lengthy to be shown here [2], indicates that (i) any mismatch in P_1 to P_4 results in nonlinearity (rather than non-zero offset voltage), (*ii*) a small mismatch in N_1 and N_2 causes negligible nonlinearity, (*iii*) any small mismatch in the tail-end biasing current will only lead to non-zero output offset voltage (on the assumption that output impedance of P_5 and P_6 are infinite) and (*iv*) any mismatch in threshold voltages due to body effect does not lead to undesirable effect, provided that the intrinsic threshold voltages of the MOSFETs are equal. However, if the body-effect parameter is too large, nonlinearity due to a degradation of the output impedances of P_5 and P_6 caused by excessively large gate-source voltage of P_1 to P_4 may occur. While the linearity of the three-input amplifier is not as good as that of the operational amplifier, due to the presence of negative feedback it is better than that of the open-loop differential pair used in the implementation of MOSFET-C filter. Using the setup shown in figure 4, the total harmonic distortion of the three-input amplifier in closed-loop configuration has been measured to be less than 0.02% for input frequencies over a range of 1 kHz to 30 kHz [5]. This figure compares favorably with that of the open-loop differential pair, which is from 0.5% to 0.7% for a channel length of 3 μm and t_{ox} values of 14 nm to 40.5 nm [6].

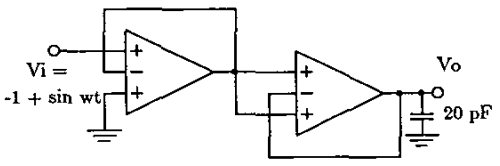

Fig. 4: The setup for measurement of THD

Taking second-order effects into consideration [7], it can be shown that reducing the biasing currents of the differential pairs leads to transfer curves that are more linear around the origin. However, large biasing currents produce transfer curves that are more linear at the upper end (lower end) if N-type transistors (P-type transistors) are used to implement the differential pairs [5]. The latter fact allows optimization of the closed-loop-gain errors [1] to produce a D/A converter that is more linear, because in most cases the largest differential-linearity error of a D/A converter occurs at the first major carry.

The only passive components used in the three-input amplifier are for the purpose of frequency compensation. Thus they can be implemented using polysilicon and P-well (for capacitor) and a MOSFET biased to be in the triode region (for resistor). While the matching of active components is still needed, transistor size may be chosen to minimize mismatches due to process gradients and edge variation, and to improve the percentage yield [3].

The differential nonlinearity of the D/A converter at the first major carry, (011...1, 100...0), can be expressed as

$$DNL = k^{1-N} - \left\{ k^{2-N} + k^{3-N} + \cdots + k^{-1} + 2 \right\} \qquad (1)$$

where k is the closed-loop gain of the three-input amplifier.

For both input codes 011...1 and 100...0, input voltages for all three-input amplifiers are either zero or very close to the reference voltage. Thus to minimize the DNL at the first major carry, the three-input amplifier should be optimized to have very small closed-loop-gain errors for large input voltages. This requires large biasing current and leads to large closed-loop-gain errors for small input voltages. (As a result of the large gate-source biasing voltages of P_1 to P_4, cascode structure for the biasing current source are not used.) The closed-loop-gain errors for small input voltages affect conversion accuracy of input codes such as 00...01 and 100...01 which causes some of the three-input amplifiers to have small input voltages. However, fortunately, DNL associated with these codes are relatively insensitive to the closed-loop-gain error as illustrated by considering the DNL at (100...0, 100...01) which is given by

$$DNL = (2k)^{i} - 1 \qquad (2)$$

where $i = N - j - 1$ and $j = log_2(V_{ref}/V_{critical})$. The variable $V_{critical}$ is the input voltage below which the closed-loop-gain errors of the three-input amplifier become significantly large.

Simulation of the circuit given in figure 3, indicate that closed-loop-gain errors is below 2% for input voltages lower than -71 mV. Using a reference voltage of -2.5 V and N=8 for a DNL less than 0.5 LSB, the maximum closed-loop-gain error allowed according to equation (2) is 22%. Thus large closed-loop-gain errors of the three-input amplifier for small input voltages is not a major concern.

The closed-loop-gain errors of the three-input amplifier for input voltages between -2V and -3V is negligible. Thus, according to equation (1), to achieve an accuracy of 8 bits (DNL=0.5 LSB), 0.2% of closed-loop-gain error due to process variation is allowed. Other simulation results for the three-input amplifier are summarized in Table 1.

Five experimental 12-bit D/A converters, implemented using the Northern Telecom 3μ-CMOS process designed for digital circuits, achieve resolutions of 10 bits (DNL=0.30 LSB), 8 bits (0.44 LSB), 7 bits (0.37 LSB), 7 bits (0.38 LSB) and 6 bits (0.50 LSB), for a negative output-voltage swing no larger than 3V peak-to-peak. The total area occupied by a D/A converter is 1.96 mm^2 or 3040 mil^2. This can be reduced to 1.4 mm^2 by simply placing the amplifier closer to one another.

A_o	1048 V/V or 60.4 dB
ω_u	3.9 MHz
ϕ_m	62.5^o
settling time	0.7 μs (20pF, 0.01%)
offset voltage	0.716 mV

Table 1: Simulated performance of the three-input amplifier

The highly regular structure of the D/A converter makes it very suitable for semi-custom chip fabrication using an analog standard cell approach. Rails for reference voltage and power supplies are laid out in such a way that they automatically couple to those of adjacent cells. Consequently, the addition and deletion of one bit from the D/A converter involves only adding or removing one three-input amplifier from the amplifier cascade.

The maximum speed of operation obtained using the linear ramp test is around 1 MHz. The high speed of operation is mainly due to a very small input capacitance of the three-input amplifier and the use of output buffer. The static power dissipation is approximately 50 mW.

An 8-bit successive-approximation A/D converter, having a differential nonlinearity of less than 0.5 LSB, was implemented using the D/A converter described here. The maximum sampling rate has been found to be approximately 100 kHz. Due to an error in the design of the digital control circuit a race condition exits and this prevent testing the A/D converter at a higher speed.

In concluding this paper, we would like to point out that any improvement in the resolution of the D/A converter reported here is solely dependent on improvements made in controlling the closed-loop gain of the three-input amplifier. New techniques such as dynamic biasing incorporated in three-input-amplifier designs that are currently being perfected lead to D/A converters with accuracies of over 10 bits.

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[1] The linearity error occurring at one or more points on the transfer curve can be reduced to zero or made negligible.