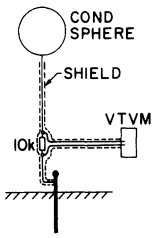

Fig. 2. Arrangement for potential measurement.

measurement arrangement used to determine the free potential in points below 60-Hz HV lines. The sphere is mounted on a plastic rod supported by a nonconducting tripod. A 3-ft rod is used for grounding.

The agreement between calculated values of free potential and values obtained from the measurements was found to be quite good. Some typical results are listed below.

x:	0			s		
y (ft)	5	6	7	5	6	7
$\lvert V_{x,y}\rvert$ (kV) calculated	2.45	3.00	3.60	4.60	5.60	6.58
$\lvert V_{x,y}\rvert$ (kV) measured	2.47	3.10	3.72	4.42	5.30	6.30

These results apply to a three-phase line of the configuration illustrated in Fig. 1 with $h = 34$ ft, $s = 22$ ft and an operating line voltage of 260 kV.

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The Kirchhoff Data Link

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Abstract—**A system is introduced for the acquisition of analog or digital data from a large number of remote sensors and its transmission and collection at a central processing facility. The system features buffering or impedance matching of the signal source, fundamental noise immunity to radiated and ground noise, integral power supplied along the signal lines, as well as fundamental ease of signal switching.**

Introduction

This paper introduces a novel solution to a typical systems problem namely, the acquisition of analog or digital data from a large number of remote sensors and its transmission and collection at a central processing facility. As will be shown, the novel concept in the system described results from a direct application of an old concept, Kirchhoff's current law. This derivation has suggested the name of the new technique.

A block diagram of a typical data-acquisition system is shown in Fig. 1. The source may be either analog or digital. A buffer stage is usually inserted between the source and the transmission line for matching purposes. The transmission line typically extends over some distance to the central computer facility where the signal is multiplexed, conditioned, digitized (if not already digital), and fed to the computer.

In data-acquisition systems there is usually a choice to be made between transmitting the data in digital or in analog form. Each scheme has its own merits and limitations. As will be shown, a potential advantage of the analog transmission scheme developed here is a considerable saving in cable costs especially if the sensor is located far from the computer facility.

The system described in this paper derives from the scheme shown in Fig. 1. To minimize the susceptibility to noise (both ground potential and radiated), the signal is transmitted in the form of two complementary currents over a shielded twisted pair. Information is encoded as the difference between the currents flowing in the wires of the pair. This mode of transmission also provides for a natural simplicity in signal switching. To further minimize cabling cost, the buffer stage is powered over the same lines that carry the signal. In the following section the system components are considered in some detail.

The Buffer

The key to the system is the buffer whose essential role is to convert the input signal from its natural mode into a pair of currents whose difference is proportional to some signal parameter. In some designs the pair of output currents vary in a complementary fashion (that is while one increases the other decreases by the same amount), though this is not a necessary condition. The currents produced by the buffer are conducted in the two wires of a shielded twisted pair. In addition to its environmental noise-rejection function, the shield provides a return path for the difference between the currents flowing in the wires of the signal pair.

Fig. 2(a) shows a black-box representation of the buffer stage. It is essentially a four-terminal network with terminals labelled V, C, P, and N. Terminal V represents a voltage input terminal with ideally zero input current and infinite input impedance. Terminal C represents a current input terminal with ideally zero impedance. Moreover, the voltage at C is ideally equal to the voltage applied to V [1]. Terminals P and N provide the positive and negative power leads through which a biasing current always flows as well as carry the signal currents. In the no-load situation, i.e., zero current through terminal C, a biasing supply current will flow into terminal P and out through N.

According to the nature of the signal source, there are various schemes for its connection to the buffer stage, which will be considered in detail subsequently. In each of these schemes one has to arrange for a current proportional to the signal to flow in terminal C. Application of Kirchhoff's current law will indicate that this current will be reproduced as a change in the currents at the terminals P and N. In some designs this change will occur symmetrically in both P and N in a complementary fashion while in others it will be single ended occurring in either P or N while the current in the other does not change. Therefore, the signal will be transmitted in the form of alteration in the current through either P or N or both. At the receiving end a subtraction of these two currents will recover the original signal.

Before proceeding further to the modes of application of such a buffer, it is appropriate to consider some possible implementations. A simple yet excellent implementation of

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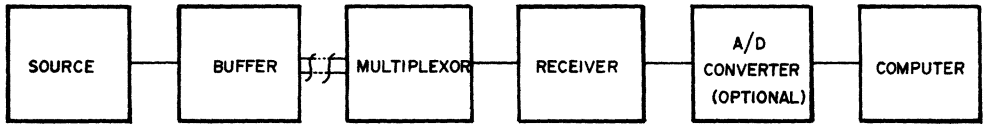

Fig. 1. System for the buffering, transmission, multiplexing, and reception of analog or digital signals.

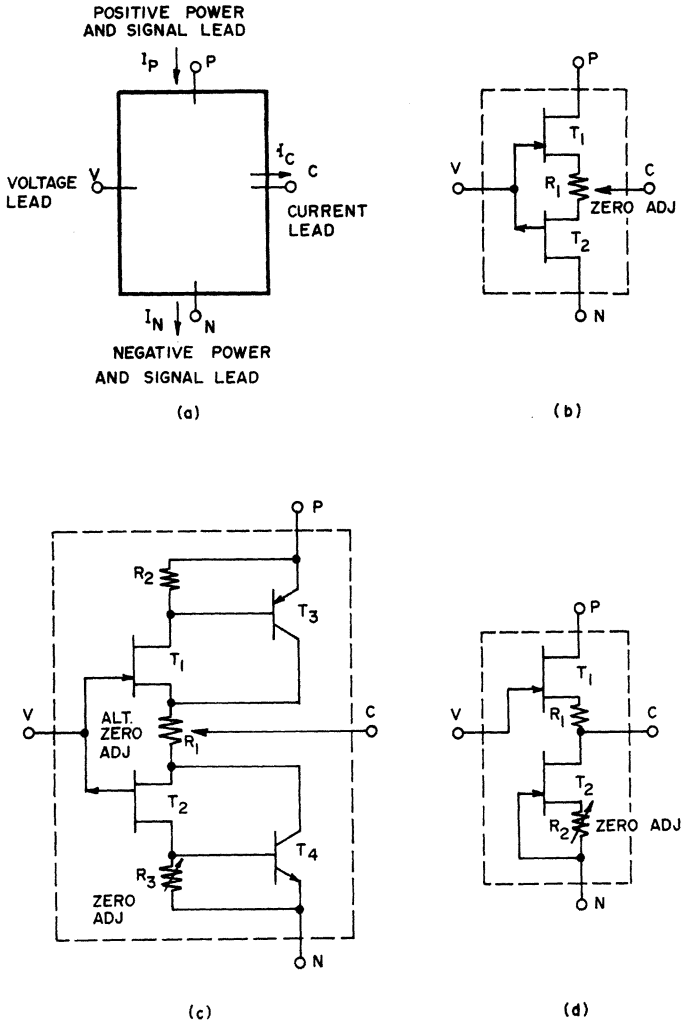

Fig. 2. Typical buffer elements receiving power from and transmitting differential signals on connecting shielded twisted pair. All FET's should be in close thermal proximity.

the buffer is shown in Fig. 2(b) where two complementary field-effect transistors (FET's) are connected as a self-biasing follower. The FET's should be matched to a reasonable degree for I_{DSS} and V_P. The end-to-end value of R_1 establishes the quiescent standing current through T_1 and T_2 that under the no-load condition (terminal C open) will flow in terminal P and out terminal N. The tap on R_1 is adjusted to account for minor mismatches in T_1 and T_2 such that the voltage at C is zero for a zero input voltage at V (referred to a shielded ground return external to the buffer). The input impedance of such a configuration is typically very high. The output impedance, however, is limited to $(1/2g_m + R_1/4)$ where g_m is the FET transconductance. This circuit is of the complementary type where both I_P and I_N change equally but with opposite sign so as to reproduce any current through terminal C, i.e., $I_P - I_N = I_C$ with the positive directions taken as indicated in Fig. 2(a).

Fig. 2(c) shows an improved implementation of the buffer with similar complementary characteristics. Transistors T_3 and T_4 are added to reduce the output resistance at C. Resistors R_2 and R_3 directly control the current levels in transistors T_1 and T_2, respectively, hence can be used to establish their operating points independently. One of these (say R_3) can be used as the zero adjustment. Resistor R_1 is normally center tapped. Its value together with the V_P characteristic of T_1 and T_2 establish the currents in T_3 and T_4. Again it is evident that the currents I_P and I_N are equal for a zero input voltage signal at V and any load on C, provided the zero is adjusted correctly.

Fig. 2(d) shows an alternative scheme [2] that belongs to the single-ended type or noncomplementary. It uses two identical FET's that are more easily matched and exhibit better thermal tracking than complementary pairs. In this circuit T_2 is self-biased via R_2. The drain current so produced flows through R_1 connected to T_1. If T_1 and T_2 are matched and $R_1 = R_2$, then clearly the voltage at C is the same as that at V to a good first approximation. Adjustment of R_2 will compensate for small mismatches. Although the current in T_2 (i.e., I_N) is forced to be constant by its biasing arrangement, the current in T_1 (i.e., I_p) will vary by the total amount I_C to satisfy Kirchhoff's law. Thus this implementation is of the single-ended variety.

Connection of the Signal Source to the Buffer

A variety of connections of the signal source to the buffer are possible, some of which are shown in Fig. 3. The most straightforward one is that shown in Fig. 3(a) where the source is connected directly to V, in which case the input impedance is very high. Thus the source is virtually unloaded. A resistance R_L is connected to C in order to accomplish the voltage-to-current conversion.

In the event that the signal is essentially a current source in nature, the connection in Fig. 3(b) is possible. Due to the low impedance at C, the signal current source will be virtually unloaded. A possible disadvantage, however, is that this connection has no current gain; that is, the line current difference is identical to the signal current. Accordingly, for very low signal currents the line signal-to-noise ratio may be prejudiced. In this case a modification of Fig. 3(a) may be useful in which the signal source current is fed into a resistance shunted from the V terminal to ground. The current gain in this case will be the ratio of this resistance to that connected to terminal C. In case a source termination is required a simple variation on Fig. 3(b) as in Fig. 3(c) may be used.

When very high transconductances are required to handle very small voltage signals, the scheme of Fig. 3(d) may be useful. Because of the bootstrap technique it requires, however, that the source be floating. A very high input resistance should also result.

The Receiver and a Typical System

Fig. 4 shows some of the details of a typical system in which the buffer stage of Fig. 2(b) is used. Since the signal source is a voltage, it is connected to the voltage terminal of the buffer. Resistance R_6 provides for the conversion of the voltage signal into a current through C. This in turn is reproduced as a pair of complementary currents that flow (superimposed on the bias current) through P and N and hence are transmitted over

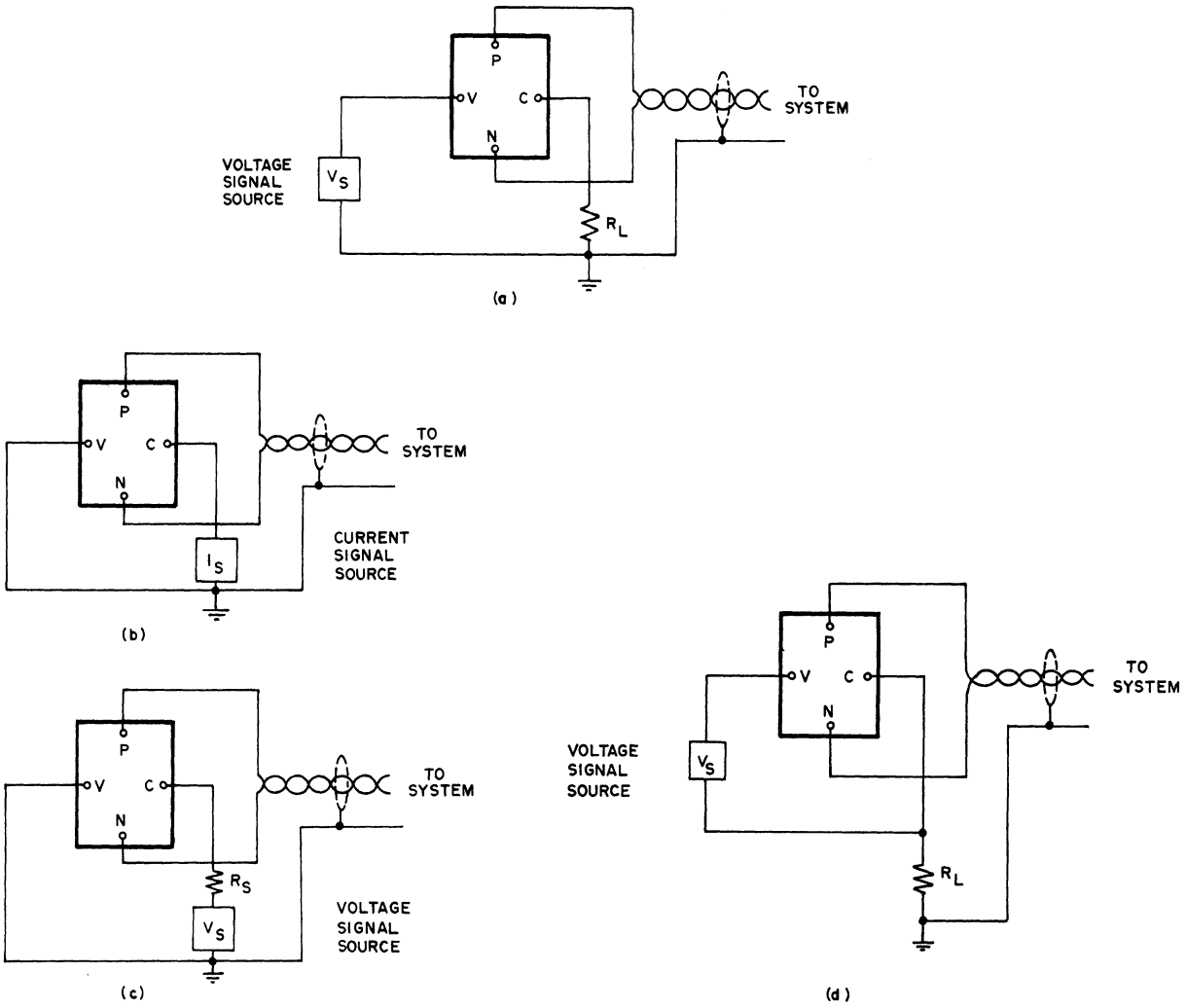

Fig. 3. Various application modes for the buffer element.

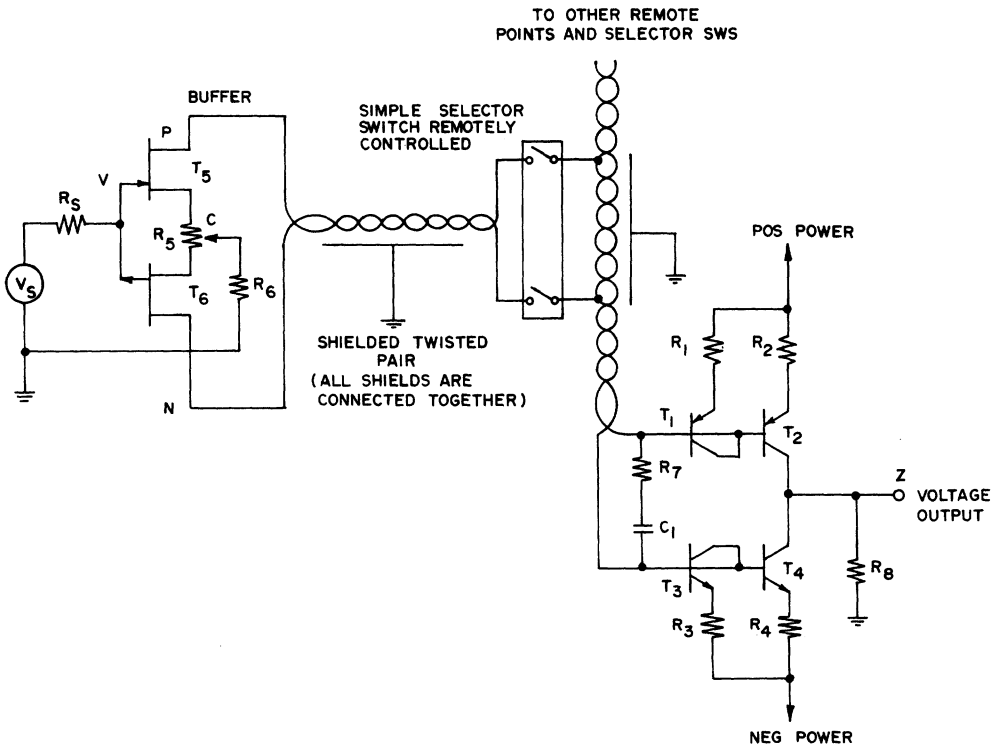

Fig. 4. Typical system detail.

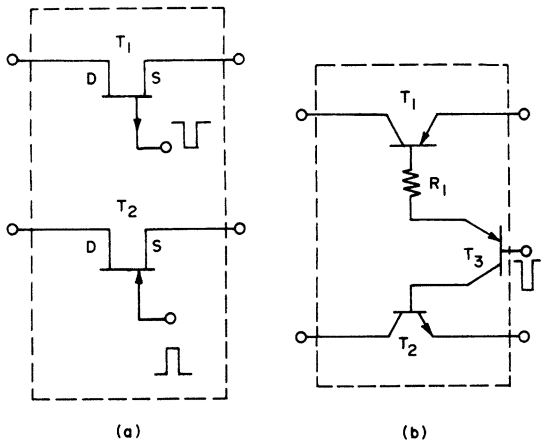

Fig. 5. Simple current switches.

the shielded twisted pair. As shown, the shielded twisted pair is part of a switched network of such cables. The particular cable and its signal source are selected by a part of a multiplexer switch array that may be distributed, as shown, throughout the system. The switches may be implemented with FET's or bipolar transistors. Switch control cables are not shown since the best implementation would vary with the system, from single selector leads to a generally distributed bus carrying coded switch-selecting data.

A simple but satisfactory receiver circuit is shown connected to the cable at the central end. Current from the N terminal of the buffer finds its way through the cable and switches to transistor T_3 of the receiver. Diode-connected T_3 transmits this current through R_3 to the negative power supply. As this current varies, the voltage on the base of T_4 varies as does the current in R_4. For the case of $R_3 = R_4$ the current in the collector of T_4 is the same as (or in general, some known multiple of) the current from the N terminal of the buffer. A similar argument shows that the current in the collector of T_2 will be equal to that flowing in the P terminal of the buffer. The connection of T_2 and T_4 provides for the difference in their collector currents, which is equal to the signal current through the terminal C of the buffer. This difference is available at point Z at a high impedance. If desired, this output current can be passed through a resistance R_8 to provide for an output voltage proportional to the signal voltage V_S, with a gain of (R_8/R_6).

In case it is required to properly terminate the transmission cable, this can be easily done by choosing

$$R_1 = R_2 = R_3 = R_4 = R_0 - 0.05/I,$$

where R_0 is the desired terminating resistance for each wire to ground, and I is the standing current flowing through T_5 and T_6. This formula is obtained by observing that the current flowing in each of T_1 and T_3 also will be I. Thus, each of these diode-connected transistors will have an average resistance of $0.05/I\ \Omega$ for silicon junctions at room temperature. The terminations provided in this manner are essentially for each line to ground. If an additional differential-mode termination is required, this should be capacitively coupled as represented by R_7.

Multiplexing or Selector Switches

Since the switched signal leads also provide power to the input buffer, there is no need to provide alternate paths for the switched currents. Thus a variety of simple switch schemes are possible. Some of these are shown in Fig. 5. Due to the fact that a pair of switches is required for each source and its cable, two switch control signals are inherently required. This is shown in Fig. 5(a) for the case of complementary FET switches. In many cases, however, the pair of signals is easily derived from a single source. Such a scheme is shown in Fig. 5(b), which also illustrates the fact that very imperfect switches can be used. Transistors T_1 and T_2 of Fig. 5(b) are bipolar devices having, in general, collector-to-emitter offset voltages and resistances as well as finite beta. However, none of these defects impair operation.

Consider the base current required to turn on T_1 and T_2. This must be large enough to force both T_1 and T_2 on for the range of collector currents expected. However, provided these two base currents are equal their value is not critical since they will flow back to the receiver to produce zero net signal current. When the base of transistor T_3 is brought more negative than the positive signal line, T_3 will turn on forcing T_1 on. Current from T_1 will flow through T_3 to turn T_2 on. These two currents will be nearly equal, particularly if T_3 is a Darlington pair or a FET.

Conclusions

It has been shown that a circuit-design approach can provide novelty and versatility in system design of data collection systems.

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Further Possibilities of the Modulated Subcarrier Technique for Microwave Attenuation Measurements in Industrial Applications

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Abstract—**In this paper a microwave system for attenuation measurement by means of the modulated subcarrier method supplying additional information on the actual parameters of the system is described. The information can be used for automatic control of output signal indicator sensitivity making the results independent of the instability of these parameters. Experimental results are reported illustrating the validity of the analysis.**

I. Introduction

The microwave system for attenuation measurement by means of the modulated subcarrier method described by Schafer and Bowman [6] is now widely used for measurement purposes owing to its good linearity, high sensitivity, and wide range of measured values. Many authors analyzed the possibilities of this system [5]. Among others, some previous publications of the author [2], [3] dealt with the modulated subcarrier method, particularly with a chance of automatic compensation of results obtained under fluctuating ambient conditions and in longer time intervals for the variation of microwave signal source power and detection efficiency. Such a compensation is of considerable importance when using the modulated subcarrier systems as input transducers in automatic control systems of industrial processes. In those systems the

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