A JFET Circuit for Instrumentation Applications

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Abstract—**A new class of junction field-effect transistor (JFET) circuit is introduced, which can serve as a simple versatile building block in instrumentation applications. Economical realizations of current-to-voltage converters, voltage-controlled voltage sources, and voltage-controlled current sources are described. The basic circuit building block, called the piggy-back pair, consists of a matched pair of JFET's and two resistors. The basic configuration is easily manipulated to realize various circuit functions when combined with a few other components. It is shown that by full utilization of the terminal properties of JFET's, many simple high-performance circuits can be designed, which have circuit functions determined essentially by resistor ratios and which accordingly are relatively insensitive to device parameters. The circuit design procedure is very straightforward with design limitations clearly indicated. The flexibility and versatility of the piggy-back pair is indicated by the wide range of circuits demonstrated.**

I. Introduction

CIRCUIT designs employing junction field-effect transistors (JFET) are often unimaginative in that JFET's are used essentially as direct replacements for bipolar transistors. Usually only a simple advantage is taken of the high input resistance of the JFET while depletion mode operation is generally considered a disadvantage to be tolerated. It is the purpose of this paper to present a class of circuits that use to considerable advantage three properties of JFET's, namely, (1) high input impedance, (2) depletion mode of operation, and (3) source to drain impedance transformation. A further advantage of the class of circuits to be introduced is that the troublesome temperature effects of JFET's can in general be eliminated or at least minimized.

The basic circuit building block upon which this treatment is based has been called the "piggy-back pair." Various combinations of this basic configuration accompanied by a limited number of other components can be used to economically implement various circuits including 1) ultralow-level current to voltage converters, 2) voltage-controlled current sources, and 3) voltage-controlled voltage sources. The circuits to be described have applications in the general area of instrumentation particularly in the fields of nuclear and biomedical electronics [1]. They are also of interest in the active circuit area as extremely low-level high-impedance synthesizing gain blocks. These gain blocks offer the advantages of low power consumption together with the possibility of extremely high-impedance circuits in which very small capacitors can be used. All circuits are compatible with thin-film hybrid circuit technology.

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II. Circuit Description

First, the detailed operation of the basic circuit building block will be outlined. Following this will be a description of various circuit configurations using this building block to implement black box characteristics. Some test results will be included.

A. Piggy-Back Pair

The piggy-back pair consists of two matched JFET's Q_1 and Q_2 (n channel for the purposes of discussion) and two resistors, R_1 and R_2 as shown in Fig. 1.

To analyze the circuit, consider the input grounded. Q_1 and R_1 establish an operating current level of I_1, where

$$I_1 = V_{GS_1}/R_1. \tag{1}$$

I_1 can be found analytically by solving the two equations

$$I_1 = I_{DSS_1}\,[1 - V_{GS_1}/V_{P_1}]^2 \tag{2}$$

(Middlebrook approximation)

and

$$V_{GS_1} = I_1 R_1. \tag{3}$$

The current I_1 is extracted from R_2 and Q_2 to establish an operating point of I_1 and V_{GS_2}. The voltage at the output now is

$$V_{\text{out}} = V_G + V_{GS_2} - I_1 R_2. \tag{4}$$

Substituting (1) in (4) we see that

$$V_{\text{out}} = V_G + V_{GS_2} - (V_{GS_1} R_2/R_1). \tag{5}$$

Now if $R_1 = R_2$ and Q_1 is matched to Q_2 (that is to say $V_{GS_2} = V_{GS_1}$ for the same current level), the output establishes itself at an operating voltage level of V_G.

Analysis for applied signals is very similar in nature. Consider a voltage V_{in} applied at the input. The current in Q_1 now becomes

$$I + \Delta I = \frac{V_{GS_1}}{R_1} + \frac{V_{\text{in}} - \Delta V_{GS_1}}{R_1} \tag{6}$$

for which the output voltage is given by

$$V_{\text{out}} = V_G + V_{GS_2} - \Delta V_{GS_2} - \left[\frac{V_{GS_1}}{R_1} + \frac{V_{\text{in}} - \Delta V_{GS_1}}{R_1}\right] R_2. \tag{7}$$

Assuming that Q_1 and Q_2 remain matched over the current range of interest [2] it can be seen that the signal transfer

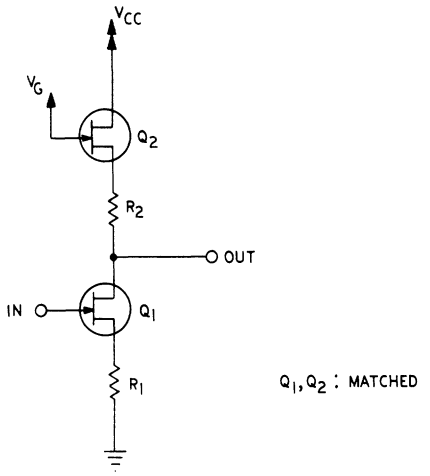

Fig.1. Circuit schematic of the piggy-back pair.

characteristic is

$$V_{out} = V'_G - V_{in} R_2/R_1, \tag{8}$$

where

$$V'_G = V_{GS} [1 - (R_2/R_1)].$$

That is, the piggy-back pair provides a negative gain of R_2/R_1 with a dc level shift of V'_G.

The normal mode of operation will be with $R_1 = R_2$ to minimize any mismatch in Q_1 and Q_2. Any fixed voltage offset of Q_1 and Q_2, $(V_{GS_1} - V_{GS_2})$ will constitute an additive term to V_G and is often insignificant. In effect then a voltage signal between the gate of Q_1 and ground is transported to become a voltage signal between the gate of Q_2 and the drain of Q_1.

Due to the depletion mode of operation of Q_1 there is no restriction on the input signal polarity with the use of a single power supply. The input signal range is restricted however by the following conditions. First, the negative swing is limited by the pinch-off voltage (V_p) of Q_1. Second, the positive swing V^+_{max} is limited by the fact that Q_1 must remain in the saturation region of operation, that is,

$$V_G \geqslant 2V^+_{max} + V_{DSsat}. \tag{9}$$

These conditions are of course qualified by the fact that Q_1 and Q_2 must remain matched throughout the entire signal excursion. Signal symmetry can be obtained by choosing the appropriate device parameters and the appropriate bias voltage V_G.

A significant point to note is that the circuit gain is dependent only on a resistor ratio R_2/R_1. This allows a free choice of operating current. The logical current at which to operate the circuit then is at the zero temperature coefficient point of Q_1 and Q_2 such that a temperature stabilized amplifier results. The procedure is very straightforward. The zero temperature coefficient current I_{DZ} is determined from the device specifications or by measurement [3]. V_{GS_Z} is then determined using (2) for which the value of R_1 is given simply as

$$R_{1Z} = V_{GSZ}/I_{DZ}. \tag{10}$$

In summary, the piggy-back pair displays the following characteristics.

1) It has an inherent high input impedance ($> 10^9$ Ω) and a low input offset or bias current ($< 10^{-9}$ A).
2) The gain is given by a resistor ratio.
3) The output is dc level shifted.
4) The circuit can be temperature stabilized.
5) The output impedance is relatively low compared to JFET input impedances, though not in absolute value.

III. Low-Level Current-to-Voltage Conversion

A problem facing the instrument circuit designer is that of providing an economic but accurate means for measuring ultralow-level currents (defined for present purposes as any current less than 1.0 μA. For many purposes the current should be amplified or converted to a voltage where standard instruments including chart recorders and A/D converters can be used to monitor its amplitude.

A possible method for measuring low-level currents is to use an operational amplifier in one of two different configurations. The first direct approach is to use a noninverting amplifier to amplify the small voltage produced by passing a current through a resistor. This resistor must be 100 times smaller than the output impedance of the current source (including cable resistance) for 1 percent accuracy. Under these conditions the voltage signal that is to be amplified is typically in the range of the input offset voltage of low-cost amplifiers and reliable operation is difficult.

A second possible configuration involves passing the current into the negative input of an inverting feedback amplifier, with the feedback resistor used to convert the current to usable voltage levels at the output. The limitation of this method is that the input offset current must be much smaller than the current level to be measured. This restriction normally also eliminates low-cost amplifiers.

Two economical solutions to this problem are presented here. All of the circuits introduced are based on providing several stages of current to voltage conversion and voltage to current conversion through the use of the piggy-back pair. The impedance transformation properties of JFET's are used to provide gain.

A. Current-to-Voltage Converter

The first circuit is that shown in Fig. 2. Transistors Q_1 and Q_2 are p-channel JFET's connected as a cascode pair. This configuration provides a very high output impedance at the drain of Q_2 [4]

$$R_0 = g_m/g_0^2, \tag{11}$$

where g_0 = output conductance of Q_1 and Q_2 alone. The input impedance at the source of Q_1 is relatively small compared to the output impedance at Q_2 and can be approximated by

$$R_{in} \simeq 1/g_m. \tag{12}$$

Thus

$$R_0/R_{in} = g_m^2/g_0^2. \tag{13}$$

The range of this ratio is generally 1000:1.

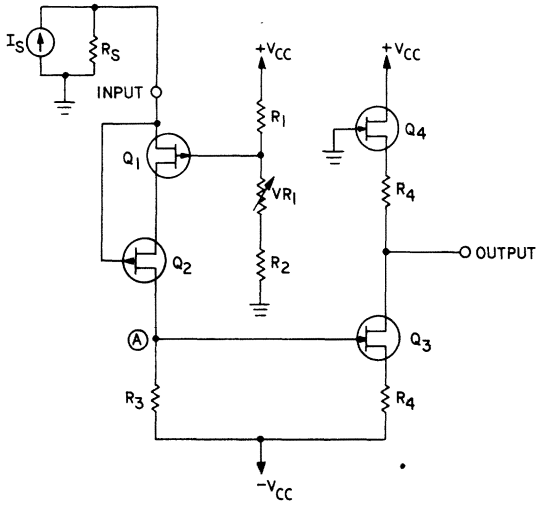

Fig. 2. Current-to-voltage converter.

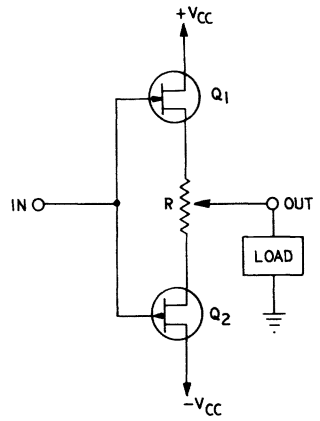

Fig. 3. Complementary JFET buffer.

Any current I_s forced into the input appears at the drain of Q_2. This current is converted to a voltage by R_3, which can be very large and is chosen to provide a signal voltage in the range of 0-10 V. Thus Q_1 and Q_2 serve to isolate a current source with a finite output impedance from the large voltage swing present at the current to voltage convertor resistor R_3.

The input impedance of the Q_1, Q_2 cascode pair is current dependent with typical values less than 1 MΩ at 10 nA.

Thus currents produced by a current source with $R_s >$ 100 MΩ can be measured to 1 percent accuracy. The value of R_3 (and correspondingly the current to voltage conversion ratio) is limited by R_0 of the Q_1, Q_2 cascode pair.

The voltage at the gate of Q_1 is set at some positive potential by the voltage divider R_1, R_2 thereby establishing the input potential at ground and eliminating currents produced by the input potential and R_s. Such currents would otherwise swamp the current signal to be measured.

The signal voltage across R_3 is referenced to $-V_{cc}$. It is desirable to shift this signal such that it is referenced to ground potential without loading the high impedance signal point A. To accomplish this the piggy-back pair of Q_3, Q_4 is used with the gate of Q_4 tied to ground. Thus the signal at A is reproduced at the output with a phase inversion and a ground potential reference.

If R_4 is made small (a few kilohms) the standing current in Q_3 and Q_4 will be in the milliampere range, which is often compatible with the temperature stability criterion. This high current operation also allows a significant amount of output current without performance degradation of the piggy-back pair and a resulting loss of accuracy. Thus the output can drive a standard instrument such as a recorder or an A/D converter for computer monitoring of low-level currents.

B. JFET Buffer

If the problem of output loading is encountered, a simple but elegant JFET buffer can be used without significant additional cost. The buffer circuit is illustrated in Fig. 3. The buffer uses complementary n-channel and p-channel JFET's analogous to the class AB output stages found in many integrated operational amplifiers. This configuration is however self-biasing with the gates of Q_1 and Q_2 connected together to form the input node. The source of Q_1 is at $+V_{GS_1}$ and the source of Q_2 is at $-V_{GS_2}$. This means that the tap on the resistor R can be adjusted to give zero dc offset at the output. The standing current level is determined by R and the JFET parameters as may be seen by the simultaneous solution of (14)-(16):

$$I = \frac{V_{GS_1} + V_{GS_2}}{R} \tag{14}$$

$$V_{GS_1} = V_{P_1}\left[1 - \frac{I}{I_{DSS_1}}\right]^{1/2} \tag{15}$$

$$V_{GS_2} = V_{P_2}\left[1 - \frac{I}{I_{DSS_2}}\right]^{1/2} \tag{16}$$

The output impedance R_{out} is a direct function of R. The value of R_{out} can be lowered to a few hundred ohms by choosing the appropriate value of R.

C. Voltage-Controlled Voltage Source

The second configuration in the class of circuits utilizing the piggy-back pair is basically a voltage-controlled voltage source as shown in Fig. 4. This circuit is capable of amplifying input signals in the millivolt range to produce output signals in the volt range. That is, an accurate voltage gain of 100 or more is realizable in an open-loop manner.

For the circuit illustrated in Fig. 4 the input stage is an n-type piggy-back pair Q_1, Q_2. From the previous analysis of the pair it can be seen that any voltage at the input appears across R_2. Thus R_2 converts the input voltage into a current of the value V_{in}/R_2 and extracts this current from node 1. This same current is then injected at the drain of Q_1. Thus a constraint is placed on the ratio R_2 to R_1. In order to ensure the 1 percent accuracy of the input pair, R_2 should be two orders of magnitude larger than R_1.

The current V_{in}/R_2 extracted from node 1 is then drawn through Q_3 and appears at a high impedance level at its drain due to the impedance transformation properties of Q_3. It should be noted that Q_3 provides the same function as the cascode pair in the previous current-to-voltage converter. The in-

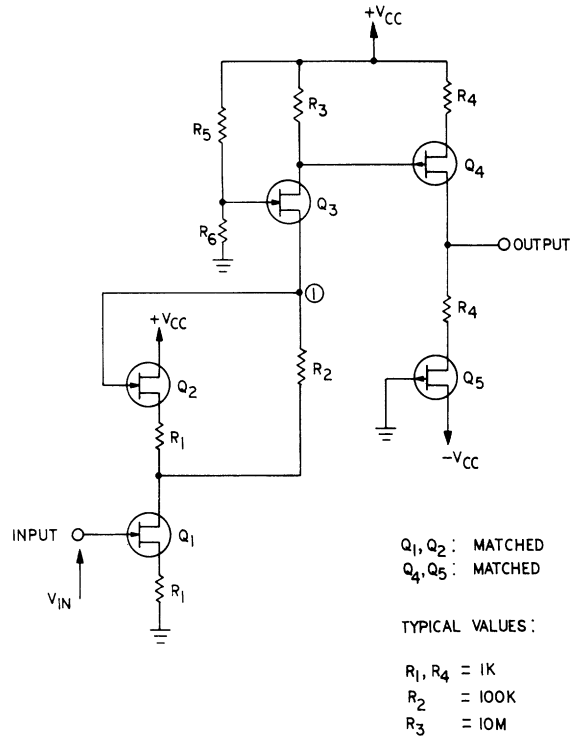

Fig. 4. Positive-polarity voltage-controlled voltage source.

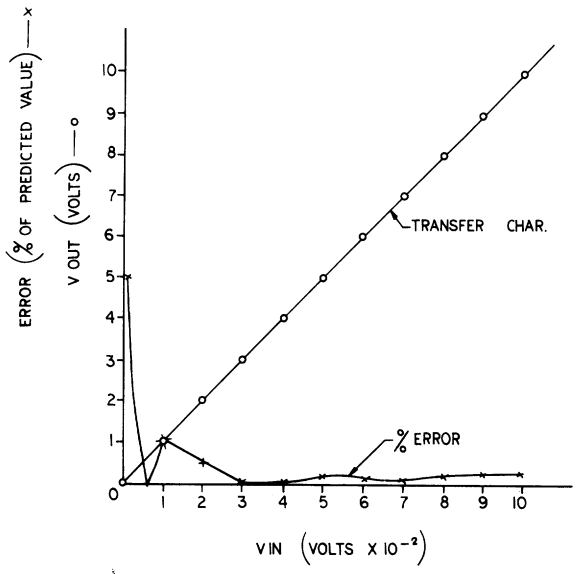

Fig. 5. Experimental results for positive polarity VCVS.

put impedance of the impedance transformer Q_3 however, is not critical in the present circuit, due to common mode rejection at node 1. That is, any change in the potential of the source of Q_3 due to its input impedance is not seen across R_2 since the gate of Q_2 is bootstrapped to the source of Q_3. Thus, the voltage across R_2 and thus the current through it are determined solely by the input pair.

Q_3 in conjunction with R_5 and R_6 also provides the bias voltage V_{G_1} for the input pair.

Note however in this particular circuit Q_3 imposes a signal polarity restriction on the input. The input can never go negative since Q_3 is a unilateral device.

The current V_{in}/R_2, which is drawn through Q_3, is converted into a large voltage signal by R_3. This signal is referenced to $+V_{cc}$ so a p-type piggy-back pair Q_4, Q_5 is used to transfer the signal reference to ground potential in a similar fashion to Q_3, Q_4 in Fig. 2. The voltage gain of this circuit is again a resistor ratio given by

$$V_{out}/V_{in} = R_3/R_2. \tag{17}$$

The measured voltage transfer characteristic of this voltage-controlled voltage source (VCVS) is illustrated in Fig. 5.

D. Polarity Independent Current-to-Voltage Converter

A simple modification of the VCVS of Fig. 4 allows the implementation of a current to voltage converter with a bipolar current input. This circuit is illustrated in Fig. 6.

The signal current i_s is converted to a bipolar voltage by the resistance R_{in} that is then fed to a biased voltage-controlled voltage source. To make a biased VCVS of the kind shown in Fig. 4, a constant bias current I_1 is extracted from node 1. This is accomplished by the addition of Q_6 and R_6 as a conventional JFET constant current source. Now positive and negative signal currents can flow in Q_3 eliminating the polarity restriction encountered previously.

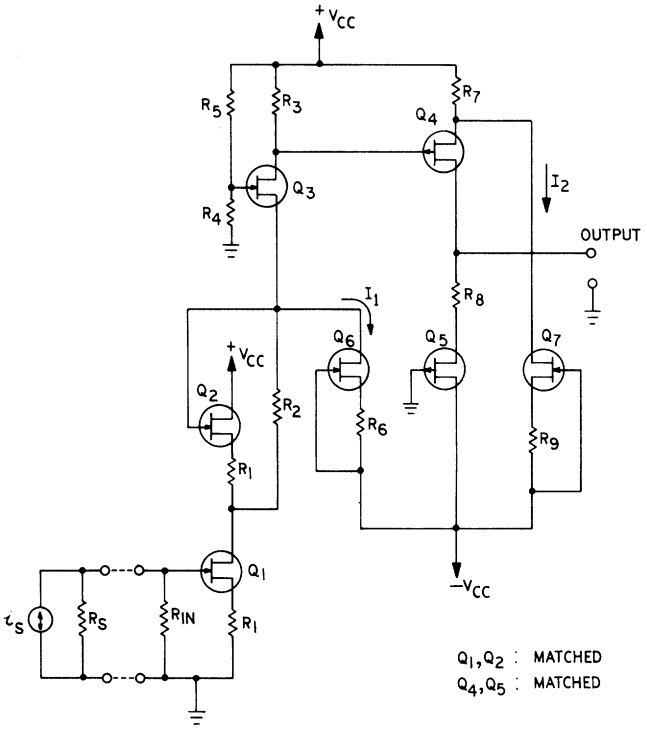

Fig. 6. Polarity-independent current-to-voltage converter.

The effect of this bias current I_1 at the output must now be removed. To accomplish this, a bias current I_2 is extracted from the source of Q_4 such that Q_4, R_8, and Q_5 do not see the effect of any bias currents. I_2 is produced in a similar manner to I_1 by the use of Q_7 and R_9. The cancellation of the bias current I_1 by I_2 means that these currents must exist with a ratio given by

$$I_1/I_2 = R_7/R_3. \tag{18}$$

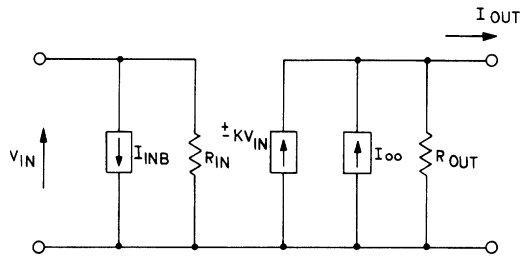

Fig. 7. Equivalent circuit representation of VCCS.

Thus to a first approximation assuming Q_6 and Q_7 matched

$$R_9/R_6 = R_7/R_3. \tag{19}$$

Allowing that the bias currents cancel each other, the current to voltage conversion can be viewed in the following manner. Current amplification of value R_{in}/R_2 is provided by the input piggy-back pair. This amplified current is then converted to a voltage signal by the impedance transformer Q_3 and R_3. This voltage is then transported to the output by the output piggy-back pair. Thus the current to voltage conversion ratio is given by the following relationship

$$V_0/i_s = R_{in}R_3/R_2. \tag{20}$$

IV. Voltage-Controlled Current Sources

In many circuit and system designs it is often convenient to have at one's disposal a voltage-controlled current source. Such a circuit building block can be thought of as the complement of an operational amplifier, which is a current- (or voltage) controlled voltage source. Voltage-controlled current sources have many distinct advantages in instrumentation systems where current signal transmission is desirable in a high-speed noisy environment. They also have many applications in the class of networks that include active filters, gyrators, and negative impedance convertors.

Before examining the detailed circuit operation, the black box terminal characteristics of a voltage-controlled current source (VCCS) must be defined. An equivalent circuit representation of a VCCS is illustrated in Fig. 7. In the ideal case the circuit should possess:

1) infinite input impedance R_{in},
2) infinite output impedance R_{out},
3) constant K over a wide signal range,
4) zero input bias current I_{INB},
5) zero output offset current I_{00},
6) temperature and time stability.

These properties will provide a basis for judging the quality of the circuit implementation proposed.

There are two types of VCCS's as illustrated in Fig. 8(a) and (b) distinguished only by their transfer polarities. The positive VCCS [Fig. 8(a)] is characterized by an input voltage V at port 1 producing an output current I at port 2 in the direction indicated. The relationship between V and I is given as

$$I = KV. \tag{21}$$

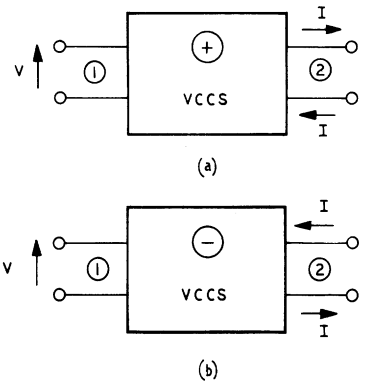

Fig. 8. Black box representation. (a) Positive-polarity VCCS. (b) Negative-polarity VCCS.

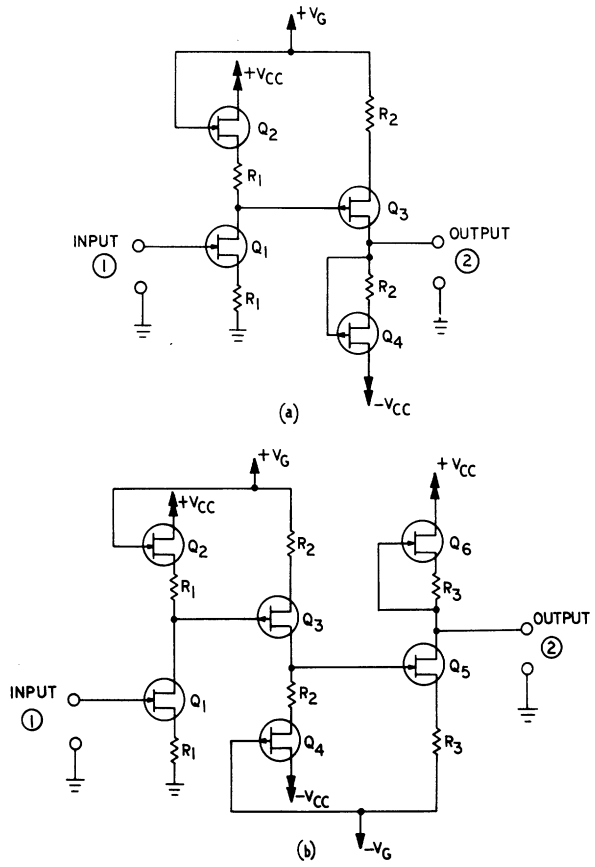

Fig. 9. Circuit schematics. (a) Positive VCCS. (b) Negative VCCS.

The negative VCCS [Fig. 8(b)] produces an output current in the opposite direction to that of the positive VCCS as indicated in (22)

$$I = -KV. \tag{22}$$

Economical implementations of both types of VCCS's utilizing JFET piggy-back pairs will now be introduced. An application of these circuits as active network building blocks will also be presented along with experimental results.

A. Positive VCCS

The first circuit of the class above is that of the positive polarity VCCS as illustrated in Fig. 9(a).

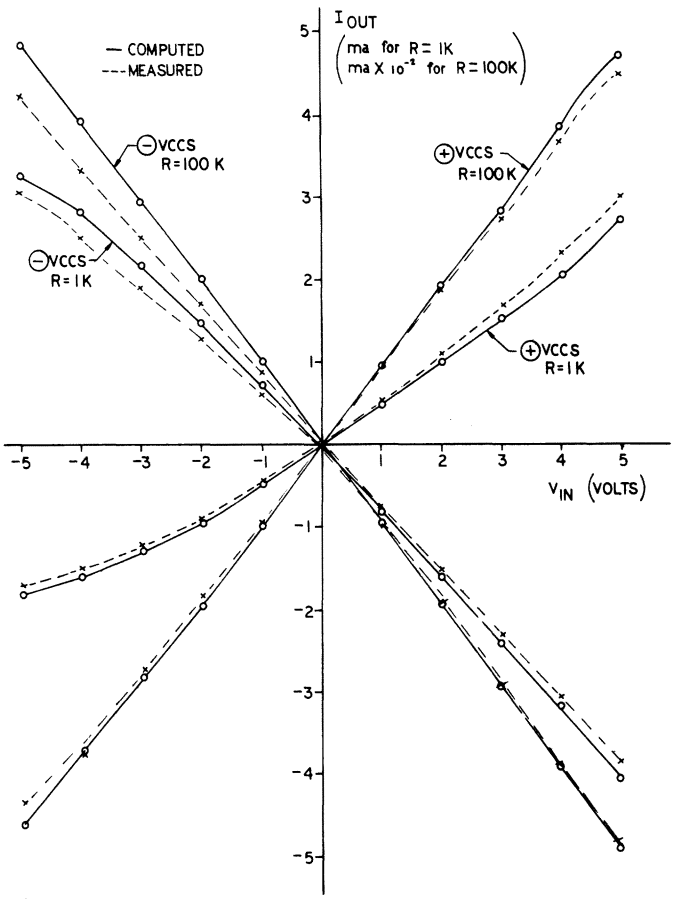

Fig. 10. Experimental and computer-calculated transfer characteristics of positive and negative VCCS's for different values of the conversion resistor R.

The input stage is an n-type piggy-back pair Q_1, Q_2 transporting the input signal from port 1 to a signal voltage existing between the power supply V_G and the drain of Q_1. This signal is fed in turn to a modified p-type piggy-back pair Q_3, Q_4 instead of a resistor as in the voltage-controlled voltage source. Thus the loading of the first pair has been eliminated.

The current in Q_3 has two components: 1) a dc quiescent current I determined in the same manner as the quiescent current in the piggy-back pair and 2) a signal current i, which is given by V_{in}/R_2. The objective now is to cancel the bias current and extract the signal current i at the drain of Q_3. This is accomplished simply by tying the gate of the bottom JFET of the output pair (Q_4) to the drain of Q_3, which is now the output. Q_4 is now operated in a two terminal constant current source mode exactly canceling the quiescent current of Q_3 at the output node. Ideally then

$$i_{out} = V_{in}/R_2. \tag{23}$$

Measured and computer-calculated results are shown in Fig. 10.

B. Negative VCCS

The circuit for the negative-polarity voltage-controlled current source is illustrated in Fig. 9(b). Its operation is very similar to that of the positive VCCS except that an intermediate piggy-back pair Q_3, Q_4 has to be added between the input and output pair to provide for a signal voltage inversion. The output stage is now an n-type pair operating in exactly the same fashion as the p-type pair in Fig. 9(a). The ideal output current signal is given by the following relation:

$$i_{out} = -V_{in}/R_3. \tag{24}$$

The measured and computed results for this circuit are also shown in Fig. 10.

C. Comparison of Circuit Implementation with the Ideal VCCS

A comparison of the actual circuit implementations of the two VCCS's with the ideal terminal characteristics as laid down in Section IV can now be made.

1) The input impedance is that of a reversed biased semiconductor diode junction. Typical values are a few hundred megohms at low frequencies decreasing to a few hundred kilohms at frequencies in the 100-kHz range due to the input capacitance.

2) The output impedance is essentially that of the output impedance of two JFET current sources in parallel. Typical values are usually in the range of a few hundred kilohms. If higher values are required two techniques can be employed: a) use a cascode FET connection in the output stage; or b) use bifets in the output stage. By using the added circuitry the output impedance can be boosted to values ranging from 1 to 10 MΩ.

3) The signal range, as indicated previously, is determined primarily by the pinch-off voltage of the JFET's used. Thus input signals ranging typically from ± 1 to ± 6 V are allowed. The output current signal range depends on the value of conversion resistor one wishes to use. There are however limitations on the size of this resistor. Ideally, as stated previously,

$$i_{out} = \pm \frac{V_{in}}{R_{conv}}.$$

This implies that the g_m of the output conversion JFET must be very high and remain constant over the entire range of output signal currents. This constraint can be relaxed to the extent of allowing g_m to take on realistic small values. Under the condition of low g_m the voltage to current conversion relationship becomes

$$i_{out} = \frac{V_{in}}{R_{conv} + 1/g_m}. \tag{25}$$

This relationship can be verified by considering the small signal equivalent circuits of Fig. 9. Thus for good linearity R_{conv} should be large since in fact g_m is approximately constant over a range of a few hundred microamperes of signal current. Small conversion resistors result in large signal currents with nonlinearity while large resistors result in very small signal currents that are linearly related to the input. Practical limits on R_{conv} are between 1 kΩ and 1 MΩ as Fig. 10 indicates. To achieve larger currents while still maintaining linearity, bifets must be employed in the output pair.

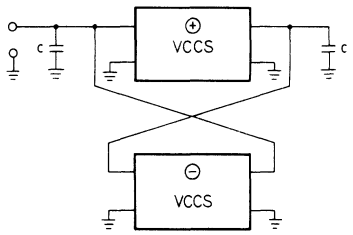

Fig. 11. Active *LC* resonant circuit using voltage-controlled current sources.

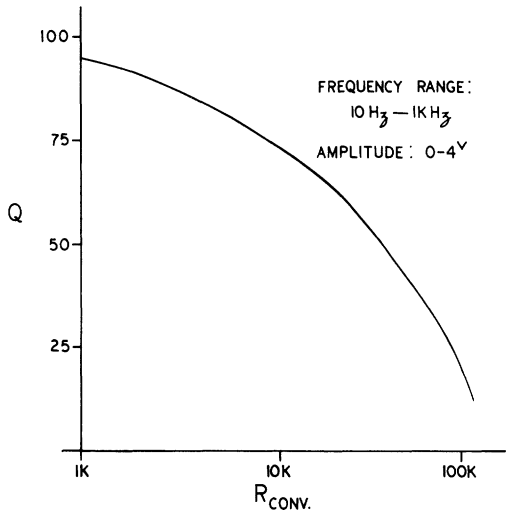

Fig. 12. Q variation with conversion resistance R_{conv}.

4) The input bias current is the leakage of a reversed biased p-n junction and is typically less than 1nA at 25°C.

5) The output offset current can be eliminated by a trimming resistor in the output stage.

6) Temperature stability can be attained by thermal coupling of the matched JFET's and by operating them at their zero temperature coefficient point.

D. Circuit Application

The particular application investigated was that of an economical active bandpass filter for low frequencies. A gyrator was implemented using the VCCS's to produce an active *LC* resonant circuit (Fig. 11) [5]. Such an implementation requires only 10 JFET's. Q approaching 100 over the frequency range of 10 Hz to 1 kHz were obtained for signal voltages up to 8 V peak to peak. The value of Q is dependent however on the value of the conversion resistor as illustrated in Fig. 12.

V. Conclusions

A new class of JFET circuits are introduced, which employ the basic circuit configuration herein called the piggy-back pair. The design of this set of circuits was based primarily on the exploitation of all the inherent characteristics of JFET's namely their high input impedance, their depletion mode of operation and their impedance transformation from source to drain.

Circuit implementations of low-level current-to-voltage converters, voltage-controlled voltage, and current sources are discussed. The use of these circuits as building blocks in such areas as instrumentation systems and active network design is presented to indicate their wide range of application.

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