Injected voltage low-power CMOS for 3-valued logic

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Indexing terms: *Integrated circuits, Logic*

Abstract: A new family of 3-valued CMOS logic circuits that uses 2-power supplies, each below the device threshold voltage, is presented. Circuit design of basic ternary operators (inverter, NAND, NOR) is described. These basic ternary operators can be used as building blocks in 3-valued digital systems.

1 Introduction

The complementary metal-oxide semiconductor family of integrated circuits (CMOS) has been used by several authors in the realisation of 3-valued logic circuits [1–8]. In all previous designs, authors have used voltage power supplies higher than the threshold voltages of the p- and n- channel MOS transistors. In most cases, this has resulted in high power consumption in the circuits. A new family of 3-valued CMOS circuits that is not restricted to the use of power supplies at the above threshold voltages is presented. The new design reduces power consumption in the circuits and comprises better performance. Circuits of basic ternary operators (inverters, NAND and NOR) are shown.

2 Design description

The ternary inverter circuit (Fig. 1) is composed of one p-channel and one n-channel enhancement-type MOS transistor and one resistor. The source of the p-channel transistor is connected to a + 1 V power supply and the source of the n-channel is connected to − 1 V. The drains of the two channels are connected to each other and constitute the output that is also connected to a load resistor R which is in turn connected to a fixed voltage C. The value of the voltage C defines the type of ternary inverter being implemented by this circuit. If the voltage C is at a high level (+ 1 V), intermediate level (0 V) or low level (− 1 V), the circuit will be implementing the function of a positive ternary inverter (PTI), simple ternary inverters (STI) or negative ternary inverter (NTI), respectively [1–2]. Following one of many possible conventions, we shall label the lower, middle and upper levels logic 0,1 and 2, respectively. Thus, the three types of ternary inverter are defined by

$$\overline{xC} = \begin{cases} C \text{ if } x = 1 \\ \\ 2 - x \text{ if } x \neq 1 \end{cases} \quad (1)$$

where C takes the value of 2 for the PTI, 1 for the STI and 0 for the NTI operator.

If the input x is at the high level (logic 2) the p-channel transistor will be off while the n-channel transistor will be on and the output will be low (logic 0) independently of the value of C. The output will be, at the high level (logic 2), also independent of the value of C if the input x is at logic 0, because this will render the p-channel transistor on and the n-channel off. However, if the input x is at the intermediate level (logic 1), both transistors will be off and the output will take the value of C: 2 in the case of PTI, 1 for STI and 0 for NTI.

Note that, for proper operation of the above ternary inverter, the following relationship must be satisfied:

$$V < V_T < 2V \quad (2)$$

where ± V is the value of the power supply and V_T is the threshold voltage of the p-channel and/or n-channel MOS transistors.

Note also that there is only one physical output for the three types of inverter and that the type of the inverter is selected by an external control input C. Thus, the ternary inverter circuit of Fig. 1 can be used as a building block in a 3-valued logic system and the injected voltage C can be generated within the system from other building blocks or by an external voltage generator.

The circuit is built and tested by using MC14007 CMOS integrated circuits. The measured propagation delay, rise and fall times under various input transitions to the simple ternary inverter with a 33 pF load is summarised in Table 1. The noise margin for this circuit is found to be + 0.58 V and − 0.46 V.

By applying the same methodology used above, the ternary NOR (TNOR) has been also realised. Similar to the ternary inverter, the circuit of Fig. 2 implements the functions of the positive TNOR, the simple TNOR and the negative TNOR

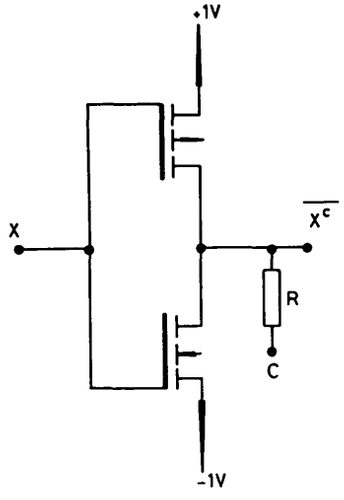

Fig. 1 *Ternary inverter*
$R = 25\,k\Omega$

Table 1: Propagation delay, rise and fall times of the simple ternary inverter with 33 pF load

Transition	Propagation delay time	Rise/fall time
	μs	μs
0 to high	0.4	0.8
High to 0	8	25
0 to low	0.2	0.4
Low to 0	8	12
High to low	0.4	1
Low to high	0.1	0.2

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[1–2], which are defined by

$$\overline{(x \, V y)^C} = \overline{\{\max(x,y)\}^C} \quad (3)$$

where $C = 1$ for the simple TNOR, 2 for the positive TNOR, and 0 for the negative TNOR.

The 2-input TNOR of Fig. 2 is composed of two p-channel transistors connected in series, two n-channel transistors conected in parallel, and one resistor. The source of the first p-channel is connected to a + 1 V power supply and the source of the two n-channels is connected to − 1 V. The drain of the second p-channel is connected to the drain of the two n-channels constituting the output that is also connected to a fixed voltage C. Similar to the ternary inverter, the value of the voltage C defines the type of TNOR being implemented by this circuit.

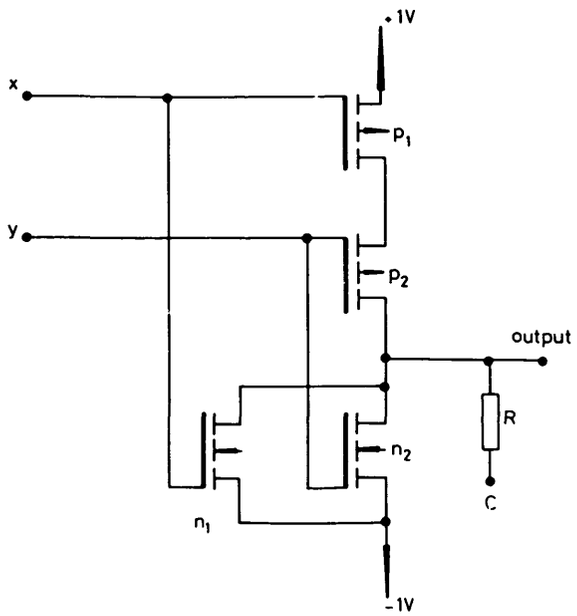

Fig. 2 *Ternary NOR gate*
$R = 25\,k\Omega$

The output of the TNOR will be always the inversion of the maximum logical value of the two inputs x and y. This output will be independent of the value of C, except when inputs x and y, are, respectively, at logical levels 1 and 1, 1 and 0 and 0 and 1. As an example, when inputs x and y are respectively at logical levels 0 and 1, transistor p_1 will be on while transistors p_2, n_1 and n_2 will be off and the output will take the value of C: 2 in the case of positive TNOR, 1 for the simple TNOR and 0 for the negative TNOR.

Similarly, a ternary NAND (TNAND) can be formed. The TNAND circuit of Fig. 3 implements the functions of the positive TNAND, the simple TNAND and the negative TNAND [1–2] which are defined by

$$\overline{(x \wedge y)^C} = \overline{\{\min(x,y)\}^C} \quad (4)$$

where $c = 1$ for the simple TNAND, 2 for the positive TNAND and 0 for the negative TNAND.

In the case of the 2-input TNAND (Fig. 3), the output is taken from two parallel p-channels connected to two series n-channels with a load resistor R, which is in turn connected to a fixed voltage C. Similar to the ternary inverter and TNOR circuits, the value of the voltage C defines the type of TNAND being implemented by this circuit and the voltage power supplies are + 1 V and − 1 V as shown in the Figure.

Finally, it should be noted that for all circuits, all p-channel substrates are connected to the positive power supply (+ 1 V), while all n-channel substrates are connected to the negative power supply (− 1 V). All circuits presented have been realised with the commercially available MC14007 CMOS integrated circuits.

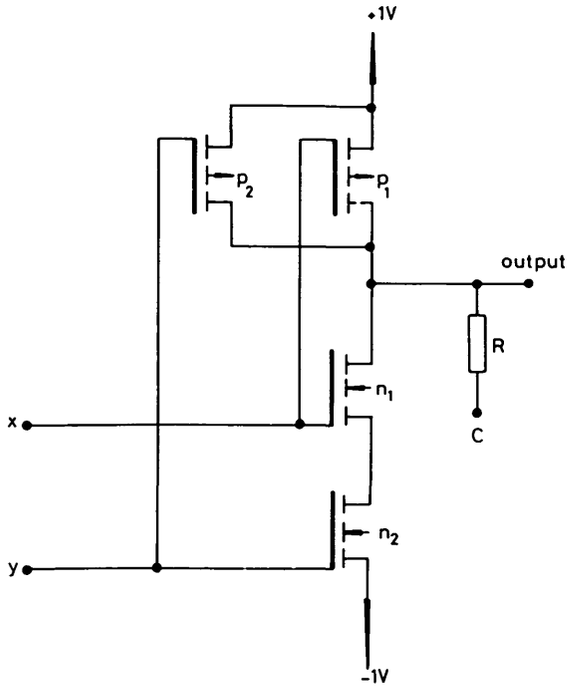

Fig. 3 *Ternary NAND gate*
$R = 25\,k\Omega$

3 Conclusions

A new family of 3-valued CMOS logic circuits that uses power supplies at below threshold voltages is presented. The new design reduces the power consumption in the circuits and shows a compromise of better performance. The basic ternary operators presented above can be used as building-block units in 3-valued digital logic systems.

4 Acknowledgments

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Book Review

Applications and design with analog integrated circuits
J. Michael Jacob

Reston Publishing Co. (Prentice Hall), 498 pp., £22.45
ISBN: 0-8359-6245-5

This is a very comprehensive and thoroughly written text on the practical application of analogue integrated citcuits. It is based on the assumption that, provided extremes of power and frequency are avoided, integrated circuits of the operational amplifier type are now the basic building blocks of analogue electronics.

The book starts with an introduction which defines the ideal operational amplifier and includes practical information on packaging, breadboarding etc. All chapters start with a defined set of objectives and conclude with a summary and very comprehensive set of (unworked) examples which, in many cases, are extensions of the wide variety of worked examples which are provided within the text.

The second chapter is devoted to the use of operational amplifiers, assumed to be ideal, in comparator and linear circuits. Chapter 3 shows how operational amplifiers may be used in regulated power supplies and leads naturally to a thorough review of available integrated circuit regulators. Switched-mode power supplies are mentioned but the treatment is sketchy and not comparable with the attention to detail in the rest of the text. The topic is perhaps beyond the scope of an already substantial work. In Chapter 4, deviations of real operational amplifiers from the previously assumed ideal are explained and used to evaluate practical performance limitations. Chapter 5 is devoted to AC amplifiers operated from a single power supply and leads naturally to a treatment of current difference (Norton) amplifiers.

Generation of pulses, ramps and sine waves is covered in Chapter 6 (using both operational amplifiers and special-purpose chips). A useful treatment of active filters is given in Chapter 7 and the book concludes with a chapter devoted to nonlinear circuits and their applications from diode function generators through logarithmic amplifiers to multipliers and variable-gain amplifiers.

In spite of the thorough analytical treatment, the text has been carefully structured in order to avoid the need for advanced mathematical concepts. Algebraic manipulation and a familiarity with trigonometrical, logarithmic and exponential functions together with complex numbers are the main requirements. Even the generation of a linear ramp is derived (Chapter 6) without specifically mentioning integration! Laplace transforms are introduced in the chapter on active filters but at a superficial level which does not require previous familiarity.

Required prior knowledge of electrical and electronic techniques is limited to basic circuit theory and a general familiarity with the properties of diodes and transistors.

Each circuit configuration is discussed in detail from basic theory through to practical consideration such as decoupling and heat sinking.

In all cases, circuits are explained and analysed with reference to readily available commercial devices (for which full data are included). It might be feared that this approach would cause the work to become rapidly obsolete. However, the devices selected are in most cases 'industry standards' and should be available, perhaps with improved specifications, for many years to come.

It is unfortunate that material on power supplies assumes 60 Hz mains. The very useful graphs relating output voltage to load current and reservoir capacitance could easily be misapplied. A correction for European editions of the book would be useful.

The advanced worker will probably find little which is new in this work, but it is an excellent text for the student of analogue circuits and should provide an invaluable reference book for the hard-pressed development engineer or technician.

There are a few typographical errors, but the reviewer did not detect any serious ones which could mislead a reader. The suggestion (p. 338) that a 2nd-order active filter could become unstable might worry students who have been taught that 2nd-order systems are inherently stable.

At £22.45, it is perhaps expensive as an undergraduate text. If a paperback version could be produced, it should be a very strong contender for recommended purchase by all electronic engineering undergraduates. It could lead to a much higher proportion of circuits which work first time!

J.C.C. NELSON