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J.H. Ting, F.E. Holmes and K.C. Smith
Department of Electrical Engineering
University of Toronto
Toronto, Ontario M5S 1A4, Canada

Introduction

This paper concerns the design and implementation of a microprocessor-based measurement and analysis system. The system is intended for use as a quality control unit for an integrated circuit processing line. It was implemented for an MOS line, but is easily adaptable to a Bipolar processing line. The unit performs a sequence of measurements on a special test pattern, which is normally fabricated along with the desired integrated circuit. The data is gathered through on-board A/D and D/A interfaces which are under software control. This data is then converted to meaningful process parameters through software written in a high level language (FORTRAN IV). If the parameters do not fall within a preset tolerance, the operator is alerted. Further testing can then be conducted through special algorithms to ascertain any problems with the IC processing line. Normal daily samples are also stored in a mass storage device to determine long term drifts in standard processor or to predict problems with the processing equipment. Since the data gathering and analysis is done automatically in real time, the system does not slow down the production line.

System Operation

The Automatic Semiconductor Parameter Measurement system (ASPM) in its operational form is incorporated into a conventional IC test system to perform additional measurements and analysis to determine important semiconductor parameters. These measurements are designed to complement the normal electrical parameter measurements done on the actual circuit. The ASPM system will operate prior to or during the wafer-sort stage. The measurements are done on a specially-designed test pattern, which is fabricated on every wafer along with the normal production devices. The test pattern consists of a capacitor of .5 mm in diameter, a resistor surrounding the capacitor, acting as a heating element for the bias-temperature stress, a diode to monitor the temperature, and resistors to determine the sheet resistance. Not all the wafers at this stage have to be tested since the semiconductor parameters are unlikely to vary greatly within a batch of wafers.

To speed up the testing process two techniques are used: selective tests and go/no-go decision making without data transformation. Selective tests implies that only a few essential measurements are made at first. If problems are indicated by these first fast tests, then the complete testing cycle can be initiated. In the standard approach, the measurements are made and then transformed into meaningful process parameters for interpretation by the human operator. Such

transformation is not necessary if the computer in the ASPM system is used to make the go/no-go decision. Information regarding the process parameters and their maximum allowable deviations can be fed to the computer, which can then find limit values for the measured data which would generate the allowable spread in process parameters. These data are stored in the computer and compared to the actual measured values to decide if problems exist on the IC processing line. If so, more complete testing with full data transformation can be used to narrow down the source of the problems.

The operating system, implemented in software, is designed to select the wafers to be tested. The algorithm for the selection involves generating a random number within a preset range. This ensures that always at least one wafer will be tested in a processing batch. The operating system is also responsible for initiating a complete test run on a sample wafer for a daily routine sample check. The data from this record contains all the measurements and analysis and is stored under the file of the day.

A complete test run takes about 20 minutes, limited mostly by the bias-temperature stress performed at 300°C with ± 55 volt bias voltage. Hence the temperature stress is normally restricted to the daily sample check and if the ASPM finds potential problems, such as a consistent shift in the flatband voltage. In the latter case, the operator will be alerted. A partial test run without the stress cycle requires less than 3 seconds.

The operator at any time can request that a partial or complete test be repeated any number of times to give a printout of the mean and extreme values. He can also request that an ideal C-V curve be superimposed on the measured one. This would enable him to visually analyze the surface state behaviour of the sample.

Measurement Theory

The system must perform resistance, capacitance and temperature measurements. The resistance and temperature data are used directly, and so require no software transformation. However, the capacitance data must be transformed, using complicated physical equations, to obtain the desired process parameters. Two sets of representative measurements were implemented, based on the MOS test capacitor structure. They are the steady state capacitance as a function of varying applied bias voltage, and both the ramp and pulse responses of capacitance as a function of time.

From the steady-state capacitance-voltage measurements, the following parameters are

obtained: 1) conductivity type, 2) oxide thickness, 3) impurity doping concentration, 4) flatband voltage, 5) flatband capacitance, 6) oxide charge Q_{ss} , and 7) behaviour of surface states. From the pulse response of the capacitance as a function of time, minority life-time and surface recombination velocity are determined. From the non-steady-state ramp response of the capacitance as a function of time, a doping profile into the silicon is mapped as a function of distance. The system can easily be expanded to include other measurements, such as surface carrier mobility.

From the slope of the capacitance versus applied bias voltage curve, the type (n/p) of the substrate impurity concentration can be determined. While other parameters are not so apparent, they can be found through analysis via the use of a set of physical equations developed over the years. Hence the oxide thickness is determined through the following equations:

$$t_{ox} = \frac{\epsilon_{ox} \epsilon_0}{C_o} \quad (1)$$

where ϵ_{ox} , ϵ_0 are constants and C_o is obtained by measurement.

The impurity doping concentration is found by solving the following transcendental equations using iteration techniques with a special convergence factor:

$$C_s = \frac{1}{C_t - \frac{1}{C_o}} \quad (2)$$

$$\frac{\frac{N_a}{N_i}}{\ln\left(\frac{N_a}{N_i}\right)} = \frac{2\phi_s \epsilon_s}{\epsilon_s \epsilon_0 q} \quad (3)$$

With the evaluated doping concentration, the ideal C(V) curve can be constructed using the following algorithm:

- Solve for U_F from $N_A = n_i e^{U_F}$, where N_A is from (3) above.
- Arbitrarily pick a value for U_s and solve for Q_t where $Q_t = -2qn_i L_d [\text{Cosh}(U_s - U_F) - \text{Cosh}(U_F) + U_s \sinh(U_F)]^{1/2}$ and U_F is from (a).
- Calculate U_g from

$$U_g = \phi_s - \frac{Q_t}{C_o}$$

where ϕ_s is a constant and Q_t is obtained from (b).

- Finally solve $C_s = \frac{\epsilon_s \epsilon_0 q (p_s - n_s - N_d - N_a)}{Q_t}$ where $p_s = n_i e^{-(U_s - U_F)}$ and $n_s = n_i e^{(U_s - U_F)}$.

By iteration, the value of C_s corresponding to the appropriate value of U_g can be found.

Similar techniques are used to transform the other measurements into process parameters.

HARDWARE The ASPM is implemented with a Z-80 based microcomputer. In the development stage, dual minifloppy drives were used in conjunction with 48K bytes of RAM. A custom design interface board with on-board 8 bit A/D converter, a digitally controlled power supply with ± 54 volt range, a reed relay switching network for routing the appropriate bias voltage and test probe inputs to the proper channel, a digitally controlled current source, a programmable gain amplifier, and a crystal controlled timer for generation of interrupts at a fixed interval (used in the transient measurements).

The main software language used was FORTRAN IV. For controlling the interface board, assembler language was used. The routine from the two languages are linked together after compilation. They also share a common storage area. In this way, the FORTRAN variables are directly assigned with the values read in by the Assembler-based routines. The use of FORTRAN IV language was necessary to allow the system to handle the complex mathematics. It also allows for easier modification of the transformation relations, should more complex equations be desired.

In the final version, the ASPM will have one mass storage device (cassette tape or a standard size floppy drive) and the resident software will be in ROM.

System Performance

The system was tested against the conventional way of making C-V and C-t measurements. The measurements have been consistent to better than $\pm 1\%$. The use of an 8 bit A/D converter is adequate since the capacitance ranges from no less than 20 pF to no more than 1000 pF. For measurements such as C-t, a software offset is automatically added such that the 8 bit A/D converter measures only a narrow segment of the total range (5-20 pF). When combined with the programmable gain feature of the input amplifier, 0.25 pF can be resolved.

Conclusion

The good performance and high operating speed of the ASPM suggests the feasibility of a permanent quality control unit for monitoring semiconductor processing parameters continuously on an IC production line. This would undoubtedly result in a better understanding of the long term drift behaviour of the production equipment and lead to tighter control of IC process variables. The unit can also be used to more accurately predict the frequency of routine cleaning and maintenance operation on the production line.