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A FAST IMAGE PROCESSOR

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ABSTRACT

The design of a versatile, fast image processor is presented. It comprises a TV camera driven by a bit slice processor. It has the ability to analyze the whole or any part of video frame in real time under software control. Various system advantages and the results of an implementation are outlined.

INTRODUCTION

Scene analysis using a TV camera is becoming an invaluable aid to computer control of many systems. Most image processors today cannot process video signals in real time and therefore preclude usage in many potential applications. The processor describe here can easily synchronize to and process an input video signal continuously. It was used to configure a man to machine interface, wherein the camera 'looked' at a key-area and determined operator actions. The overall system response was guaranteed less than 100 ms, and allowed unprecedented flexibility. In general, this image processor has been intended to lend powerful support to another slower computer executing standard software. The AMD 2900 series bit slice family was used to implement the processor and a Motorola 6844 Direct Memory Access Controller to control the data transfer.

HARDWARE FEATURES AND DETAILS

The output of the image processor is a single bit/pixel map of the video frame which can either be transferred by Direct Memory Access into the host computer or retained for further processing. The resolution possible is 512 x 512 pixels. The black-white decision threshold can be set to any of 256 grey levels by either the host or the image processor. The image processor does not have any high speed frame buffer since it uses the host computer memory to store the digitized frame. The buffer location is changeable as often as every frame access by the host computer. Figure 1 shows a block diagram of the processor.

The video signal is digitized into 'black' or 'white' using a very high speed comparator. These bits are concatenated to form bytes and stored into the host computer memory via a Direct Memory Access. DMA is possible through four channels, each being programmable by the host computer to set block length, block position,transfer direction and transfer mode (interrupt on end of transfer or re-transfer). One comparator input is derived from an 8-bit D/A converter which effectively establishes the black-white decision threshold. It is accessible to both computers and therefore the threshold can be updated continuously. Signals like vertical and horizontal sync pulses from the composite video are fed into the status register of the image processor. This results in micro-instructions like WAIT till (or branch on) start (or end) of current frame (or line). The host computer also has direct access to the writeable control store of the image processor as well as a register in the image processor microprogram sequencer. It can therefore, continuously re-write the image processor micro-code and using the address register, point to the exact routine to be executed.

The image processor CPU has an 8-bit data word, and is pipelined at two levels: the outputs of the control store, which contain the micro-instruction and the status outputs of the ALU (Carry, Negative, Zero, Ovf and four externals). The primary objective was a decrease in overall cycle time. In this scheme the microinstruction access time is overlapped with the ALU operation, thus reducing the overall cycle time.

The micro-instruction width is 40 bits with 4 bits reserved for future custom applications. The use of 4-bit slices for the microprogram sequencer imply an address space which is trivially expandable to any size. The same holds true for the data word size. Since the image processor and host computer clock rates are vastly different, and communication is totally asynchronous, steps were taken to minimize system errors: A 'mailbox' data buffer was implemented and a 8 flip flop circuit to implement a correct handshake across all four DMA channels. In the implementation, no incorrect transfer has been detected in all tests made so far.

SOFTWARE FEATURES

The instruction set of the image processor eases the software writing effort. A complete instruction set can be easily generated by referring to the processor architecture and the AMD 2900 series data book. Space limitations preclude a list here. A subroutine to digitize and fill a frame buffer assuming the transfer channel to be number 0, would consist of the following steps:

1) Synchronize to vertical sync.

   * Wait for the flyback
   * Frame will start on
   * execution of next micro-instruction

This architecture differs from all other existing organizations in that a single memory device contains all the information of a plane. To improve the z resolution (i.e., the shade of grey or colour), one is required merely to add more chips--possibly on the same board--rather than adding new boards. This expansion does not require any modification of the control unit. Furthermore, a failure of one chip does not distort the entire image.

Coordinate Transformation

The innovative transformation reduces the memory mapper to simple interconnections and results in a natural, fast refreshing scheme for the dynamic RAM. For a 64 Kbit dynamic memory, the transformation $F(\underset{\sim}{x}, \underset{\sim}{y}) = (\underset{\sim}{X}, \underset{\sim}{Y})$ is given by

$$F_1([x_0, x_1, \ldots x_7]) = [CAS_0, CAS_1, RAS_2, RAS_3, \ldots RAS_7]$$

and

$$F_2([y_0, y_1, \ldots y_7]) = [RAS_0, RAS_1, CAS_2, CAS_3, \ldots CAS_7]$$

where $\underset{\sim}{x}$, $\underset{\sim}{y}$ are the image coordinate vectors and $\underset{\sim}{X}$, $\underset{\sim}{Y}$ are intermediate vectors whose elements refer to the dynamic RAM physical coordinate vectors.

The above transformation has the following properties. Since the mapping is symmetrical, the memory mapper reduces to simple wire routing (no ROM required). The dynamic RAM is refreshed every four horizontal lines on the raster scan display and, therefore, no refresh controller sequencer is required. Since the RAS address is changed every four successive horizontal pixels, the memory sequencer (Fig. 1) can be designed so as to permit reading in the page mode.[2]

Higher resolutions such as 256 x 512, 512 x 512 can be achieved with the chip-per-plane architecture by using interleaving and interlacing. The present 64 Kbit memory devices and any larger chips could be utilized in the higher spatial resolution video RAMs.

Summary of Features

The chip-per-plane architecture allows increased z resolutions to be accomplished easily with common control logic. The innovative mapping results in natural dynamic RAM refreshing and the simplest possible memory mapper. The time-slice sequencer enables random access to any pixel by the external computer. The overall design of the video RAM, has, therefore, enhanced reliability and maintainability.

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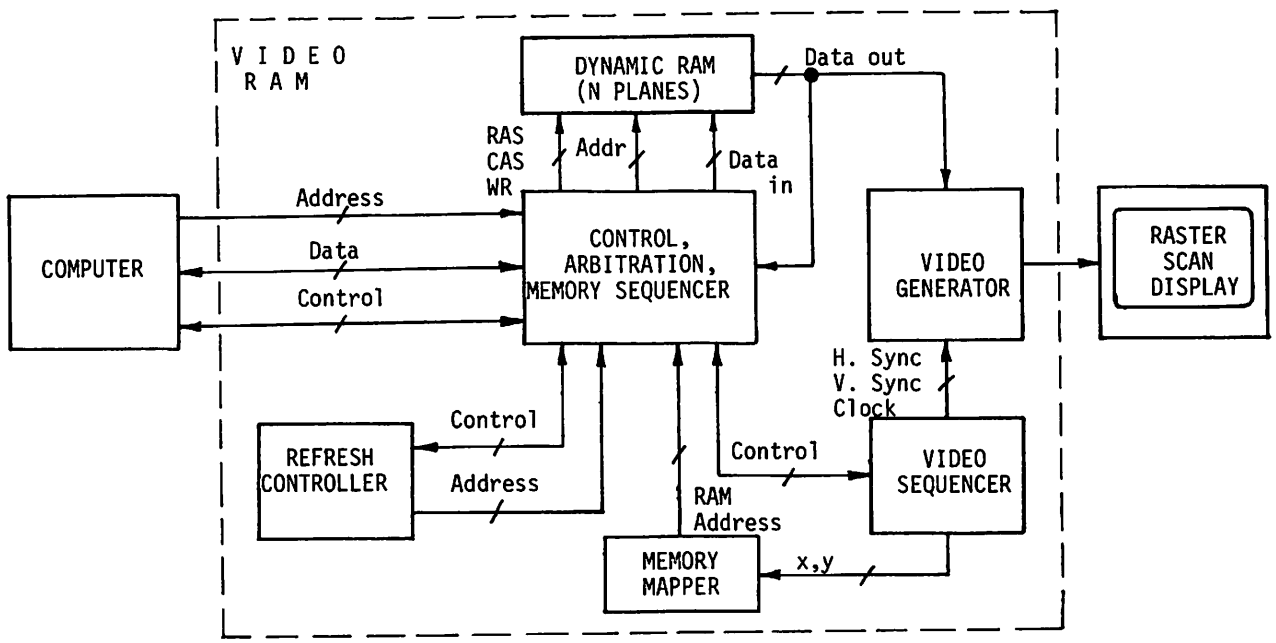

Fig. 1: General video RAM organization