Analog Integrated Circuits and Signal Processing 2, 117-130 (1992)

Real-Time Edge Detection and Image Segmentation

C.P. CHONG, C.A.T. SALAMA, AND K.C. SMITH
Department of Electrical Engineering, University of Toronto, Toronto, Ontario, Canada M5S 1A4

Received June 11, 1991; Revised December 11, 1991.

Abstract. The implementation of real-time edge detection and image segmentation using analog VLSI is described. A novel technique of image segmentation using radially propagating signals is discussed. Current-mode processing is used to avoid offset voltages and lead to circuit implementations which are compatible with standard CMOS processes. A system using raylike signal propagation and implemented using 3μ-CMOS technology is described together with experimental results.

1. Introduction

Edge detection and image segmentation are important image-processing steps which must precede image velocity computation [1], [2], pattern recognition, binocular stereo vision, optical flow computation, and shape-from-texture extraction [3]. Edge detection in digital image processing is equivalent to high-pass filtering. Effective algorithms which are complex and computationally intensive can be implemented relatively easily on digital processors. However, to process the digital image, sequential image digitization must be performed, and parallel processing is limited. Moreover, each processing module has to be executed sequentially [4]. On the other hand, analog parallel processors are highly specialized and are less flexible [5]. Implementations of known algorithms are difficult due to the unavailability of suitable analog circuit building blocks. However, analog processing techniques offer the possibility of highly parallel processing [6]. This is because no A/D converter is required, and an analog processor, which occupies only a fraction of the area occupied by its digital counterpart, can be integrated with each signal source, without leading to impractically low pixel density. Imagers with medium pixel density find applications in, for example, manufactured-part recognition and collision avoidance between two moving robots.

In digital image processing, the important design criteria for the edge-detecting module are reliability and speed [7]. A reliable edge-detecting module is able to detect edges of images with different contrast or background texture. The resolution of the image processed is independent of the algorithm used and is controlled by the pixel density of the imager: the higher the pixel density, the slower the edge-detection process. On the other hand, the pixel density of an analog edge-detecting imager is highly dependent on the degree of sophistication and reliability of the edge-detecting technique used. Since the analog edge-detecting imager is highly parallel, the speed of computation is relatively independent of the pixel density.

Some image edges are not well defined [8], because intensity fluctuates from pixel to pixel, and image boundaries cannot be defined based on uniform intensity of pixels within a particular region. To extract this type of edge, the average intensity of a few adjacent pixels must be used. The application of analog edge-detection techniques [9] in this area is very promising; however, methods of reducing pixel size and the offset voltages in the edge detector are required.

In the real world, well-defined image edges are very common. Objects such as robots and motor vehicles have a well-defined boundary, and edge detection is easier. Earlier attempts to perform image contour extraction using analog circuit techniques were very similar to their digital counterparts [10]. Discrete time sample systems are used, and processing is performed after the outputs of the pixels are sampled and stored in analog form on an S/H circuit. However, the sequential nature of the data generation severely limits the parallel-processing capability of the next module.

To exploit fully the parallel-processing capabilities of analog processing techniques, the edge-detection process must be performed locally. Moreover, the size of the edge detector must occupy a small area so that

when other processing circuits (such as those performing image segmentation or image velocity computation [1], [2]) are integrated with it the resulting pixel density is not impractically low. This paper describes work leading to the implementation of a viable edge-detection and image segmentation system on silicon. Current-mode signal processing is used to avoid the large output offset voltage associated with a voltage-mode circuit. While current mismatch and voltage offset are related, the problem caused by a current mismatch in a current-mode circuit is potentially less than that in a voltage-mode circuit. For example, a 1% current mismatch may cause the voltage of an output node (of, for example, the op amp) with a high node impedance to saturate at supply-rail voltage. However, if current-mode signal processing is used, the 1% mismatch will produce an error of only 1%.

2. Edge Detection Using Analog VLSI Technique

2.1. Basic Theory

Generally, analog circuits with high accuracy are more sensitive to process parameter variations and are less suitable for analog VLSI implementation where a circuit may be duplicated many times on the chip. A relatively accurate current-mode circuit building block is the current mirror. In general, minimum size MOSFETs used to implement the current mirror result in a current duplicating accuracy of better than 10% (standard deviation) [11]. While this figure may not be impressive for high-precision analog circuit design, it is within the acceptable range suitable for analog VLSI image processing (see Section 2.2).

To perform edge detection, the average of the outputs of neighboring pixels must be computed as shown in figure 1. Since no feedback exists between pixels, the network is stable. The general formula for edge detection is

$$I'_o = I_a - \frac{1}{N}\{I_1 + I_2 + \cdots + I_N\} \qquad (1)$$

where I'_o is the output signal of the edge detector, I_a is the locally generated activation signal, and I_1 to I_N are the inhibition signals generated by neighboring pixels. The activation and inhibition signals of a pixel can be derived directly from the photogeneration current of the local pixel. However, to produce a smoother I'_o function, the activation and the inhibition currents

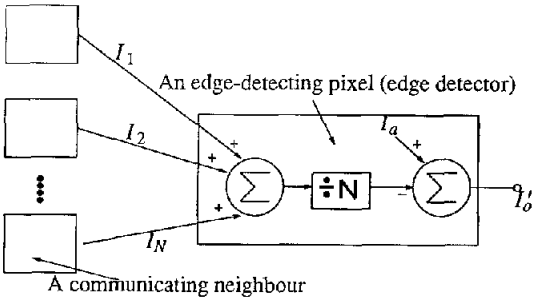


Fig. 1. Edge-detection process performed by a pixel.

should be the average of the photogeneration currents of the local pixel and a fixed number of neighboring pixels. The larger the numbers of neighboring pixels used in the averaging process, the smoother is the I'_o function.

In this paper, we consider only the case where the activation and inhibition currents are derived from local photogeneration currents only. Smoothing the I'_o function by using the spatially averaged photogeneration current requires more complex circuits which need to be optimized in terms of transistor count and area (see Appendix A).

While equation (1) can be implemented directly using current mirrors, the output current generated is low because the activation current and the inhibition currents are in the nanoampere or subnanoampere range. A better method of edge detection is based on the equation

$$I_o = N\,I'_o = N\,I_a - \{I_1 + I_2 + \cdots + I_N\} \qquad (2)$$

Note that equation (2) is derived from equation (1) by multiplying equation (1) by N. Thus, the output current expressed by equation (2) is N times larger than that expressed by equation (1).

A current-mirror-based circuit implementing equation (2) is shown in figure 2. The photodiode generates an output current I_{ph}. This current is duplicated by N p-MOSFETs, p_1 to p_N, to generate N inhibition currents to be supplied to the neighboring pixels. The

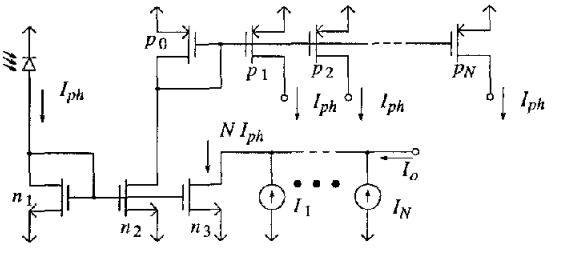


Fig. 2. Schematic of the edge detector.

activation current, which is N times the photogeneration current I_{ph}, is generated by n_3. Inhibition currents, I_1 to I_N, supplied by the neighboring pixels are fed to the drain of n_3. The resultant current flowing into the drain of n_3 is taken to be the output current I_o.

Two photodiodes located on the bright and the dark sides of the image edge are shown in figure 3. Photodiode A, located on the bright side of the image edge, generates a current I_b, and photodiode B, located on the dark side of the image edge, generates a current I_d. The sharpness of the image edge is defined as

$$E_S = \frac{I_d}{I_b} \tag{3}$$

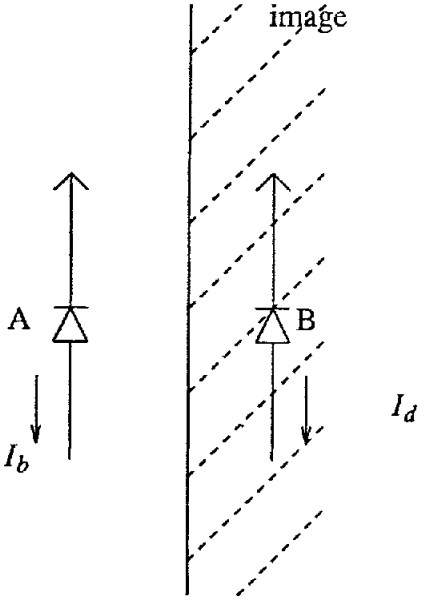


Fig. 3. Two photodiodes located on the bright and the dark sides of an image edge.

The quantity E_s will be used in the characterization of the edge-detecting imager.

The pixel containing either photodiode A or photodiode B can be used to encode the presence of an image edge. Here, the pixel containing photodiode A is chosen. For this case, the condition for the detection of an image edge is

$$I_o > 0 \tag{4}$$

where I_o is given by equation (2). No image edge is present if

$$I_o \leq 0 \tag{5}$$

2.2. *The Effect of a Current Mismatch*

Practically, the current mirror does not duplicate current with perfect accuracy. This may lead to undesirable effects in high-precision analog circuit design; however, in the implementation of the edge detector, the current mismatch has a desirable effect if the magnitude of mismatch is not too large. Referring to the schematic in figure 2, if the illumination is uniform over the surface of the edge-detecting imager, all photogeneration currents are ideally equal. This implies that the activation current in each pixel cancels exactly the inhibition currents supplied by neighboring pixels. Thus, the output current of each pixel is zero and susceptible to noise. This problem can be solved easily by making the inhibition current slightly larger than I_{ph}. In this case, condition (5) is easily met when the surface of the edge-detecting imager is evenly illuminated.

The inhibition currents generated by p_1 to p_N in figure 2 have a desirable systematic offset current greater than zero. This is due to the fact that an inhibition current is duplicated twice before it is supplied to a neighboring pixel. The drain-to-gate voltage of n_2 is much higher than that of n_1, and, thus, the drain current of n_2 will be higher than that of n_1.

The maximum current mismatch allowed is a function of the sharpness of the image edge and the number of communicating pixels. To simplify our discussion, the activation current is assumed to be exactly NI_{ph} and the inhibition current is $(1 + \epsilon_I)I_{ph}$, where ϵ_I is a constant greater than zero. If the image edge is well defined, the smoothness of the function I_o is not critical. Therefore, a pixel does not have to communicate with a large number of its neighbors. Rather, the reliability of the edge detector is more important. For the pixel to detect an edge with sharpness of E_s, it can be shown that ϵ_I should satisfy the condition (see Appendix B)

$$\epsilon_I \leq \frac{(m/N)(1 - E_S)}{1 - (m/N)(1 - E_S)} \tag{6}$$

where N is the total number of communicating pixels and m is the number of communicating pixels located on the dark side of the image edge.

To detect an image edge of any orientation, a pixel should communicate with at least four neighboring pixels. Figure 4 shows a pixel communicating with (a) four neighboring pixels and (b) eight neighboring pixels. For case (a), the possible values of m/N are 1/4 and 1/2, and for case (b) possible m/N values are 1/8,

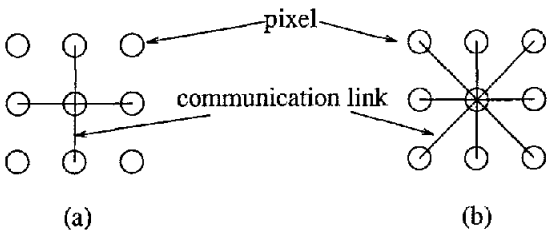


Fig. 4. A pixel communicates with (a) four neighbors and (b) eight neighbors.

1/4, 3/8, and 1/2. A plot of ϵ_I versus E_s with m/N as a parameter is shown in figure 5. From the plot we may conclude that as $E_s \rightarrow 1$ (image with low contrast), the accuracy of current matching becomes critically important. If $E_s \ll 1$, a lower value of m/N requires a lower ϵ_I. For example, consider a 10% current mismatch. For $N = 4$, the worst case is $m/N = 1/4$, and from the plot in figure 5 a 10% current mismatch requires $E_s < 0.7$. For $N = 8$, the worst case is $m/N = 1/8$, and from the same plot the same level of current mismatch requires $E_s < 0.3$. It follows that if the image edge is well defined, the optimal case is the one with four communicating pixels.

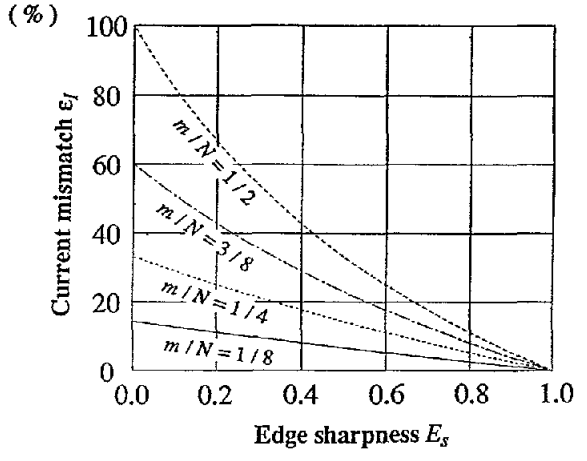
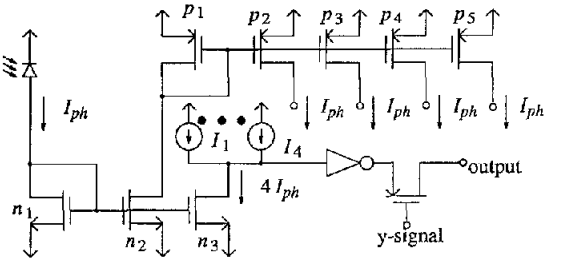


Fig. 5. Upper bound of current-matching error as a function of edge sharpness.

2.3 Silicon Implementation and Experimental Results

An edge-detecting imager using the edge-detector circuit shown in figure 6 has been implemented using standard 3μ-CMOS technology. Instead of sampling the output current of the edge detector directly, an inverter is added to the output. If an image edge is detected, the output voltage of the inverter is high. The total area



I_1 to I_4 are the inhibition currents supplied by neighbouring pixels.

Fig. 6. Circuit of the edge detector used in the CMOS implementation.

of the pixel is 147 μm by 157.5 μm or 0.023 mm^2. This leads to a pixel density of 43 pixels/mm^2, which is about two orders of magnitude lower than that of the state-of-the-art CCD imager [12]. However, for most real-time image-processing applications, such as manufactured-part recognition and collision avoidance between moving robots, pixel density as high as that achievable by CCD imagers is not required.

The architecture of the edge-detecting imager is shown in figure 7. The array size is 23 by 23 or 529 pixels. The y-signal for turning on the switch in series with the output of the pixel is supplied by the y-shift register. The clock signal that drives the y-shift register is supplied to an off-chip counter which generates a linear digital ramp for an off-chip D/A converter. The output of the D/A converter supplies the y-sweeping signal for the CRT display. The x-shift register controls the multiplexers (MUX), which are turned on one at a time by connecting the output of the pixel being sampled to the external pin. The MUX is a tristate inverter, as shown in figure 8. Thus, an image edge is detected if the output of the edge-detecting imager is low; otherwise, the output of the imager stays high. The output of the edge-detecting imager can be used to control the density of the electron beam in a CRT display. The clock signal supplied to the x-shift register is also supplied to the circuit which generates the x-sweeping signal for the CRT display. The static power dissipation of the edge-detecting imager is less than 40 μW.

A micrograph of the edge-detecting imager is shown in figure 9. The small square inset shows an expanded view of a pixel. The total area of the imager, including the pads, is 20.34 mm^2. Most of the pixel area is covered by the second-layer metal except for the photodiode.

For a circular image projected onto the edge detecting imager, the output of the imager in the form of a 2D pattern on the CRT display is shown on figure 10. The dark spots indicate the presence of image edges. However, since the edge threshold is not controllable

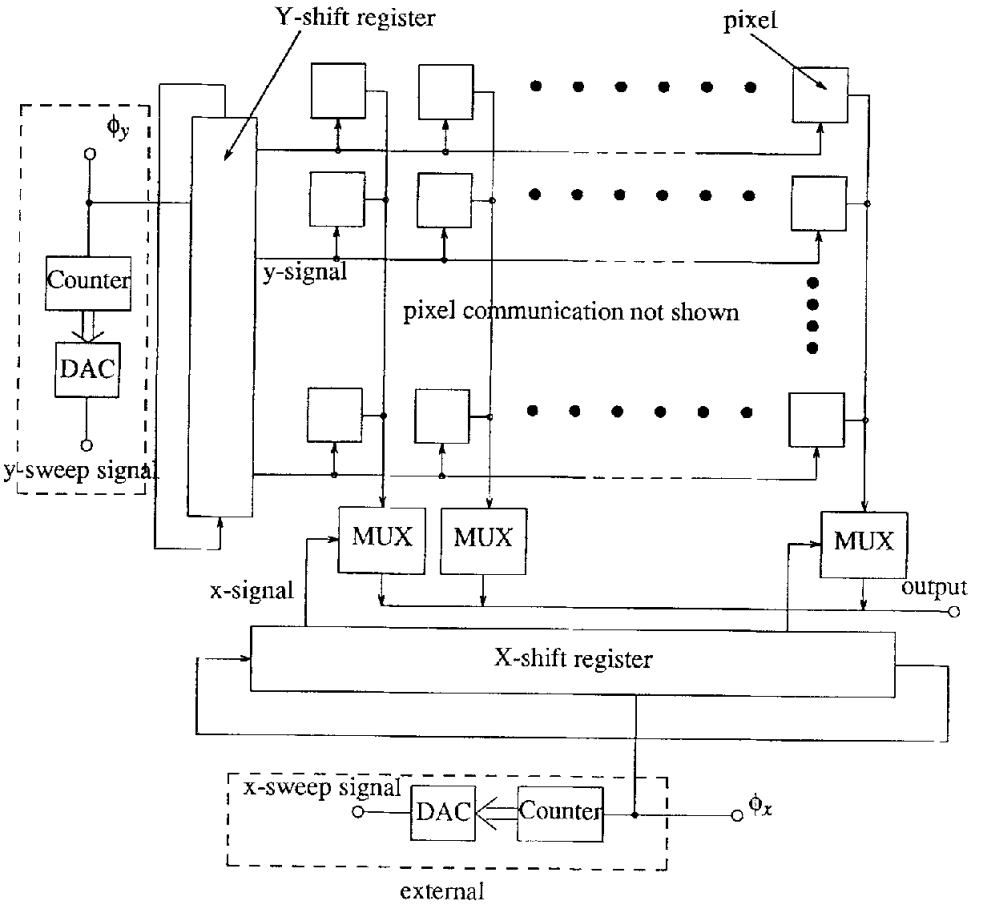


Fig. 7. Architecture of the edge-detecting imager.

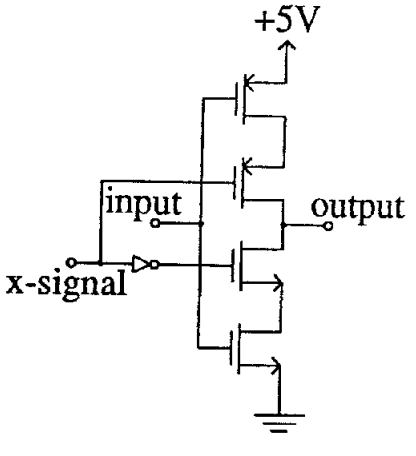


Fig. 8. Schematic of the multiplexor (MUX).

externally, spurious image edges are found both inside and outside the image boundary. (The images used are created by shining light through holes cut out of hardboards. However, the spatially uneven intensity of light produced by the light source used, creates "false edges.") The image can be cleaned up easily by adding a threshold control circuit to each pixel. Since the spurious image edges are discontinuous, they will not block the signal propagation required for image segmentation, which will be discussed in the following sections.

When an image edge of $E_s = 0.01$ ($I_d = 100$ pA) is presented to a pixel (at $t = 0$), the output voltage of the pixel is shown in figure 11 (multiple traces are due to noise interference from the stepper motor which moves the image). As shown, the delay of the output voltage of the pixel is approximately 0.8 ms. If the image contrast is high (E_s is low), the photogeneration current of the photodiodes located on the dark side of the image edge is low. Consequently, the sum of the inhibition currents, $I_1, \ldots, I_N$, supplied to the pixel located on the bright side of the image edge will also be low. According to equation (2), this leads to a higher I_o for the pixels located on the bright side of the image edge (which encode the image edge). As a result,

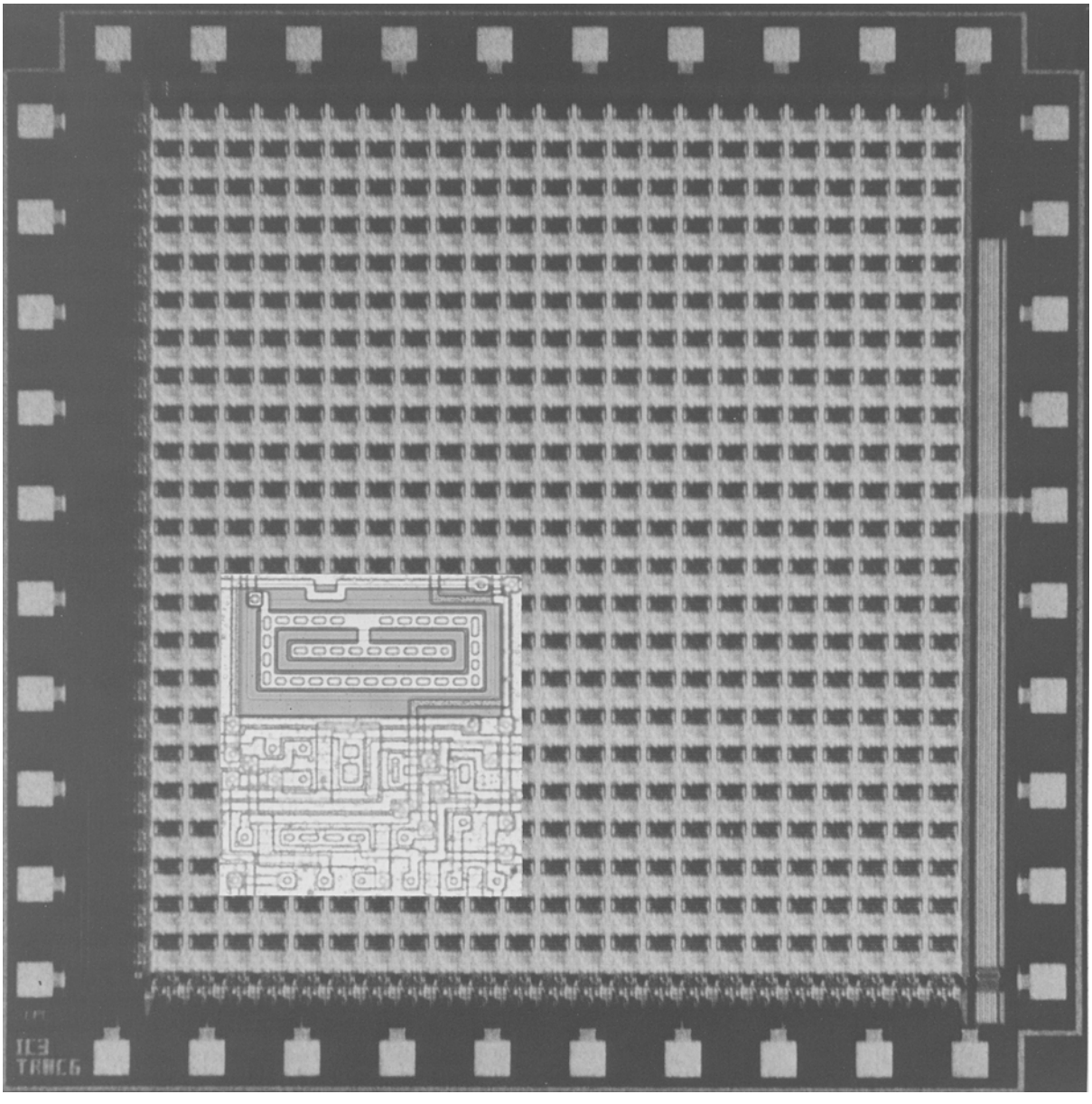


Fig. 9. Micrograph of the edge-detecting imager. The small square inset shows an expanded view of a pixel.

a larger output current is available to charge the output node in a shorter time. Thus, as $E_s \rightarrow 1$, the delay of the output voltage increases. Thus, for a given edge sharpness, there exists a maximum image velocity where the edge-detecting imager fails to detect image edges. The maximum image velocity allowed decreases as $E_s \rightarrow 1$. This is illustrated by figure 12. As shown, the maximum velocity allowed deteriorates rapidly when $E_s > 0.005$. Further work is required to improve the response time of the edge-detecting pixel.

3. Image Segmentation Using Analog VLSI

3.1. Basic Theory

Using digital techniques, image segmentation can be performed only after edge detection. Analog VLSI techniques allow these two steps to be performed in parallel, as discussed in the following paragraphs.

A novel technique for image segmentation that uses signals propagating radially out of a point source,

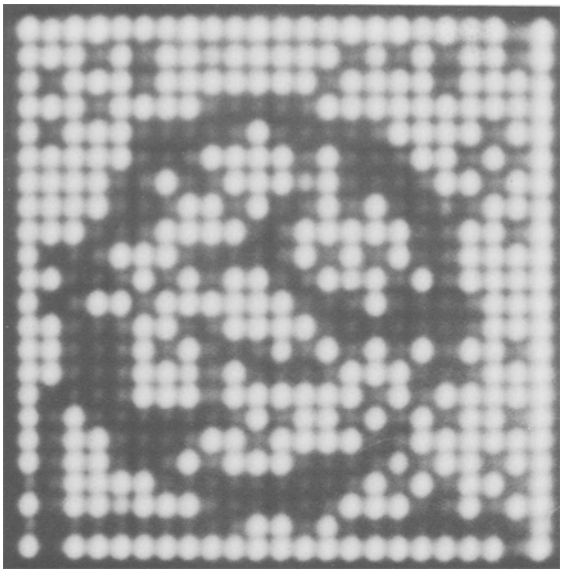


Fig. 10. Output pattern of the edge-detecting imager when a circular image is projected onto the imager.

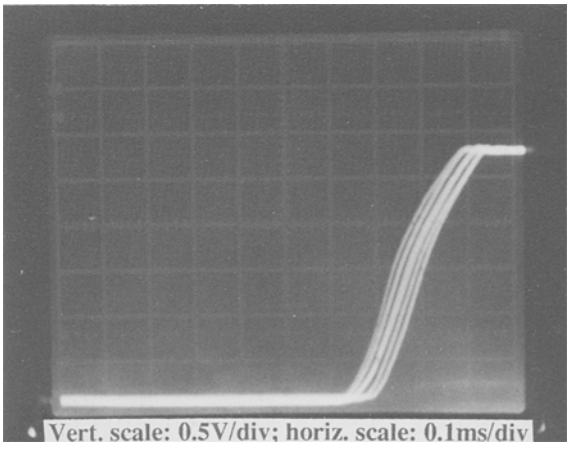


Fig. 11. Output voltage of an edge detector when an image edge of $E_S = 0.01$ is projected onto it.

known as the point of emission, is reported here. In actual implementation, only one point of emission is used. Thus, only one image at a time can be selected. While multiple points of emission may be used, in most envisioned applications (e.g., image velocity computation), only one point of emission is required. Whenever these signals reach a pixel, the pixel will be activated to perform its processing function, which may be as simple as allowing the output of the photosensor to be sampled. However, these signals are destroyed if they reach the pixels encoding the image edge. In this way, only pixels located inside a continuous image boundary,

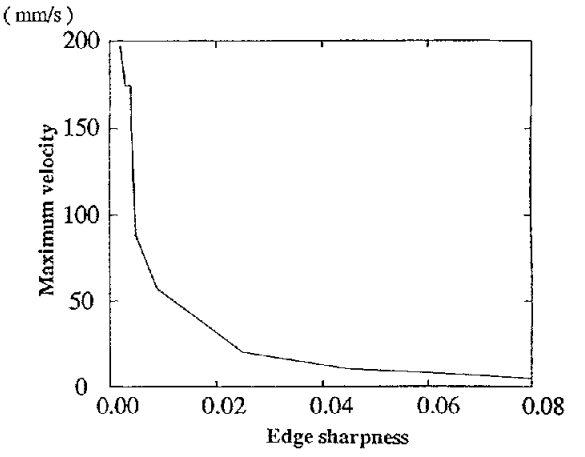


Fig. 12. Maximum velocity allowed before edge detection failed versus the edge sharpness.

which contains the point of emission, are activated, and pixels located outside the image boundary are deactivated. Since the edge-detection and the image-segmentation processes are relatively independent of each other (except at the image boundary), they can be performed in parallel. The novel segmentation technique, in a fundamental way, resembles the region-growing technique used in digital image segmentation [8].

The image segmentation process is shown in figure 13a. The point of emission is inside an image with a continuous boundary, and the signals are contained inside the image boundary. If the edge-detection process fails to produce a continuous image boundary due to a high edge threshold as shown in figure 13b, the signals will propagate to the image edge and be received by a special pixel which indicates the failure of the edge-detection process. Negative feedback can be used to reduce the edge threshold until the image segmentation process is performed successfully.

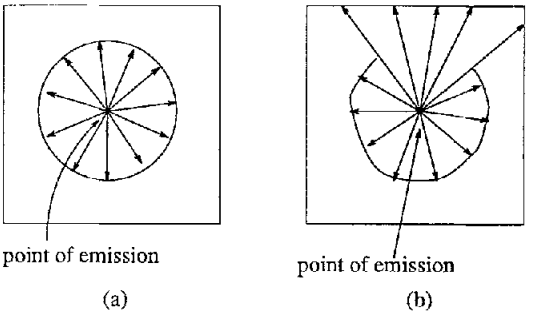


Fig. 13. Segmentation of image with (a) continuous boundary and (b) incomplete boundary.

3.2. Possible Modes of Signal Propagation and Network Stability

There are at least two possible modes of signal propagation. In one mode the signals propagate in a raylike manner; in the other mode, the signals propagate in a gaseous manner.[1] The raylike signal propagation, which has been used in maze-solving neural processor [13], is used here in the actual implementation of the image-segmenting imager.

If the raylike signal propagation is used, the network is unconditionally stable. This is because the network operates in the feedforward mode and no local feedback loop exists. Figure 14a illustrates a network using raylike signal propagation. The disadvantage of raylike signal propagation is the formation of shadows inside the image boundary if a discontinuous boundary exists inside the image boundary, as shown in figure 14b.

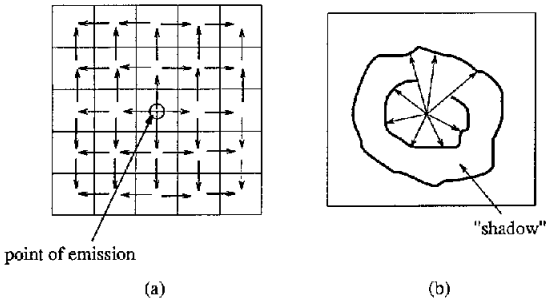


Fig. 14. (a) Propagation of raylike signals and (b) the formation of shadows inside the image boundary.

To avoid the formation of shadows inside the image boundary, the gaseous signal propagation shown in figure 15a must be used. If a discontinuous image boundary exists, the signals may propagate sideways to reach the pixels in the shadow, as shown in figure 15b. However, for the signals to propagate in a gaseous manner, bidirectional cross-border communication as shown in figure 15a is required. This leads to positive feedback between pixels, and the network may become unstable.

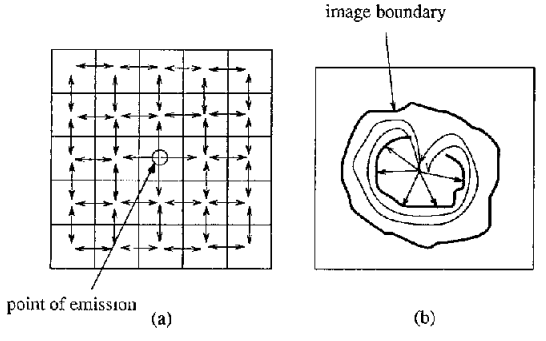


Fig. 15. (a) Propagation of gaseous signals, and (b) no shadow is formed inside the image boundary.

Since minimum-size MOSFETs are used, the capacitive components of the network are low and can be neglected. A simplified model for pixel communication is shown in figure 16. Each pixel generates a voltage denoted by v_{s1} or v_{s2} as shown in figure 16. The output resistances of the voltage sources generating v_{s1} and v_{s2} are equal and are denoted by R. The node voltage v_a of the communication link between the two pixels is given by

$$v_a = \frac{1}{2}(v_{s1} + v_{s2}) \tag{7}$$

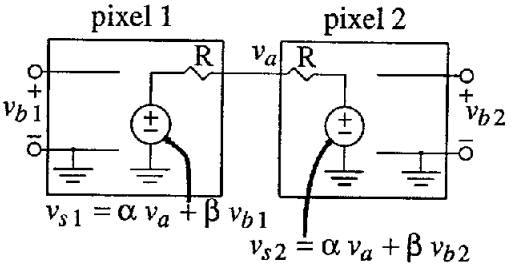


Fig. 16. Equivalent circuit that models the communication between two pixels.

The voltage v_{s1} (or v_{s2}) consists of two components $\alpha v_a + \beta v_{b1}$ (or $\alpha v_a + \beta v_{b2}$). The term αv_a, where α is a constant, models the positive feedback that exists between the two pixels. For the βv_{b1} term (or βv_{b2}), β is a constant, and v_{b1} (or v_{b2}) is a voltage generated by the communication between the pixel and its other neighbors. The actual values of α and β are determined by the circuit used and are functions of circuit parameters, such as output resistance, intrinsic gain (not including the loading effect), and any resistive components used in the feedback loop.

Substituting $v_{s1} = \alpha v_a + \beta v_{b1}$ and $v_{s2} = \alpha v_a + \beta v_{b2}$ into equation (7) leads to

$$v_a = \frac{\beta(v_{b1} + v_{b2})}{2(1 - \alpha)} \tag{8}$$

To prevent regenerative effect between pixels, α must be smaller than 1.

3.3. Silicon Implementation and Experimental Results

The circuit in figure 17a implements raylike propagation of signals. Voltage v_s is the signal that propagates

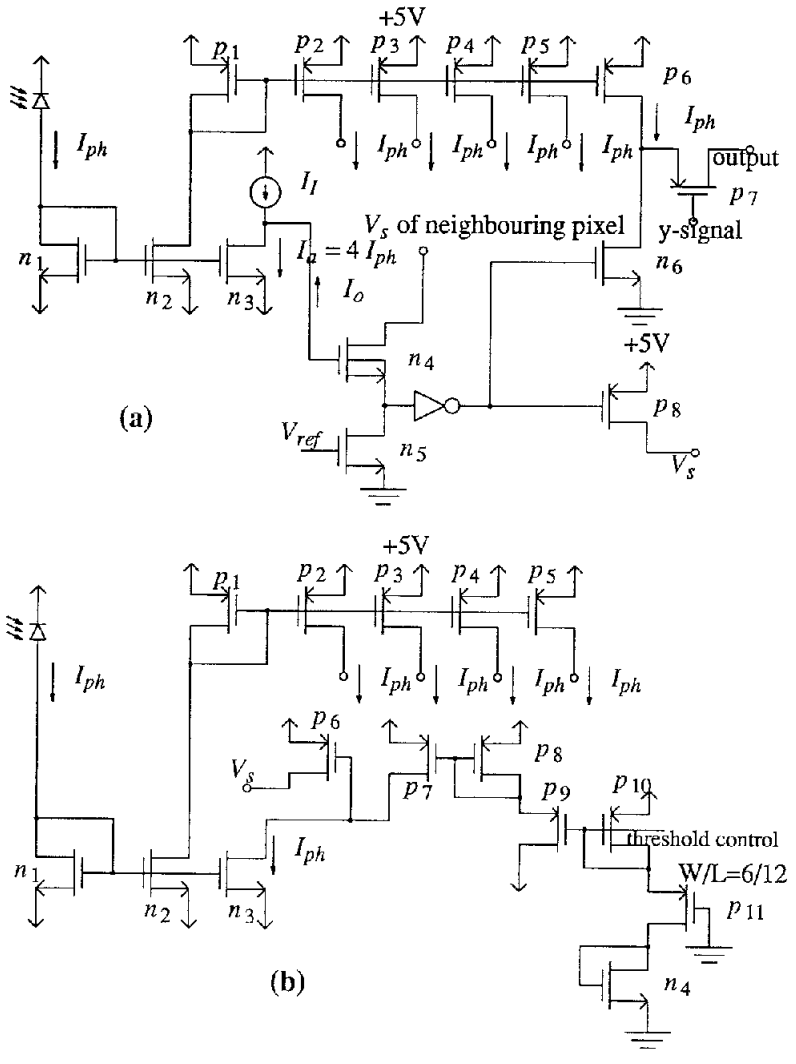


Fig. 17. Circuits of (a) the pixel and (b) the point of emission.

form one pixel to the others. Note that the signal v_s of a pixel will go high only if the signal generated by the communicating neighboring pixel goes high and an image edge is not detected. If an edge is present, n_4 will be off and the signal v_s of the pixel will stay low and cut off the signal propagation to another pixel. While there are 25 different pixels on the image-segmenting imager, they are simple variations of the circuit in figure 17a. For example, if a pixel communicates with only two other neighbors, then only two MOSFETs (instead of four are used to generate the inhibition currents.

A 3μ-CMOS p-well process was used to fabricate the imager. The p-well of n_4 in figure 17a is connected to the source. If n_5 is turned off, the reverse-bias saturation current of the junction between p-well and substrate charges the input node of the inverter to a logic-high level. This turns on p_8 and turns off n_6, disregarding the result of the edge-detection process. Thus, a simple means for turning off the effect of the edge-detection process is provided.

The schematic of the point of emission is shown in figure 17b. Inhibition currents for the neighboring pixels are supplied by p_2 to p_5. The signal v_s is provided by p_6. However, for the signal to propagate out of the point of emission, the photogeneration current, and thus the brightness of the image, has to be higher than a level controlled by the drain current of p_7. P_{II} is used as a resistor. By injecting a small current into the drain of n_3 allows the segmentation process to be stopped when no image is projected onto the imager and the entire surface of the imager is dark.

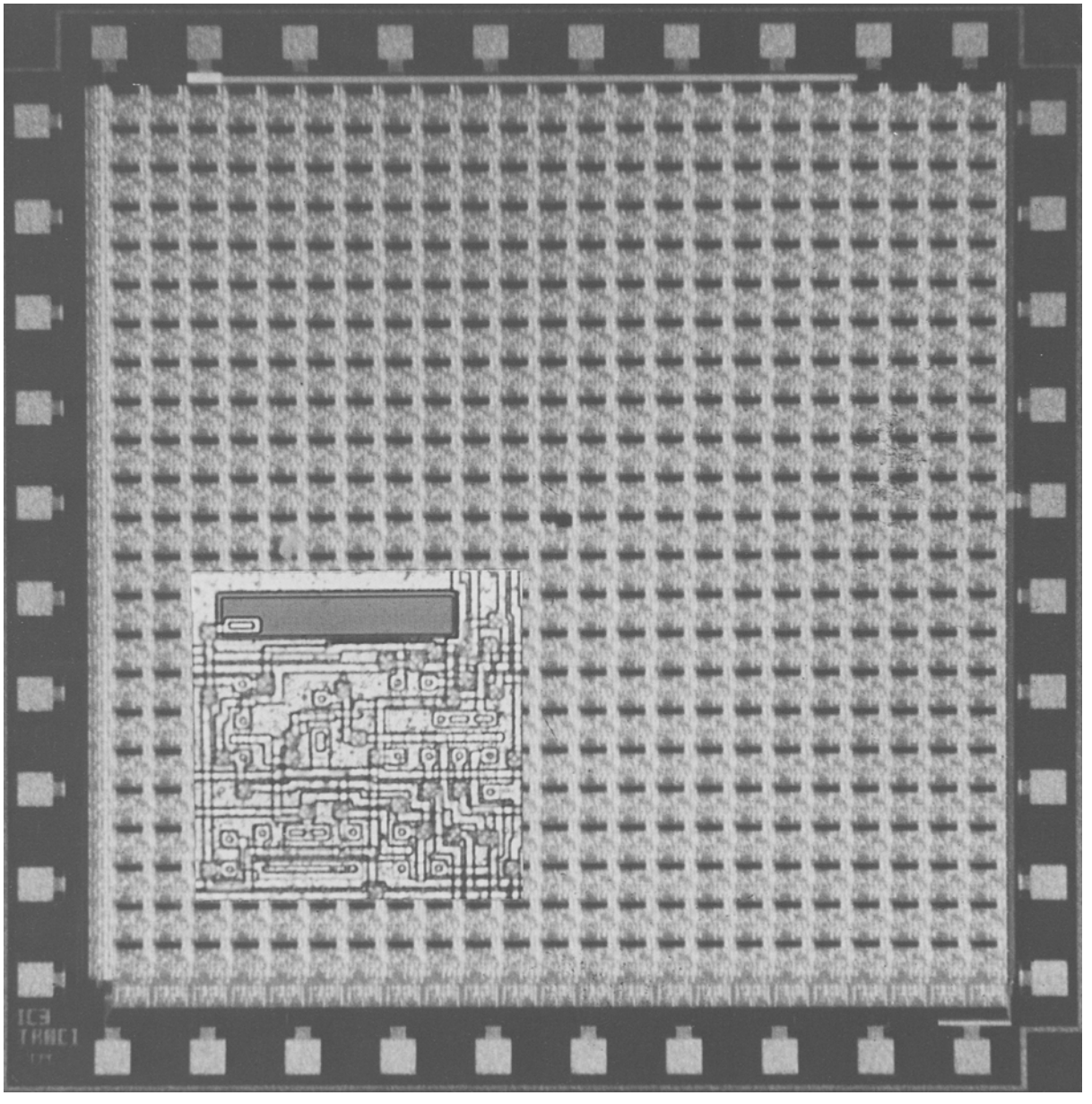


Fig. 18. Micrograph of the image-segmenting imager.

The micrograph of the image-segmenting imager is shown in figure 18. The smaller square shows an expanded view of a pixel. The array size is 23 by 23 or 529 pixels. The pixel size is 162 μm by 162 μm or 10.026 mm^2 which leads to a pixel density of 38 pixels/mm^2. Similar to the case of the edge-detecting imager, the output of each pixel can be sampled individually and displayed as a 2D pattern on the oscilloscope. The static power dissipation of the image-segmenting imager is 211 μW.

Two irregular-shaped images with continuous nonoverlapping image boundaries are projected onto the image-segmenting imager. One image is located at the center of the imager, and the point of emission is located inside the image boundary. The other image is located at the lower left corner of the imager. When the edge detection is turned off by setting V_{ref} in figure 17a to zero, the output pattern of the imager is illustrated in figure 19a. As shown, both images are clearly visible and no offset is detected. When edge detection is

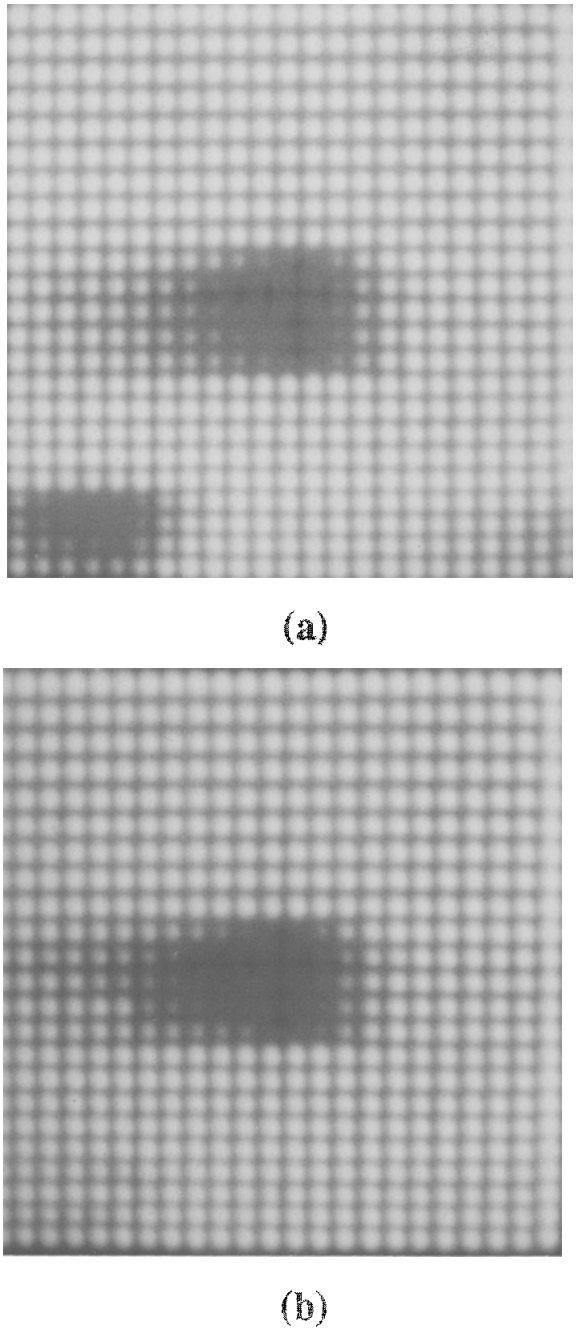


Fig. 19. Output patterns of the image-segmenting imager when (a) edge-detection process is disabled and (b) edge-detection process is enabled.

turned on by setting V_{ref} to an appropriate value (V_{ref} = 0.9 V), the output pattern of the imager is shown in figure 19b. Only the image that contains the point of emission is clearly visible, and the other image has completely disappeared.

Since the simple inverter is a much faster circuit than the edge detector, the image-segmentation process is much faster than the edge-detection process. Thus, the speed of the image-segmenting imager is limited by the slow edge-detection process, and the maximum image velocity versus edge sharpness plotted in figure 12 is also applicable to the image-segmenting imager.

4. Conclusion

This paper has demonstrated the feasibility of using analog VLSI techniques to perform real-time edge detection and image segmentation. The pixel densities achieved are 43 pixels/mm^2 and 38 pixels/mm^2 for the edge-detecting and image-segmenting imagers, respectively. Improvements in reliability, speed of computation, and pixel density are needed to make these imagers viable for large-scale implementation.

Appendix A: Edge Detection Using Spatially Averaged Photogeneration Current

Consider the case of a pixel (x, y) shown in figure A1 surrounded by pixels $(x - 1, y)$, $(x + 1, y)$, $(x, y + 1)$, and $(x, y - 1)$, where x and y are the coordinates of the position of the pixels. The local activation current can be expressed as

$$I_a(x, y) = 4\{I_{ph}(x, y) + I_{ph}(x + 1, y) + I_{ph}(x - 1, y) + I_{ph}(x, y + 1) + I_{ph}(x, y - 1)\} \quad \text{(A1)}$$

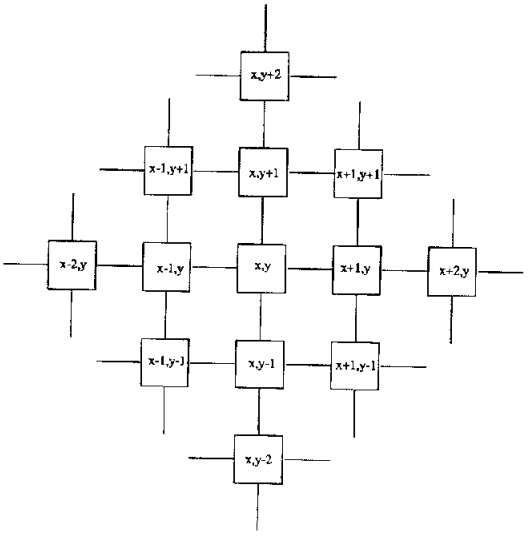


Fig. A1. A pixel (x, y) communicates with four neighboring pixels.

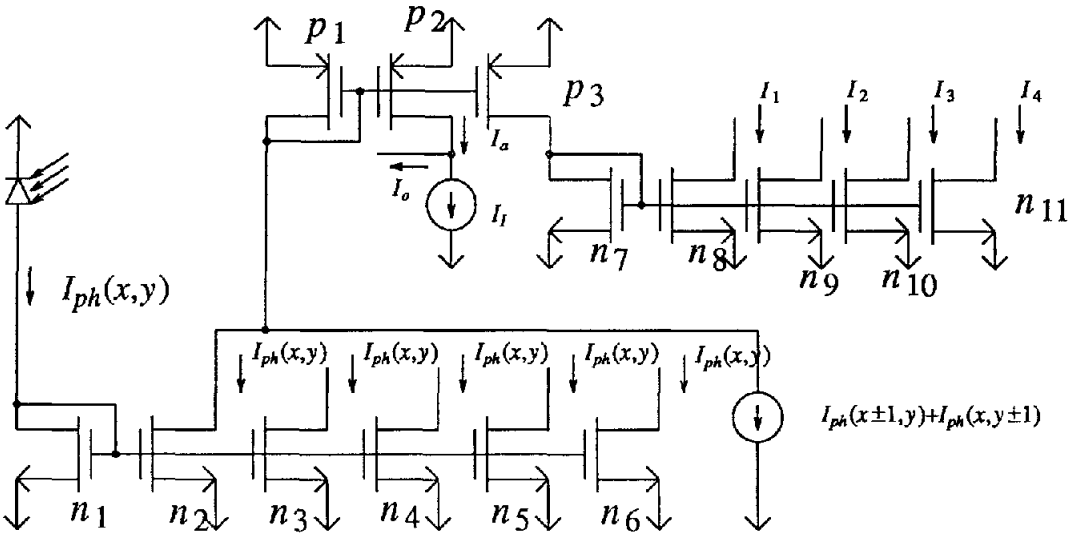


Fig. A2. Schematic of the edge detector that uses spatially averaged photogeneration currents in the edge-detection process.

The inhibition current supplied by the pixel (x, y) to its neighboring pixels is

$$I_{1,4}(x, y) = I_{ph}(x, y) + I_{ph}(x + 1, y) + I_{ph}(x - 1, y) + I_{ph}(x, y + 1) + I_{ph}(x, y - 1) \quad \text{(A2)}$$

Using equation (A2) the local inhibition current can be shown to be

$$I_I(x, y) = I_{1,4}(x, y + 1) + I_{1,4}(x, y - 1) + I_{1,4}(x + 1, y) + I_{1,4}(x - 1, y)$$

$$= 4I_{ph}(x, y) + 2I_{ph}(x \pm 1, y \pm 1) + I_{ph}(x \pm 2, y) + I_{ph}(x \pm 1, y) + I_{ph}(x, y \pm 2) + I_{ph}(x, y \pm 1) \quad \text{(A3)}$$

An edge detector using equations (A1) and (A3) is shown in figure A2.

Appendix B: The Relationship between Current Mismatches and Edge Sharpness

Let N be the total number of communicating neighbors of a particular pixel encoding an image edge. Out of N communicating neighbors, m of them are located on the dark side of the image edge. Let the photosensors located on the bright side of the image edge generate photocurrents I_b; then the photosensors located on the dark side of the image edge generate photocurrents E_sI_b, where E_s is the edge sharpness.

Interpixel communication is shown in figure B1. A mismatch factor of $1 + \epsilon_I$ between inhibition and activation currents within a pixel is assumed. Using equation (2) leads to

$$I_o = N I_b - (1 + \epsilon_I)\{m E_s I_b + (N - m) I_b\} \quad \text{(B1)}$$

For the pixel to encode the image edge, I_o must be larger than zero; thus,

$$\epsilon_I < \frac{(m/N)(1 - E_s)}{1 - (m/N)(1 - E_s)} \quad \text{(B2)}$$

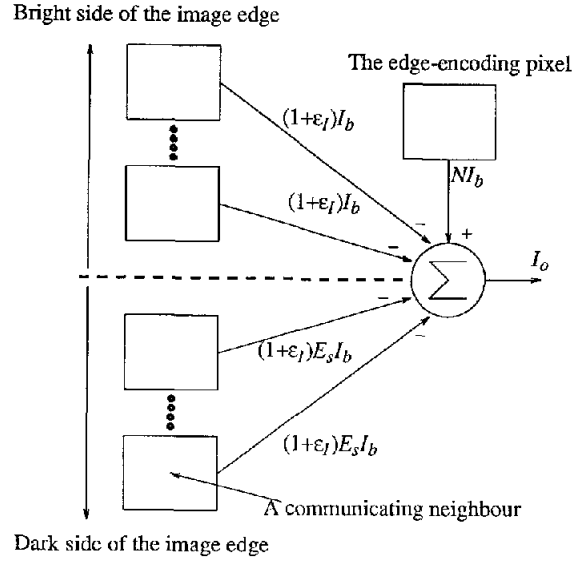


Fig. B1. Communications between a pixel encoding an image edge with its neighbors.

Acknowledgment

This work was supported by NSERC of Canada, ITRC and MicroNet. Chip fabrication was provided by the Canadian Microelectronics Corp. and Northern Telecom Inc.

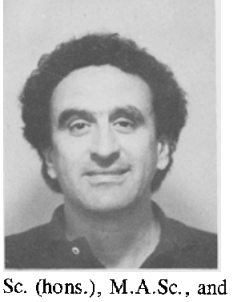
Notes

1. In the gaseous mode the signal may propagate out of a pixel in all directions.

References

1. C.P. Chong, C.A.T. Salama, and K.C. Smith, "A novel technique for image-velocity computation," to appear.
2. C.P. Chong, C.A.T. Salama, and K.C. Smith, "An imager with built-in image velocity computation capability," to appear.
3. M.M. McCabe and P.V. Collins, "Image processing algorithms," in *VLSI Image Processing* (R.J. Offen, ed.), Collins: London, 1985.
4. S. Cussons, "A real-time operator for the segmentation of blobs in imaging sensors," *Proc. IEEE Int. Conf. on Electronic Image Processing*, pp. 51–57, 1982.
5. R.W. Brodersen, "Evolution of VLSI signal-processing circuits," *Proc. Conf. on Advanced Research in VLSI*, pp. 43–47, 1989.
6. M.A. Sivilotti, M.A. Mahowald, and C.A. Mead, "Real-time visual computations using analog CMOS processing arrays," *Proc. Conf. on Advanced Research in VLSI*, pp. 295–312, 1987.
7. P. Siohan, D. Pele, and V. Ouvrard, "Two design techniques for 2-D FIR LoG filters," *Proc. Visual Communications and Image Processing '90*, pp. 970–981, 1990.
8. R. Wilson and M. Spann, *Image Segmentation and Uncertainty*, Research Studies Press: Herts, England, 1988.
9. C. Mead, *Analog VLSI and Neural Systems*, Chaps. 7, 15, Addison-Wesley: Reading, MA, 1989.
10. P.I. Suciu and D.A. Hodges, "Image contour extraction with analog MOS circuit techniques," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 65–72, 1977.
11. A.G. Andreou, K.A. Boahen, P.O. Pouliquen, A. Pavasovic, R.E. Jenkins, and S. Strohbehn, "Current-mode subthreshold MOS circuits for analog VLSI neural systems," *IEEE Trans. Neural Networks*, vol. 2, pp. 205–213, 1991
12. T.H. Lee, R.P. Khosla, B.C. Burkey, W.C. Chang, G.R. Moore, D.L. Losee, and K.Y. Wong, "A four-million pixel CCD image sensor," *Proc. Int. Symp. on VLSI Technology, Systems and Applications*, pp. 41–44, 1989.
13. C.R. Carroll, "A neural processor for maze solving," in *Analog VLSI Implementation of Neural Systems* (C.A. Mead and M. Ismail, eds.) Kluwer: Boston, 1989.

C.P. Chong received his B.A.Sc. and M.A.Sc. degrees from the University of Toronto, Canada in 1986 and 1988, respectively. He is currently completing his Ph.D. degree at the Department of Electrical Engineering, University of Toronto. He has published more than 15 papers in microelectronics, filters, and analog integrated circuits. He holds a patent on data conversions. His research interests include circuit, building block, and system design, analog VLSI parallel-processing arrays, neural networks, photosensitive devices, ASIC vision, A/D and D/A converters, and mixed A/D VLSI.



C. Andre T. Salama received the B.A. Sc. (hons.), M.A.Sc., and Ph.D. degrees, all in electrical engineering, from the University of British Columbia in 1961, 1962, and 1966, respectively. From 1962 to 1963 he served as a research assistant at the University of California, Berkeley. From 1966 to 1967 he was employed at Bell Northern Research, Ottawa, as a member of scientific staff working in integrated circuit design. Since 1967 he has been at the Department of Electrical Engineering, University of Toronto, where he is currently a professor and holder of the J.M. Ham chair in microelectronics. In 1975–1976 he was a visiting professor at the Katholieke Universiteit, Leuven, Belgium. In 1984 he was appointed as the Founding Chairman of the board of directors (presently member of the board) of the Canadian Microelectronics Corporation (CMC) funded by the Canadian government to further the development of microelectronics design and technology within the Canadian University system in close cooperation with industry and government laboratories. His research interests include the design and fabrication of semiconductor devices and integrated circuits. He has published extensively in technical journals, is the holder of 11 patents, and has served as a consultant to the semiconductor industry in Canada and the United States. He was associate editor of the *IEEE Transactions on Circuits and Systems*

for 1986–88 and is a member of the editorial board of *Solid State Electronics* and the *Analog IC and Signal Processing Journal*. He is a principal investigator in the Information Technology Research Center, a center of excellence funded by the Province of Ontario. He is also the program leader of Micronet, a network of centers of excellence focusing on microelectronics research and funded by the Canadian government. He was awarded an ITAC/NSERC Research Fellowship in information technology for 1989–90. Dr. Salama is a fellow of the Institute of Electrical and Electronics engineers, a member of the Association of Professional Engineers of Ontario and the Electrochemical Society.

K.C. Smith is a professor in the Department of Electrical Engineering, of Computer Science, and of Library and Information Science at the University of Toronto. His research interests are in linear and digital electronics, computer architecture, instrumentation, and human factors. He is the author or coauthor of well over 100 journal and symposium papers and a contributor to several books, including *Microelectronics Circuits*, second edition, coauthored with Adel S. Sedra. He is also an advisor to corporations in the United States and Canada. An IEEE fellow, Dr. Smith received his B.A.Sc., M.A.Sc., and Ph.D. degrees in engineering science, electrical engineering, and physics, respectively, from the University of Toronto.