INT. J. ELECTRONICS, 1988, VOL. 64, NO. 3, 409–415

A high-resolution CMOS comparator

CHU PHOON CHONG† and KENNETH C. SMITH†

A new high-speed high-resolution CMOS comparator is reported in this paper. A new offset-voltage-cancellation technique is used to reduce the effect of clock feed-through or charge pumping. The effective input voltage is doubled by the use of a cross-multiplexed technique. SPICE simulations using a modified MOS3 model (Wong 1986) show that the comparator reported here is capable of resolving 40 μV in less than 2·5 μs and 100 μV in 1 μs.

1. Introduction

The CMOS comparator is an important building block of A/D converters. Very often the speed and resolution of an A/D converter are limited by the speed and resolution of the comparator used.

A simple single-stage comparator is shown in Fig. 1. As shown, a capacitor is used to store the effective input offset voltage during the set-up phase of the clock (while ϕ is high). This effective offset voltage is then subtracted from the voltage at the negative-input terminal during the comparison phase (while ϕ is low). While such a scheme may effectively reduce the input offset voltage to a very low value, comparator resolution is limited by the error voltage produced by charge pumped out of the channel of the MOS switch connecting the output and the negative-input terminals of the opamp, and trapped on the grounded capacitor. The magnitude of this error voltage is a function of the size of the grounded capacitor and the size of the CMOS switch, typical value is around a few 100 μV.

Currently, the only technique available to reduce the charge-pumping effect is based on the use of a differential opamp as shown in Fig. 2. If the two (positive and negative) signal paths of the differential comparator are laid out symmetrically, the error voltages due to charge pumping in each signal path are likely to be equal and

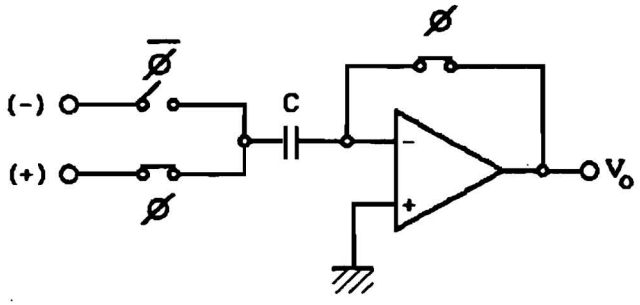

Figure 1. A single-stage comparator.

Received 30 July 1987; accepted 2 September 1987.

† Department of Electrical Engineering, University of Toronto, Toronto, Ontario, Canada M5S 1A4.

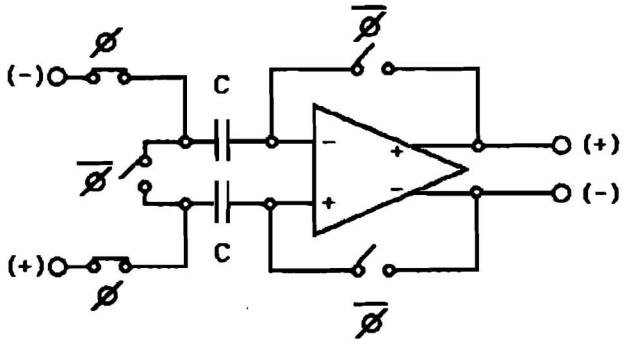

Figure 2. Differential comparator.

cancelled by the differential amplifier. A differential comparator with an input offset voltage as low as $5\,\mu V$ has been reported (Poujois and Borel 1978). However, for very low input voltages, the output voltage swing is limited due to low open-loop gain. By adding a latch to the output of the differential opamp, a resolution as low as $300\,\mu V$ in $5\,\mu s$ has been reported (Ng and Salama 1986). For high-speed operation the feedback loop around the latch is broken during the setup phase and is closed only at the end of the comparison phase. Such a scheme requires a three-phase clock.

Some authors have proposed comparators that do not include the offset-compensation switch in the feedback loop (Poujois *et al.* 1973, Alstott 1982, Hamade 1978). This removes the charge-pumping effect entirely. An example of such comparator is shown in Fig. 3. However, in order to prevent the output from entering saturation, the gain of each stage must be controlled to a relatively low value by a load device which can be either a diode-connected transistor or resistor.

2. A new CMOS comparator with low sensitivity to the charge-pumping effect

In this paper, we investigate the implementation of a new CMOS comparator based on the scheme shown in Fig. 3. However, instead of using a load to prevent each stage of the comparator from entering into saturation, we propose an internal offset-adjustment scheme which results in much-reduced sensitivity to the charge-pumping effect when compared to the circuit shown in Fig. 1. The gain of the new

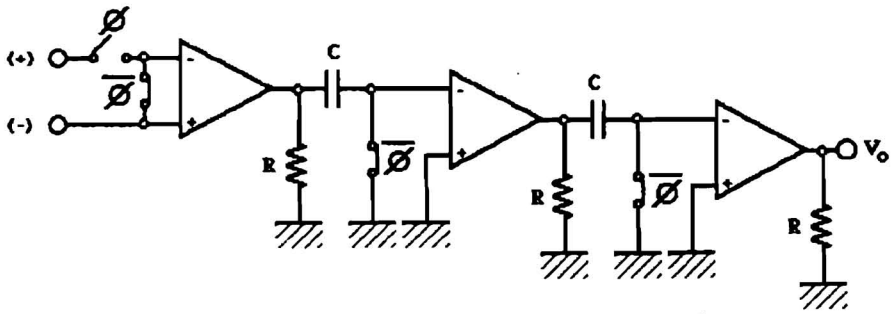

Figure 3. Multistage CMOS comparator.

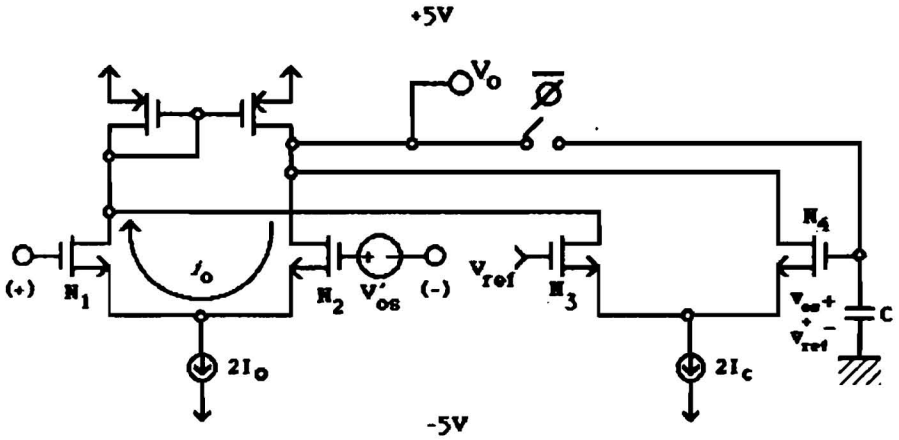

Figure 4. An internal offset-adjustment scheme that is less sensitive to the charge-pumping effect.

comparator proposed here is also not degraded by a load as in the case of the comparator shown in Fig. 3.

The internal offset-adjustment scheme proposed here is described in Fig. 4. Two differential pairs are connected in parallel; one differential pair (N_3 and N_4) is used to force the output voltage to be equal to V_{ref} at the end of the setup phase of a clock cycle, the other (N_1 and N_2) performs the function of voltage subtraction. In order to have high open-loop gain, the differential pair formed by N_1 and N_2 uses larger transistors and a higher biasing current to produce a large transconductance gain. To minimize the effect of the error voltage produced by charge pumping out of the switch and trapped in the grounded capacitor, the differential pair formed by N_3 and N_4 are biased by a smaller current and employ smaller transistors.

One may replace the actual error voltage, V_{os}, at the gate of N_4 by a smaller effective error voltage, V'_{os}, at the gate of N_2. The relationship between V_{os} and V'_{os} is given by

$$\frac{V'_{os}}{V_{os}} = \left(\left(\frac{I_c}{I_0}\right)\left(\frac{\beta_{3,4}}{\beta_{1,2}}\right)\right)^{1/2} \tag{1}$$

Thus $V'_{os}/V_{os} < 1$ if $I_c/I_o < 1$ and $\beta_{3,4}/\beta_{1,2} < 1$. Note that the smaller effective error voltage is achieved without sacrificing the gain of the comparator because the values of I_o and $\beta_{1,2}$ can be as large as necessary.

To increase the gain of the comparator, the gain-enhancement technique proposed by Martin (1987) is applied to the circuit in Fig. 4 and the resulting circuit is shown in Fig. 5.

Applying eqn. (1) to the circuit shown in Fig. 5, the effective error voltage is reduced by a factor of

$$\frac{V'_{os}}{V_{os}} = \left(\left(\frac{12}{180}\right)\left(\frac{6}{9}\right)\left(\frac{60}{225}\right)\right)^{1/2} = 0{\cdot}109.$$

Thus, the effective error voltage is approximately 10 times smaller.

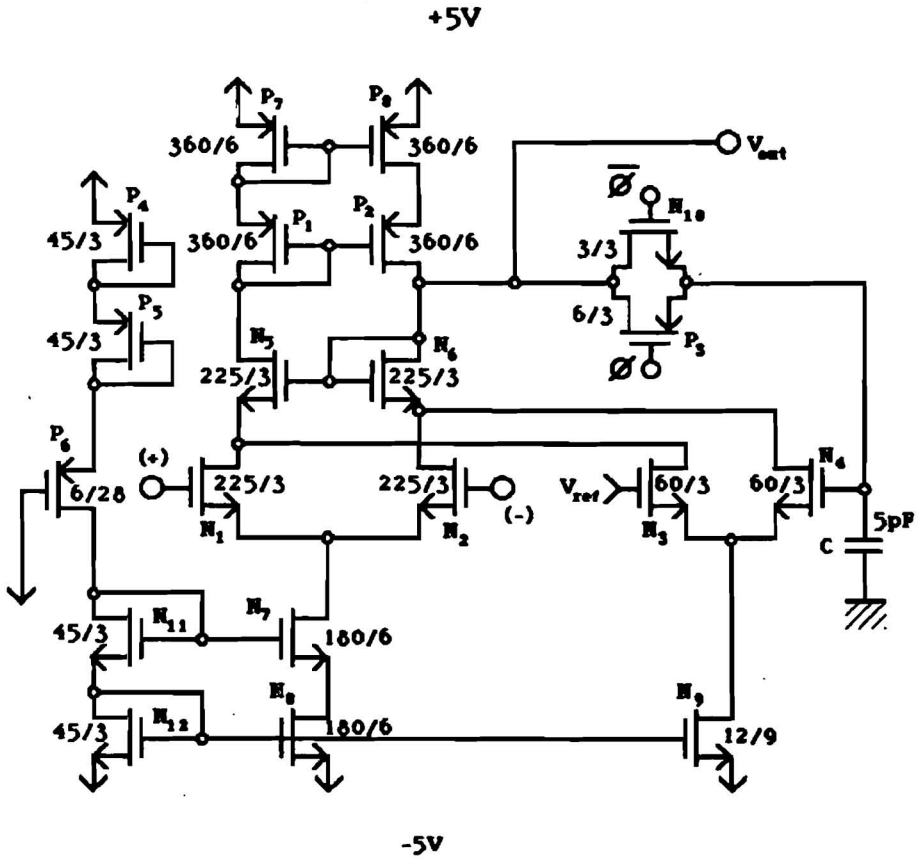

Figure 5. Schematic of CMOS comparator.

After a slight modification, eqn. (7) of Temes (1986) becomes

$$|V_{os}| \geq \left| \frac{7L_n^2}{\mu_n T} - \frac{7L_p^2}{\mu_p T} \right| \tag{2}$$

where L is the channel length of the MOSFETs used in the switch, T is the period of the clock and μ is the carrier mobility in the channel. Note that eqn. (2) is valid only if r is less than or equal to $T/14C$, where r is the turn-on resistance of the switch (Temes 1986).

Applying eqn. (2) to the circuit in Fig. 5,

$$|V_{os}| \geq 157\,\mu V,$$

for $T = 10\,\mu s$, $\mu_n = 785\,cm^2/Vs$ and $\mu_p = 265\,cm^2/Vs$. Thus,

$$|V'_{os}| \geq 17{\cdot}2\,\mu V$$

and the minimum resolution of the comparator is no longer limited by the error voltage due to charge pumping, but rather by the circuit noise level.

To further improve the minimum resolution of the comparator, a new cross-multiplexed technique can be used to double the effective voltage applied across the

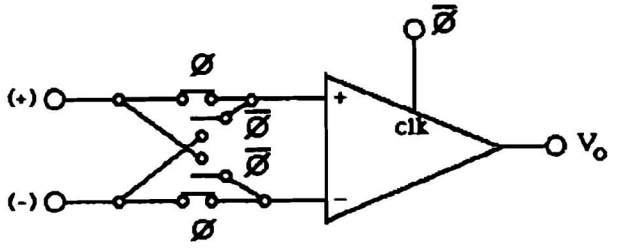

Figure 6. A high-resolution comparator using the cross-multiplexed technique.

input of the comparator without using a capacitor. The actual circuit is shown in Fig. 6. The principle of operation of the cross-multiplexed technique is illustrated in Fig. 7. As shown in Fig. 7, the output current during the comparison phase of a clock cycle is given by

$$i_o = 4i = 4g_m V_i \tag{3}$$

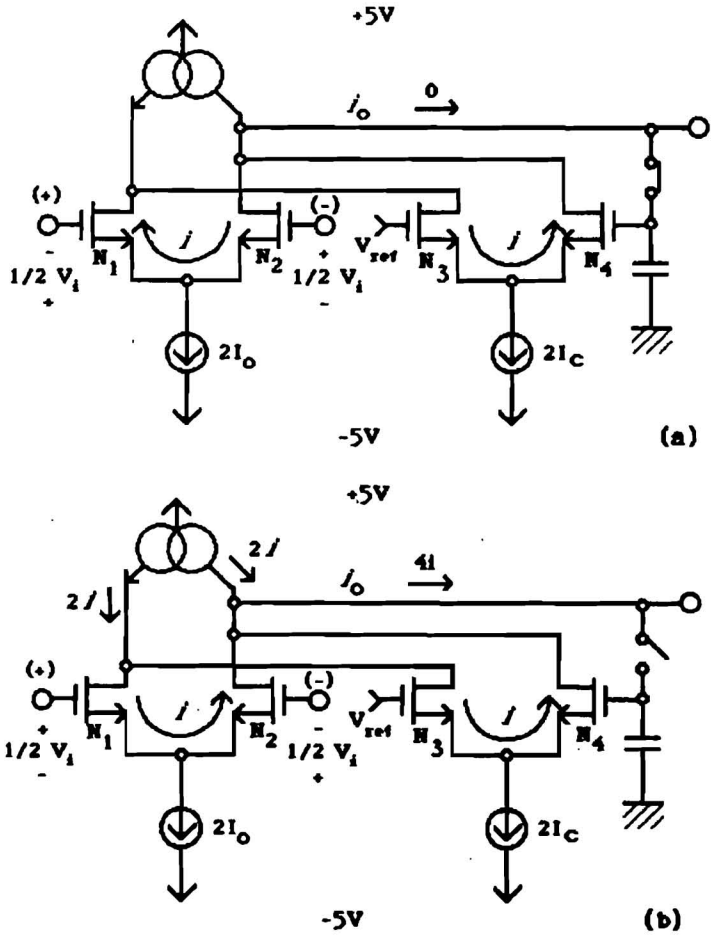

Figure 7. Small signal current flow in the comparator. (*a*) When the clock is low, and (*b*) when the clock is high.

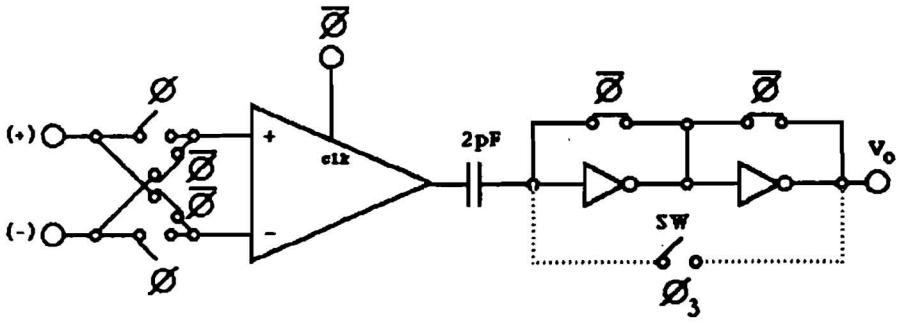

Figure 8. Three-stage CMOS comparator.

where g_m is the transconductance gain of the differential pair formed by N_1 and N_2. If the cross-multiplexed technique is not used, as in the case of the input stage in Fig. 3, the corresponding output current must be two times smaller. Thus the effective input voltage is increased two fold when the cross-multiplexed technique is employed.

SPICE simulation using the modified MOS3 model (Wong 1986) was performed on the comparator with and without the cross-multiplexed technique. Without the cross-multiplexed technique, for an input voltage of 100 μV, the output-voltage swing is 1 mV for a positive step and 58 mV for a negative step. (Assuming that the gain is constant for both cases of input voltages, the effective error voltage is calculated, base on the output voltages, to be 33·63 μV which is close to twice that predicted by eqns. (1) and (2).) With the cross-multiplexed technique, the corresponding output-voltage swings are 33 mV and 93 mV, respectively.

To increase the magnitude of output-voltage swing, two stages are added to the comparator as shown in Fig. 8. The size of the P- and N-MOSFETs used in the inverter are 21/3 and 10·5/3 respectively.

SPICE simulation of the multistage comparator shows that the comparator is capable of resolving 40 μV in less than 2·5 μs. For an input voltage of 100 μV, the response time of the comparator is about 1 μs for loads less than 20 pF.

For an input voltage below 100 μV, the output voltage falls significantly from its maximum possible value. For example, in the case of an input voltage equal to 40 μV, the output voltage falls to 3·8 V. This problem of low gain (and low output voltage) may be eradicated by using positive feedback and a three-phase clock (Ng and Salama 1986). This approach is shown in Fig. 8, where an additional switch, SW, is used to apply positive feedback around the two inverters at the end of the

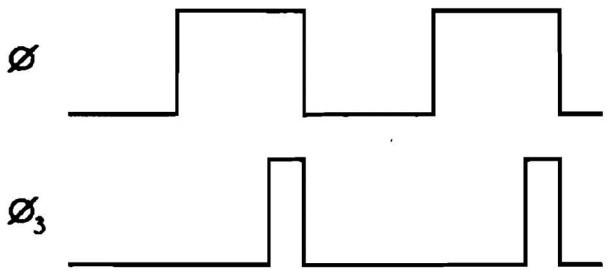

Figure 9. Three-phase clock.

comparison phase. The switch, SW, is turned on by a third phase of the clock which goes high 1 μs before the comparison phase ends as shown in Fig. 9.

Unlike related circuits reported heretofore, the resolution of the comparator reported here is not sensitive to mismatch between the two inverters. Moreover, only three switches are used in the latch, compare to four for similar circuits already reported (Ng and Salama 1986). The comparator consumes only 3 mW (maximum) of power during setup time.

3. Conclusion

A high-speed high-resolution comparator has been reported in this paper. The comparator uses an input stage that is less sensitive to clock feed-through (or charge-pumping). The new input stage is followed by two inverters which may be converted to a latch by turning on a third switch in order to increase the output voltage swing. Unlike any comparator reported thus far, the resolution of the comparator is not affected by mismatch in the two inverters. To further improve the resolution of the comparator, a cross-multiplexed technique can be used to effectively halve the required minimum input voltage. According to SPICE simulation results using the modified MOS3 model (Wong 1986), the comparator is capable of resolving 40 μV in less than 2·5 μs and 100 μV in less than 1 μs while consuming only 3 mW of power.

References

Alstott, D. J., 1982, A precision variable-supply CMOS comparator. *IEEE Journal of Solid-State Circuits*, **17**, 1080–1087.

Hamade, A. R., 1978, A single chip all-MOS 8-bit A/D converter. *IEEE Journal of Solid-State Circuits*, **14**, 785–791.

Martin, K. W., 1987, Gain enhancement technique for differential pairs. *Electronics Letters*, **23**, 154–156.

Ng, W. T., and Salama, C. A. T., 1986, High-speed high-resolution CMOS voltage comparator. *Electronics Letters*, **22**, 338–339.

Poujois, R., and Borel, J., 1978, A low-drift fully integrated MOSFET operational amplifier. *IEEE Journal of Solid-State Circuits*, **13**, 499–503.

Poujois, R., *et al.*, 1973, Low-level MOS transistor amplifier using storage techniques. *ISSCC Digest Technical Papers*, pp. 152–153.

Temes, G. C., 1986, Simple formula for estimation of minimum clock-feedthrough error voltage. *Electronics Letters*, **22**, 1069–1070.

Wong, S. L., 1986, CMOS analog circuit techniques for VLSI applications. PhD Thesis, Department of Electrical Engineering, University of Toronto, Canada, pp. 128–137.