INT. J. ELECTRONICS, 1987, VOL. 62, NO. 4, 515–520

Sinusoidal oscillators employing current conveyors

C. P. CHONG† and K. C. SMITH†

The effects of non-zero offset current at terminal z of a current conveyor on the operation of the entire circuit employing it are discussed. Correspondingly, criteria for DC biasing are derived. Application of these criteria leads to a proposal of two new circuits for sinusoidal oscillators. Additional constraints on the value of resistive components required to avoid large DC biasing currents are also considered.

1. Introduction

The concept of current conveying was introduced by Smith and Sedra (1968). Since then, the basic circuit building block called the current conveyor has been used in the implementation of a wide variety of circuits, for example, the gyrator, the mutator, the resonator and so on (Bhattacharyya *et al.* 1977, Black *et al.* 1971, Nandi 1977, 1978, Sedra and Smith 1970, Soliman 1978). The conveyor has been successfully used in the implementation of floating as well as grounded generalized-impedance converters (Chong 1986, Senani 1984, Soliman 1976). It has also been used extensively in the design of filters (Nandi 1978, Soliman 1973, Toumazou and Lidgey 1986) and sinusoidal oscillators (Jana and Nandi 1984, Senani 1979). In short, the current conveyor appears to be approaching the operational amplifier in terms of potential versatility.

Many authors have proposed circuits for sinusoidal oscillators employing current conveyors. So far, their main emphasis has been on the reduction of the number of components, both active and passive. As well, in order to ease the fabrication of the circuit proposed in IC-chip form, many authors have paid particular attention to the fact that a grounded capacitor is more compatible with current integrated-circuit technology than is a floating one. However, a majority of the authors do not take into account the effect of the non-zero offset current at terminal z of the current conveyor on the operation of the entire circuit.

2. The effect of non-zero offset current at terminal z

In a great many papers, several authors have proposed circuits employing a current conveyor in topologies which employ feedback directly or indirectly from terminal z to terminal y. Two examples of such circuits will be presented later in this paper in the context of Figs. 2 and 3. When a positive current conveyor is used, the connection provides positive feedback with the result that the magnitude of the DC biasing current at terminal z of the current conveyor, I_z, may potentially be much larger than the generating non-zero offset current $I_{z\,\mathrm{offset}}$. This can be seen easily from the following expression relating I_z to $I_{z\,\mathrm{offset}}$ derived, based on the typical circuit shown in Fig. 1.

Received 1 September 1986; accepted 6 October 1986.

† Department of Electrical Engineering, University of Toronto, Toronto, Ontario, Canada M5S 1A4.

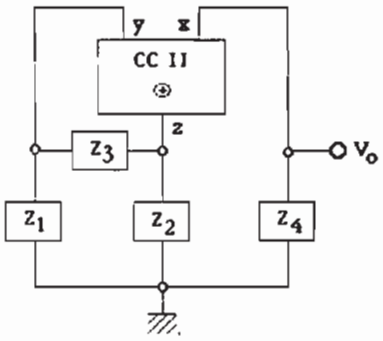

Figure 1. A general one-port circuit configuration of a sinusoidal oscillator employing a single current conveyor.

Since $V_y = V_x$

$$(I_{z\,\text{offset}} + I_z)\frac{Z_1Z_2}{Z_1 + Z_2 + Z_3}\bigg|_{s=0} = I_x Z_4\bigg|_{s=0}$$

$$= I_z Z_4\bigg|_{s=0}$$

Therefore

$$I_z = I_{z\,\text{offset}}\left\{\frac{Z_1Z_2}{(Z_1 + Z_2 + Z_3)Z_4 - Z_1Z_2}\right\}\bigg|_{s=0}$$

Thus, to obtain a small value of I_z, either $I_{z\,\text{offset}}$ must be very small or

$$\lim_{s\to 0}(Z_1 + Z_2 + Z_3)Z_4 \gg \lim_{s\to 0} Z_1Z_2$$

That is

$$\lim_{s\to 0} Z_4 \gg \lim_{s\to 0}\frac{Z_1Z_2}{Z_1 + Z_2 + Z_3} \tag{1}$$

It should be noted that if

$$\lim_{s\to 0} Z_1Z_2 \gg \lim_{s\to 0}(Z_1 + Z_2 + Z_3)Z_4 \tag{2}$$

then $I_z \approx -I_{z\,\text{offset}}$, which shows that I_z is small and is in a direction opposite to that of $I_{z\,\text{offset}}$. This appears to be desirable; however, in general, it is not! There are three ways to satisfy condition (2).

The first way is to choose both Z_1 and Z_2 to be capacitive. In this case, the output voltage will be saturated at the positive or negative supply voltage depending on the direction of I_z offset. Here, this phenomenon is termed latch-up.

The second way is to make either Z_1 or Z_2 capacitive. In this case, condition (2) reduces to

$$\lim_{s\to 0} Z_2 \gg \lim_{s\to 0} Z_4 \ (Z_1 \text{ is capacitive})$$

or

$$\lim_{s\to 0} Z_1 \gg \lim_{s\to 0} Z_4 \ (Z_2 \text{ is capacitive})$$

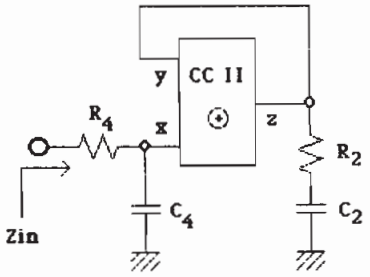

Figure 2. RCD series resonator configuration proposed by Nandi (1979).

These obviously will cause a much larger offset voltage at terminal z than that at terminal x.

The third way is to choose all impedances having a parallel resistive component, with the parallel resistive component of Z_4 much smaller than that of the others. This case is more complicated than the above two cases. It is hard to discuss the effects on the circuit in general; however, in some special cases the parallel resistive component of Z_4 may have to be so small that during the power-up time of the circuit a large current may flow out of terminal x while terminal z is saturated at the supply voltage (making the voltage at terminal y large).

When a negative current conveyor is used, the expression for I_z becomes

$$I_z = I_{z\,\text{offset}} \left\{ \frac{Z_1 Z_2}{(Z_1 + Z_2 + Z_3)Z_4 + Z_1 Z_2} \right\} \Bigg|_{s=0}$$

which shows that I_z is always smaller than $I_{z\,\text{offset}}$. Latch-up will not occur due to the existence of negative feedback between terminals y and z.

An example of a circuit published in the literature that may not meet condition (1) stated above, is the resonator proposed by Nandi (1979). The resonator is shown here in Fig. 2, with the components relabelled to ease the application of condition (1).

If the resonator is connected in parallel with some resistive or inductive impedance, it can be easily shown that condition (1) is not met, and the resonator suffers from the latch-up effect described above.

As another example, consider the sinusoidal oscillator proposed by Senani (1979). It is shown here in Fig. 3.

In this case, $Z_1 = r_1 \| (r_2 + r_3)$. Applying condition (1), we obtain the following additional constraint on the value of resistive components

$$R_4 \gg r_1 \| (r_2 + r_3)$$

Many other circuits that have been published in the literature potentially suffer from the latch-up phenomenon described above. Since some of the circuit configurations employed are much more complex than the ones discussed here, condition (1) cannot be applied directly. However, in most cases, simple DC analysis will yield the required constraint on values of resistive components.

3. Modification to the sinusoidal oscillator

Jana and Nandi (1984) proposed a sinusoidal oscillator circuit employing only a single current conveyor and with all capacitors grounded. Moreover, tuning is done

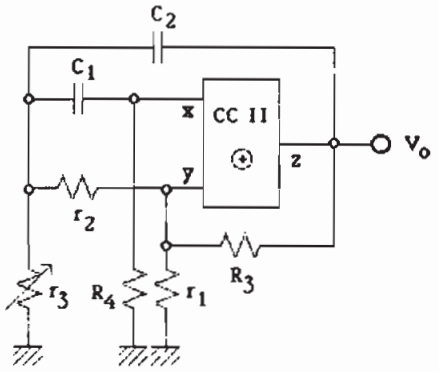

Figure 3. Single-resistance-controlled sinusoidal oscillator proposed by Senani (1979).

by a grounded resistor. This circuit, shown in Fig. 4, is generally considered to be one of the best sinusoidal oscillator circuits employing current conveyors proposed thus far. The condition for oscillation is

$$C_4 = C_2(1 + R_3/R_1) + C_1 \tag{3}$$

and the frequency of oscillation is

$$\omega_0 = \left(\frac{R_4 - R_1}{R_1 R_3 R_4 C_1 C_2}\right)^{1/2} \tag{4}$$

Employing condition (1) to the circuit in Fig. 4, the following constraint on the values of resistive components is obtained

$$R_4 \gg R_1 \tag{5}$$

Condition (5) coincides with the criterion for low sensitivity of ω_0 to R_1 and R_4, a fact which is not explicitly stated by the original authors. Thus, for the circuit to operate at low frequency with small values of C_1 and C_2 and with R_4 only slightly larger than R_1, then the value of R_1 and R_4 must have a very small tolerance, which is not easily possible, certainly in integrated-circuit technology without laser trimming. As well, for these conditions, the value of $I_{z\,\text{offset}}$ must be kept as small as possible to reduce the offset voltages at various points in the circuit.

One possible way to reduce the offset voltage at terminal z is to remove the resistor R_1 and replace it with a resistor R_2 connected in parallel with C_2. The resulting circuit is as shown in Fig. 5.

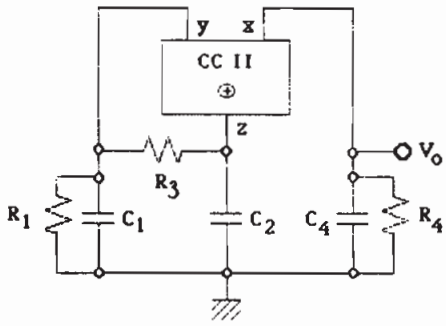

Figure 4. Sinusoidal oscillator proposed by Jana and Nandi (1984).

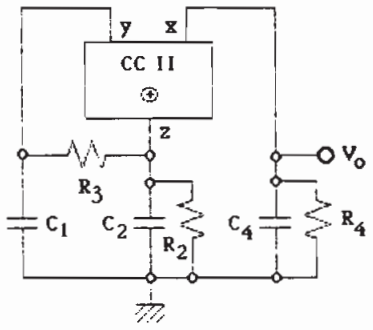

Figure 5. Modification to sinusoidal oscillator proposed by Jana and Nandi (1984).

Simple analysis shows that

$$R_2 R_3 R_4 C_1 C_2 s^2 + R_4(R_2 C_2 + R_2 C_1 + R_3 C_1 - R_2 C_4)s + R_4 - R_2 = 0 \quad (6)$$

Therefore, the condition for oscillation is

$$C_4 = C_1(1 + R_3/R_2) + C_2 \quad (7)$$

which is slightly different from eqn. (3), and the frequency of oscillation is

$$\omega_0 = \left(\frac{R_4 - R_2}{R_2 R_3 R_4 C_1 C_2}\right)^{1/2} \quad (8)$$

which is similar to eqn. (4) except that R_1 is replaced by R_2.

While this modified circuit still has the problem that R_4 must be much larger than R_2, for low frequency oscillation it is possible to choose R_3 to be very large without affecting the DC offset voltage at terminal z. This is obviously an advantage over the original circuit.

A latch-up-free sinusoidal oscillator circuit can be obtained as a special case of the circuit shown in Fig. 5 by removing R_4 (that is allowing R_4 to approach infinity). The resulting circuit has the following characteristic polynomial

$$R_2 R_3 C_1 C_2 s^2 + [R_2(C_1 + C_2 - C_4) + R_3 C_1]s + 1 = 0 \quad (9)$$

Therefore, the condition for oscillation is

$$C_4 = C_1(1 + R_3/R_2) + C_2 \quad (10)$$

and the frequency of oscillation is

$$\omega_0 = \left(\frac{1}{R_2 R_3 C_1 C_2}\right)^{1/2} \quad (11)$$

It should be noted that eqn. (10) is the same as eqn. (7) and no finite constraint exists for the value of resistive components.

4. Conclusion

This paper has studied the effect of a non-zero offset current at terminal z of a current conveyor on the operation of the entire circuit. Expressions relating the biasing current, I_z, have been deduced. Two new circuits for sinusoidal oscillators

obtained by modifying the sinusoidal oscillator circuit proposed by Jana and Nandi (1984) are proposed. One of the circuits proposed here is latch-up-free for non-resistive loads.

References

BHATTACHARYYA, B. B., DAS, S. K., and SWAMY, M. N. S., 1977, A simple inductance-simulation scheme and its application in data communication. *Proceedings of the I.E.E.E.*, **65,** 268–269.

BLACK, G. G. A., FRIEDMAN, R. T., and SEDRA, A., 1971, Gyrator implementation with integrable current conveyors. *I.E.E.E. Journal of Solid-state circuits*, **6,** 396–399.

CHONG, C. P., 1986, The current conveyor—its implementations and applications, B.A.Sc. thesis, Department of Electrical Engineering, University of Toronto, Canada, pp. 90–91.

JANA, P. B., and NANDI, R., 1984, Single current conveyor tunable sinewave *RC* oscillator. *Electronics Letters*, **20,** 44–45.

NANDI, R., 1977, Inductor simulation using a current conveyor. *Proceedings of the I.E.E.E.*, **65,** 1511–1512.

NANDI, R., 1978, Active inductances using current conveyor and their application in a simple bandpass filter realization. *Electronics Letters*, **14,** 483–484.

NANDI, R., 1979, A new equal-valued grounded-capacitor resonator realization using current conveyor. *Proceedings of the I.E.E.E.*, **67,** 870–871.

SEDRA, A., and SMITH, K. C., 1970, A second generation current conveyor and its applications. *I.E.E.E. Transactions on Circuit Theory*, **17,** 132–134.

SENANI, R., 1979, New canonic single-resistance-controlled sinusoidal oscillator using a single current conveyor. *Electronics Letters*, **15,** 568–569.

SENANI, R., 1984, Floating ideal FDNR using only two current conveyors. *Electronics Letters*, **20,** 205–206.

SMITH, K. C., and SEDRA, A., 1968, The current conveyor: a new circuit building block. *Proceedings of the I.E.E.E.*, **56,** 1368–1369.

SOLIMAN, A. M., 1973, Inductorless realization of an all-pass transfer function using the current conveyor. *I.E.E.E. Transactions on Circuit Theory*, **20,** 80–81.

SOLIMAN, A. M., 1976, Generalized immittance inverters and their realizations. *International Journal of Electronics*, **41,** 59–64.

SOLIMAN, A. M., 1978, New active gyrator circuit using a single current conveyor. *Proceedings of the I.E.E.E.*, **66,** 1580–1581.

TOUMAZOU, C., and LIDGEY, F. J., 1986, Universal active filter using current conveyors. *Electronics Letters*, **22,** 662–664.