Self-checking binary logic systems using ternary logic circuits

Systèmes logiques binaires à auto-vérification utilisant des circuits logiques ternaires

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The present status of multivalued logic is highlighted in a Canadian context. A particular example is given of the use of ternary circuits in the solution of the problem of testability of binary logic, through the introduction of a new concept called 2-of-3-valued logic. Its application to the design of combinational and sequential self-checking systems is demonstrated. Keywords in this paper include: multivalued logic, testability, reliability, ternary logic, CMOS logic, and fault tolerance.

La situation présente de la logique à valeurs multiples est mise en relief dans un contexte canadien. Un exemple particulier est donné sur l'utilisation de circuits ternaires dans la solution de problème de la possibilité de contrôle de la logique binaire par le biais de l'introduction d'un nouveau concept appelé logique à valeur 2-de-3. Une démonstration est faite de son application au design de systèmes combinatoires et séquentiels à auto-vérification. Dans cette étude, les mots-clés comprennent: logique à valeurs multiples, possibilité de contrôle, fiabilité, logique ternaire, logique MOS complémentaire, et insensibilité aux défaillances.

Overview

In spite of the current dominance of binary logic, the more general alternative, called multiple-valued logic (MVL), has been a concern to researchers for a very long time.[1-4] For example, Post in 1921 prepared a definitive paper on the mathematical potential of the MVL discipline.[4] Since that time, there has been a recurring interest in the topic of multiple-valued logic as a solution to practical problems of many kinds. For instance, in 1958, the Russians announced the existence of a multiple-valued computer (SETUN) using magnetic devices. It was, however, not a great success. While the mathematics has been relatively mature and powerful, the difficulty has been in the lack of an appropriate technology.

Such was the situation in the late 1960s, when work in electrical engineering was initiated by Vranesic at the University of Toronto in multiple-valued logic.[5] Shortly thereafter, researchers at Toronto assisted in the first International Symposium on Multiple-Valued Logic held in Buffalo in 1971. In response to the interest it generated, this event was repeated in Buffalo in 1972, in Toronto in 1973 and at various locations throughout the world each year since that time, most recently in Paris and then in Kyoto.

Surprisingly, a glance at the proceedings of the symposium[1] will show that researchers from all across Canada have played an unusually important role in this recent cycle of developments in MVL. This is particularly gratifying now that integrated silicon technology is providing a variety of opportunities, both demonstrated and potential, for the implementation of multiple-valued circuits.[3] The present paper is intended to provide a glimpse of this large, but largely unknown, topic and of its potential for use in the solution of problems in the binary world.

Introduction

The application of multivalued logic circuits to fault detection of binary logic system has attracted many investigators.[6-11] The accepted approach is simply to replace each binary logic circuit by its multivalued logic circuit equivalent. In this case, otherwise surplus logic values can be used either to detect faults within the circuit or to simplify the method of fault detection. The scheme which has been proposed by Hu and Smith[9,10] is to realize a binary logic system with Inverters and NAND (or NOR) gates using an augmented version of a proven CMOS ternary technology.[12] Of the three logic values provided by each CMOS ternary gate, two extreme logic values are used as working values, while the middle logic value is reserved for self-checking and testing. This type of logic circuit has been called a *2-of-3-valued logic circuit,* and the resulting system is called a 2-of-3-valued system.

All single faults in the system of 2-of-3-valued gates can be classified as one of the following four types: mid-seeking quasi-mid-seeking, mid-rejecting, and masked. It is proven[9,10] that 2-of-

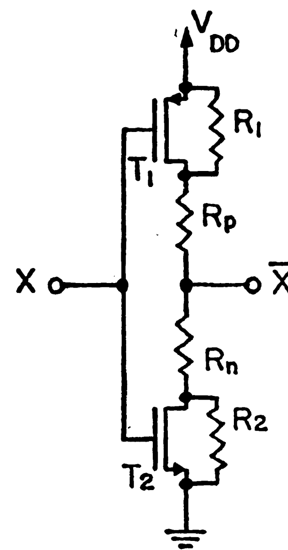

Figure 1: *A 2-of-3-valued inverter.*

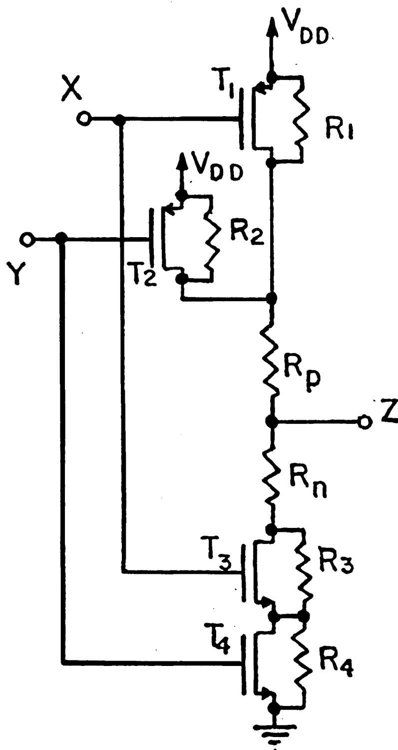

Figure 2: *A 2-of-3-valued NAND gate.*

3-valued combinational systems are totally self-checking for mid-seeking and quasi-mid-seeking faults, and that 2-of-3-valued synchronous sequential systems are totally self-checking for mid-seeking faults. However, mid-rejecting faults in a 2-of-3-valued combinational system, and both mid-rejecting faults and quasi-mid-seeking faults in a 2-of-3-valued synchronous sequential system should be treated as hardcore and can be tested off-line. For masked faults, both systems are fault secure. The following material describes both the 2-of-3-valued combinational system and synchronous sequential system in a unified manner. The discussion is based on two papers presented by Hu and Smith.[9,10]

2-of-3-valued logic gates

In the 2-of-3-valued system, two logic operators are used, specifically, the Negation operator and the NAND operator. Let $Q = \{0, 1/2, 1\}$ be the set of logic values. Inputs x,y are in Q. The Negation operator is defined as:

$$\bar{x} = 1 - x.$$

The truth table of the Negation operation is given in Table 1, columns 1 and 2.

The NAND operator is defined as:

$$x \bullet y = 1 - \min(x,y).$$

The truth table of the NAND operation is given in Table 2 columns 1, 2, and 3.

Logic value set Q can be divided into two disjoint subsets, the normal working value set $N = \{0,1\}$, and the fault-testing value set $E = \{1/2\}$. Note from Tables 1 and 2 that when the inputs take on values only in N, these ternary operators are the same as binary operators. In other words, for binary signals, these operators serve as binary operators. The third logic value (the middle one) is dedicated to testing and self-checking.

It is well known that CMOS devices may easily be used to form ternary logic circuits because of their intrinsic circuit symmetry. There are several basic schemes for realizing CMOS ternary circuits.[2,12,13] From the fault detection point of view, a modified form of one of the traditional circuits which was introduced by Mouftah[12] is proposed. Such a CMOS 2-of-3-valued Inverter realizing the Negation operator is shown in Figure 1. In this circuit, logic value 0 corresponds to 0 volts, logic value 1/2 corresponds to $1/2V_{DD}$, and logic value 1 corresponds to V_{DD}. The values of V_{DD}, R_p, R_n, R_1, and R_2 should be chosen properly to meet the following conditions.

$$R_p = R_n, \text{ and } R_1 = R_2 \geq 20R_p.$$

Note that R_1 and R_2 are redundant in normal operation. However, they are important for fault detection purposes. Figure 2 is a NAND gate which realizes the NAND operator. The analysis for this circuit is similar to that for the Inverter.

Fault analysis

Although historically important in the analysis of faulty binary logic, the stuck-at model has recently been recognized as an incomplete model of real faults.[17] Accordingly, an *"open-short" model* was adopted in which faults are attributed directly to open and short circuits of each device in the circuit diagram. The single fault assumption has also been adopted. Under these conditions, all possible single faults are listed in Table 1 for an Inverter and in Table 2 for a NAND gate. In these tables, "*s*" denotes a short-circuit fault and "*o*" denotes a open-circuit fault.

In Tables 1 and 2 it is apparent that there are four types of faults. The first type of fault meets the following two conditions: Firstly there exists at least one normal input (taking values from N) such

TABLE 1
Truth table for a 2-of-3-valued inverter

Input	Output														
	Fault-free	Mid-seeking				Quasi-mid-seeking		Mid-rejecting				Masked	
x	$\bar{x}$	T_{1s}	T_{2s}	R_{1s}	R_{2s}	T_{1o}	T_{2o}	R_{ps}	R_{ns}	R_{po}	R_{no}	R_{1o}	R_{2o}
0	1	1	1/2	1	1/2	1/2	1	1	1	0	1	1	1
1/2	1/2	1/2	1/2	1/2	1/2	0	1	1	0	0	1	1/2	1/2
1	0	1/2	0	1/2	0	0	1/2	0	0	0	1	0	0

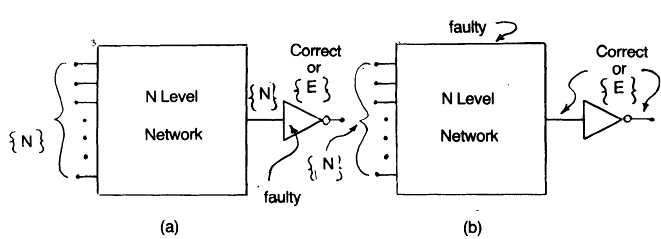

Figure 3: *An N-level network followed by an inverter.*

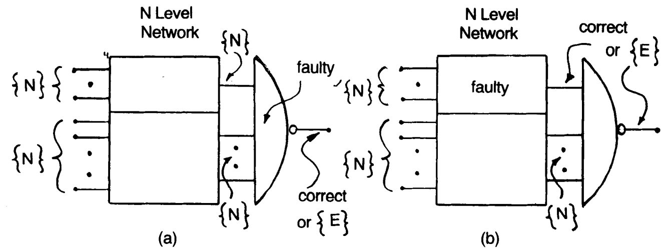

Figure 4: *An N-level network followed by a NAND gate.*

that the output of the faulty gate will be 1/2. Secondly for all possible inputs (taking values from Q), the output of the faulty gate is either correct or 1/2. This type of fault is called a *mid-seeking fault*. The second type of fault also meets two conditions. The first condition is the same as that for a mid-seeking fault. The second condition is the Negation of the second one for a mid-seeking fault. That is, there exists at least one possible input such that the output of the faulty gate is neither correct nor 1/2. This fault is called a *quasi-mid-seeking fault*. The third type of fault will prevent the occurrence of a 1/2 signal at the output of the faulty gate. Such a fault is called a *mid-rejecting fault*. The fourth type of fault produces no error at the output of the faulty gate. It is called a *masked fault*.

2-of-3-valued combinational systems

To form a self-checking combinational system, 2-of-3-valued circuits can be used. To facilitate the analysis of such a system, it is necessary to introduce some concepts related to self-checking.[14] A logic circuit is *self-testing* for a set of faults (F) if for any fault in F there is at least one normal input combination (in N) which produces an output in E, the testing value set. A logic circuit is *fault secure* for F if, for any fault in F and any input in N, the output is either in E or correct, but never incorrect in N. This means that for a fault secure logic circuit, a fault can only change a normal output to an abnormal one, but cannot change one normal output level (0 or 1) to another normal output level (1 or 0). A logic circuit is *totally self-checking* for F if it is both fault secure for F and self-testing for F.

For a combinational system which consists of 2-of-3-valued gates, some conclusions can be reached:

- For any mid-seeking and quasi-mid-seeking fault, the 2-of-3-valued Inverter is totally self-checking. This conclusion can be easily proven by observing Table 1.
- For any mid-seeking and quasi-mid-seeking fault, the 2-of-3-valued NAND gate is totally self-checking. This conclusion can be easily proven by observing Table 2.
- For any mid-seeking and quasi-mid-seeking fault, any irredundant combinational logic network which consists of 2-of-3-valued Inverters and NAND gates is totally self-checking.

A formal proof for this third conclusion, which is based on a mathematical inductive method, can be found in Reference 9. Here, a brief discussion only will be given. Firstly, for a single-level network, this conclusion is the direct result of combining conclusions 1 and 2. Furthermore, if one assumes that an N-level network is totally self-checking, it can be proven that an (N+ 1)-level network is also totally self-checking. This can be done by considering all possible situations:

- an N-level fault-free network followed by a faulty Inverter (*see Figure 3a*).

TABLE 2
Truth table for a 2-of-3-valued NAND gate

Input		Output																								
		Fault-free	Mid-seeking								Quasi-mid-seeking				Mid-rejecting				Masked			
X	Y	$X \cdot Y$	T_{1s}	T_{2s}	T_{3s}	T_{4s}	R_{1s}	R_{2s}	R_{3s}	R_{4s}	T_{1o}	T_{2o}	T_{3o}	T_{4o}	R_{ps}	R_{po}	R_{ns}	R_{no}	R_{1o}	R_{2o}	R_{3o}	R_{4o}
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1/2	1	1	1	1/2	1	1	1	1/2	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1/2	1	1	1	1/2	1	1/2	1	1	1	1	0	1	1	1	1	1	1
1/2	0	1	1	1	1	1/2	1	1	1	1/2	1	1	1	1	1	0	1	1	1	1	1	1
1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1	1	1	0	0	1	1/2	1/2	1/2	1/2
1/2	1	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	0	1/2	1	1	1	0	0	1	1/2	1/2	1/2	1/2
1	0	1	1	1	1	1/2	1	1	1	1/2	1	1/2	1	1	1	0	1	1	1	1	1	1
1	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	0	1	1	1	0	0	1	1/2	1/2	1/2	1/2
1	1	0	1/2	1/2	0	0	1/2	1/2	0	0	0	0	1/2	1/2	0	0	0	1	0	0	0	0

- a faulty N-level network followed by a fault-free Inverter (*see Figure 3b*).
- an N-level fault-free network followed by a faulty NAND gate (*see Figure 4a*).
- a faulty N-level network followed by a fault-free NAND gate (*see Figure 4b*).

Since under each of these situations, it can be shown that the entire network is totally self-checking, the general conclusion is proven.

According to these conclusions, in a 2-of-3-valued combinational system, all mid-seeking and quasi-mid-seeking faults can be detected during normal operation. If the output is in N, the system is guaranteed to be operating properly. The only additional requirement is that of a checker to detect a 1/2 signal at the output of the system.

2-of-3-valued synchronous sequential systems

A sequential system differs from a combinational system in that it includes feedback. Conventionally, a pseudo-combinational circuit model[15] can be used to analyze fault characteristics of a sequential system. Here, because of feedback, a single fault in a sequential system is logically equivalent to a multiple fault in the corresponding iterative array. Thus in a sequential system, the input of the faulty gate cannot be guaranteed to take on values only from N as it would in a combinational system.

By observing Tables 1 and 2, it is found that for mid-seeking faults, and all possible input combinations, the gate will remain totally self-checking. However, for quasi-mid-seeking faults, when the input combination contains some values from E, the gate will not remain totally self-checking. Accordingly, for a 2-of-3-valued synchronous sequential system (*see Figure 5*), the following conclusion stands: if both input X and next state W (or output Z and internal state y) are observable, then for any mid-seeking fault, a 2-of-3-valued synchronous sequential system is totally self-checking. The formal proof for this conclusion can be found in Reference 10. As an example, a 2-of-3-valued R–S flip-flop will be discussed.

Figure 6 is a 2-of-3-valued R–S flip-flop.[16] The structure is the same as that of a binary R–S flip-flop. However, the component gates are 2-of-3-valued gates instead of binary ones. Its state table is shown in Table 3. In this table, there are undefined states denoted by "u". To ensure proper operation, it is necessary to place a limitation on allowed input combinations:

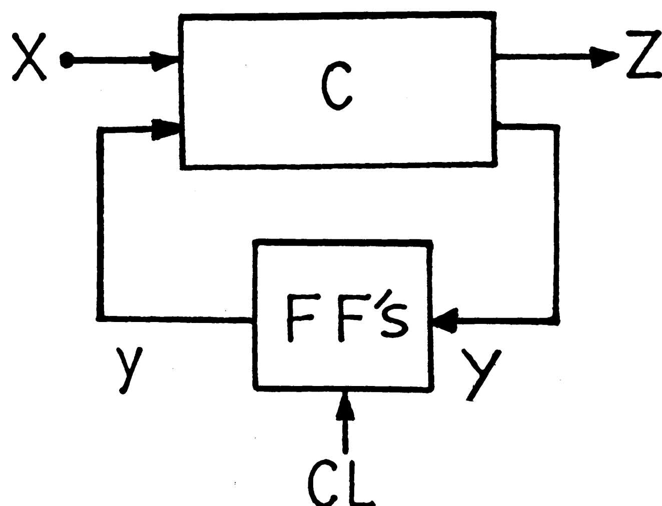

Figure 5: *Block diagram for a sequential system.*

$$\bar{S} + \bar{R} \geq 1.$$

To demonstrate that this flip-flop is totally self-checking for any mid-seeking fault, it is assumed arbitrarily that there is a mid-seeking fault T_{3s} in gate 1. Furthermore, assume $Q(t) = 0$, $<SR> = <01>$. Under these conditions, the fault-free flip-flop will change state from $Q(t) = 0$ to $Q(t+1) = 1$ (*see Table 3*). For the faulty flip-flop, the input of gate 1 is $<01>$. According to Table 2, Q will become 1/2, at which time the input of gate 2 becomes $<1/2\ 1>$. According to Table 2, $\bar{Q}$ will also turn to 1/2. This signal change causes the input of gate 1 to change to $<0\ 1/2>$. According to Table 2, for this input, Q is still 1/2. Thus, the whole flip-flop stabilizes at the state $Q(t+1) = 1/2$, $\bar{Q}(t+1) = 1/2$ indicating that there is a mid-seeking fault.

TABLE 3
State table for an R–S flip-flop

$Q(t+1)$		$\bar{S}(t)\ \bar{R}(t)$								
		0 0	0 1/2	0 1	1/2 0	1/2 1/2	1/2 1	1 0	1 1/2	1 1
$Q(t)$	0	u*	u	1	u	1/2	1/2	0	0	0
	1/2	u	u	1	u	1/2	1/2	0	1/2	1/2
	1	u	u	1	u	1/2	1	0	1/2	1

*u—undefined state

When an R–S flip-flop is connected with a combinational network, the resulting network can be proven still to be totally self-checking. Thus, more complicated flip-flops such as clocked R–S flip-flops and D flip-flops can be constructed. Moreover, it is also possible to form master-slave 2-of-3-valued flip-flops, and they have been proven to be totally self-checking. Since all these flip-flops have the same structure as their binary counterparts (only master-slave J–K flip-flops have a slightly different structure), the detailed circuit diagrams are omitted. They can be found in Reference 10.

Testing the hardcore

All mid-rejecting faults in a 2-of-3-valued combinational system and all mid-rejecting and quasi-mid-seeking faults in a 2-of-3-valued synchronous sequential system are not included in the fault set for which the system is totally self-checking. Hence, they must be treated as hardcore and tested off-line. Here only a test procedure for mid-rejecting faults in a combinational system will be discussed in detail. However the general idea is applicable to the test of sequential systems.

In Tables 1 and 2, it is noted that when all the inputs of a gate are 1/2, the output of a fault-free gate will be 1/2, but for a gate having a mid-rejecting fault, the output becomes 0 or 1. Thus by setting all inputs to 1/2, the 1/2 signal at the output of a gate indicates freedom from mid-rejecting faults. From Table 2, to propagate this 1/2 signal through succeeding levels, all other inputs of each succeeding NAND gate should be held at 1. Accordingly, a traditional method, such as path sensitizing, must be used to derive the test. In the particular case that a two-level NAND network realization is used, the test method becomes quite straightforward.

The procedure is as follows. In Figure 7, set all the inputs of the gate to be tested in the first level to 1/2. Set at least one input of each remaining gate in the first level to 0. This will cause the outputs

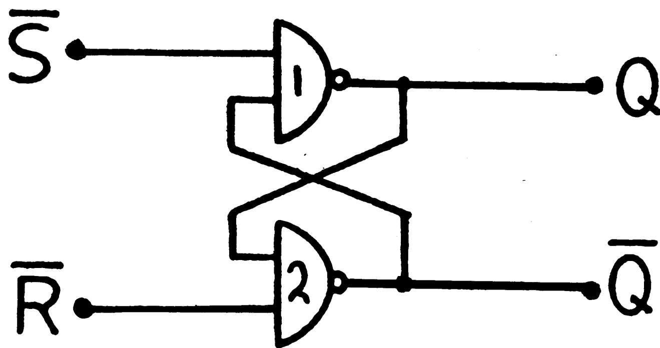

Figure 6: *An R–S flip-flop.*

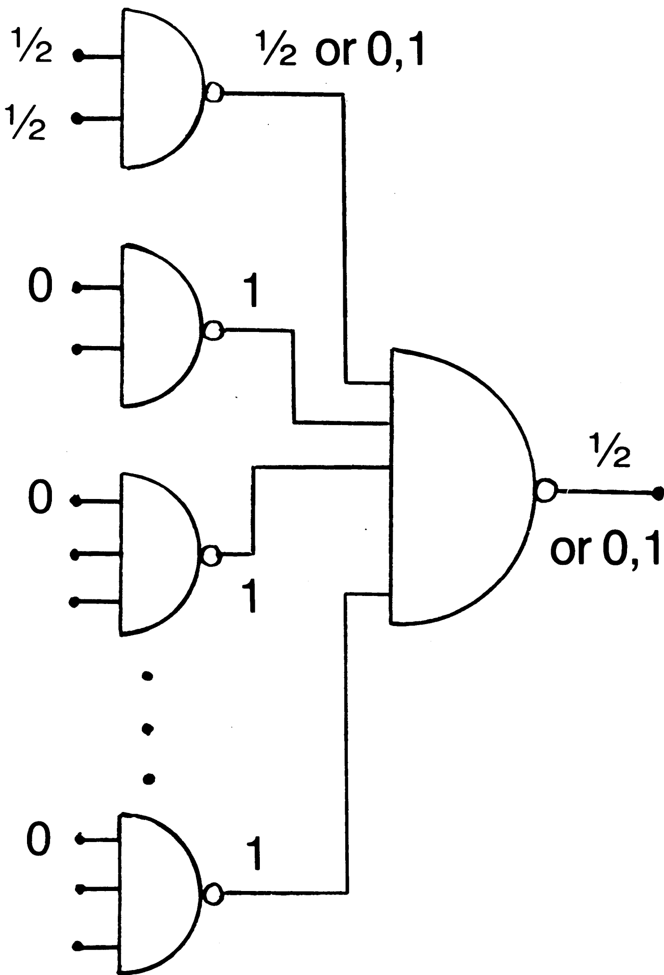

Figure 7: *Testing for mid-rejecting faults.*

of the remaining gates in the first level to be 1. If the tested gate is fault-free, its output will be 1/2. This 1/2 signal will propagate to the output of the second level gate. If the tested gate is faulty, the output of the second level gate will not be 1/2. If the second gate has a mid-rejecting fault, then for every test code its output will always be 0 or 1, but never 1/2.

For masked faults, the output of the system remains correct. That is, no error will be produced. In the case when multiple masked faults occur, an error may result. However, the probability of this is very low.

Conclusion

In this paper, a scheme of 2-of-3-valued logic circuits is described by which both combinational and sequential self-checking systems can be realized. This scheme is an example of a *circuit solution* to a *logic problem*. Further, it is an example of applying multivalued (ternary) circuits in a binary system to improve testability and reliability. This approach to the creation of a self-checking system is to be contrasted with that of conventional information redundancy (coding). It may accordingly be appropriate to call it *logic value redundancy*. It seems that a 2-of-3-valued system has the potential to provide considerably enhanced reliability and testability for a modest increase in gate circuit complexity.

Acknowledgement

This research has been supported in part by the Natural Sciences and Engineering Research Council of Canada.

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