LOW POWER 2-OF-3-VALUED CMOS SELF-CHECKING CIRCUITS

Hu, Mou*+‡ Smith, K. C.+ Mouftah, H. T.‡

Abstract

Two new schemes for the implementation of self-checking binary logic systems are proposed which utilize low power 2-of-3-valued CMOS logic circuits. While 2-of-3-valued circuits are inherently ternary, only two of their three logic values are used in normal operation. The third (middle) logic value is used for self-checking and testing. To evaluate these circuits an "open-short-conducting" fault model for CMOS circuits is developed. All the single faults in these circuits are studied and classified into four types, named mid-seeking, quasi-mid-seeking, mid-rejecting, and masked. The conclusions reached for 2-of-3-valued circuits in previous papers apply to these new circuits as well. Finally a comparison between implementation schemes is made on the basis of the size of the fault set each produces.

I. Introduction

One important application of multiple-valued logic is the creation of self-checking binary logic systems using ternary circuits (1), (2), (3). In (1), a particular kind of ternary circuit with special properties was proposed. For this circuit, called a 2-of-3-valued circuit, two of the three logic values provided are used as normal binary working values, while the surplus third logic value (the middle value) is used for self-checking and testing. In (1), 2-of-3-valued combinational systems were studied. Reference (4) extended the study to 2-of-3-valued synchronous sequential systems. There it was proved that the use of 2-of-3-valued circuits can improve system reliability and simplify fault detection procedures.

In this paper two new schemes to implement 2-of-3-valued circuits based on a low power CMOS technology (5) are proposed. An "open-short-conducting" fault model for these CMOS circuits is developed. All of the single faults in these circuits are studied and classified into four types: mid-seeking, quasi-mid-seeking, mid-rejecting, and masked. The conclusions made for earlier 2-of-3-valued circuits demonstrated in (1) and (4) still apply for these new 2-of-3-valued implementations. Finally, a comparison between schemes is made on the basis of the size of each fault set.

II. The 2-of-3-Valued Circuits

The first scheme for implementing 2-of-3-valued circuits was proposed in (1). These circuits are ternary logic circuits working in binary mode utilizing the two extreme logic values. The middle logic value is available for self-checking and testing.

In this section some important concepts and conclusions for 2-of-3-valued circuits will be reviewed. They are extracted from the original derivations in (1) and (4).

For compatibility with binary logic, 2-of-3-valued logic operators are defined in what follows. In each definition, variables $x, y \in Q$, where Q is the set of logic values, $Q=\{0,\frac{1}{2},1\}$. Let $N=\{0,1\}$ and $E=\{\frac{1}{2}\}$ be disjoint subsets of Q.

Definition 1

The Negation operator is defined as:

$$\bar{x}=1-x,$$

where "-" is arithmetic subtraction. The truth table of the Negation operator is given in Table 1. The circuit implementing the Negation operator will be called an Inverter.

x	$\bar{x}$
0	1
½	½
1	0

Table 1

* Shanghai Institute of Railway Technology, Shanghai, China

\+ University of Toronto, Toronto, Ontario, Canada

‡ Queen's University, Kingston, Ontario, Canada

0195-623X/83/0000/0064$01.00 © 1983 IEEE

Definition 2

The NAND operator is defined as:

$$\overline{x \cdot y} = 1 - \min(x,y),$$

where "min(x,y)" implies the choice of the smaller of x and y. The truth table of the NAND is given in Table 2.

x	y	$\overline{xy}$
0	0	1
0	½	1
0	1	1
½	0	1
½	½	½
½	1	½
1	0	1
1	½	½
1	1	0

Table 2

Note from Tables 1 and 2 that when the input lies in N={0,1} the truth tables revert to those of conventional binary algebra.

In 2-of-3-valued circuits, all single faults can be classified as one of four types: mid-seeking, quasi-mid-seeking, mid-rejecting, and masked. Definitions follow:

Assume that the number of inputs of a circuit G is m. With an input vector χ, and a fault f, the output of the circuit G is denoted as $G(\chi,f)$. Correspondingly the output of fault-free circuit G is denoted as $G(\chi,\phi)$.

Definition 3

A fault f is a mid-seeking fault if

$$\{\exists \chi \in N^m G(\chi,f) \in E\} \wedge \{\forall \chi \in Q^m [G(\chi,f) = G(\chi,\phi) \vee G(\chi,f) \in E]\}.$$

In other words, for a mid-seeking fault, two conditions should be met simultaneously: first that there exists at least one normal input vector, such that the output of the faulty gate is ½; and second, that for all possible input vectors, the output of the faulty gate is either correct or ½.

Definition 4

A fault f is a quasi-mid-seeking fault, if

$$\{\exists \chi \in N^m G(\chi,f) \in E\} \wedge \{\exists \chi \in Q^m [G(\chi,f) \neq G(\chi,\phi) \wedge G(\chi,f) \notin E]\}.$$

Note here, that for a quasi-mid-seeking fault, there are also two conditions. The first condition is the same as that for a mid-seeking fault. The second condition is the negation of the second condition for a mid-seeking fault.

Definition 5

A fault f is a mid-rejecting fault, if

$$\forall \chi \in Q^m \quad G(\chi,f) \notin E.$$

In other words, for a gate having a mid-rejecting fault, the output will never be ½.

Definition 6

A fault f is a masked fault, if

$$\forall \chi \in Q^m \quad G(\chi,f) = G(\chi,\phi).$$

In other words, for a gate having a masked fault, the output remains correct.

Now some definitions related to the self-checking concept will be provided. For these definitions, assume G is a logic circuit with m inputs and n outputs. F is the set of faults considered.

Definition 7

A logic circuit G is self-testing for F, if

$$\forall f \in F \ \exists \chi \in N^m \ G(\chi,f) \notin N^n.$$

That is, for all considered faults, there exists at least one normal input vector, such that the output vector of the circuit is abnormal.

Definition 8

A logic circuit G is fault secure for F, if

$$\forall f \in F \ \forall \chi \in N^m \{G(\chi,f) = G(\chi,\phi)\} \vee \{G(\chi,f) \notin N^n\}.$$

That is, for all faults considered, and for all normal input vectors, the output vector of the circuit is either correct or abnormal.

Definition 9

A logic circuit is totally self-checking for F, if

1) it is self-testing for F, and
2) it is fault secure for F.

As provided in (1), for mid-seeking and quasi-mid-seeking faults, the 2-of-3-valued combinational system satisfies the following theorem:

Theorem 1

For any mid-seeking and quasi-mid-seeking fault, any irredundant combinational logic network which consists of 2-of-3-valued Inverters and NAND gates is totally self-checking.

As proved in (4), for mid-seeking faults in a 2-of-3-valued synchronous sequential system the following theorem applies:

Theorem 2

If both output Z and internal state Y (or Z and next-state W) are observable, then for any mid-seeking fault, a 2-of-3-valued synchronous sequential machine is totally self-checking.

In (1), it was also proved that a 2-of-3-valued combinational system is fault secure for all masked faults, and easily testable for all mid-rejecting faults.

Similarly, a 2-of-3-valued synchronous sequential system is fault secure for all masked faults. However in a 2-of-3-valued synchronous sequential system both quasi-mid-seeking and mid-rejecting faults should be treated as hardcore and must be tested off-line.

III. Low Power CMOS 2-of-3-Valued Circuits

In this section, 2 schemes for the implementation of low power CMOS 2-of-3-valued circuits will be proposed. They are modified versions of a low power CMOS ternary family introduced earlier (5).

Scheme 1

Figure 1 is a 2-of-3-valued inverter utilizing a centre-tapped power supply. The input and output can take on values -V, 0, and +V. These correspond to logic values 0, ½, and 1 respectively.

For proper operation it is necessary to arrange that the power supplies (-V and +V) and the thresholds of the MOSFETs (V_T) meet the following criteria:

$$V<V_T<2V.$$

With input $\chi=-V$, P conducts, N cuts off, and the output becomes $\chi=+V$. When $\chi=0$, both P and N cut off at which time the output takes on value 0 as supplied through R_1 and R_2. When $\chi=+V$, P cutts off, N conducts, and the output becomes $\chi=-V$. In this circuit, 2 resistors, R_1 and R_2, are used in parallel to improve the fault detection capability.

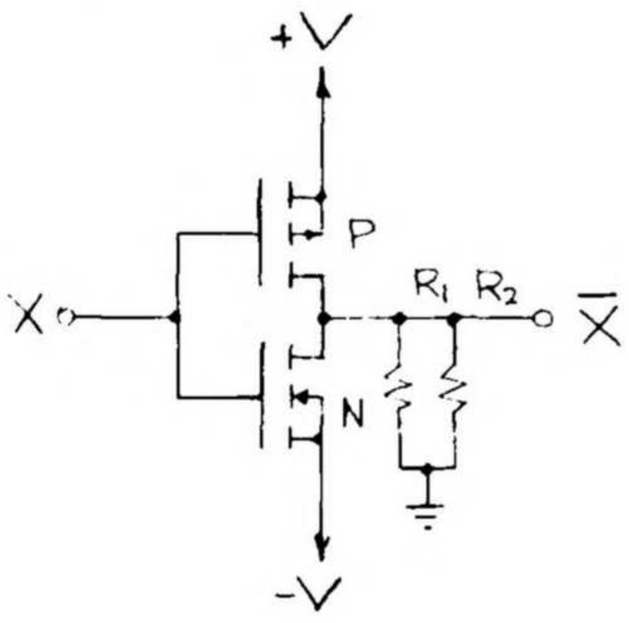


Fig. 1

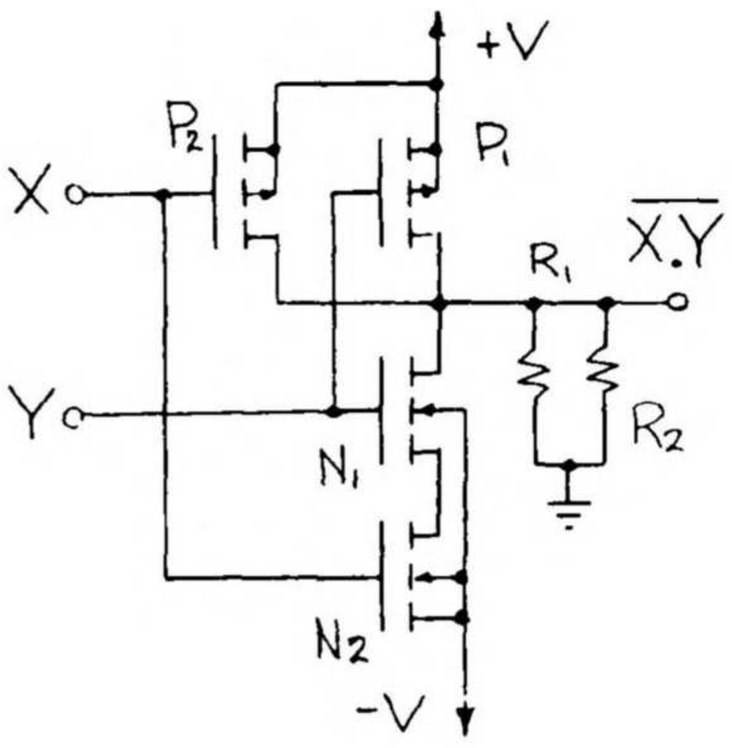


Fig. 2

Fig. 2 shows a 2-of-3-valued NAND gate. The working principle is similar to that of the Inverter. The circuit in Fig. 2 can be augmented with additional inputs.

Scheme 2

Fig. 3 is a second 2-of-3-valued Inverter, utilizing only two power supply connections. Note that the connection of R_1 and R_2 differs from that in Fog. 1. As a result the power supply requirement is reduced from a need for matched supplies to a requirement for only a single one. However, in this circuit R_1 and R_2 have to be matched.

The required relationship between V and V_T is

$$½V<V_T<V.$$

The operation of this circuit is similar to that of the circuit of Fig. 1. The corresponding NAND gate is shown in Fig. 4

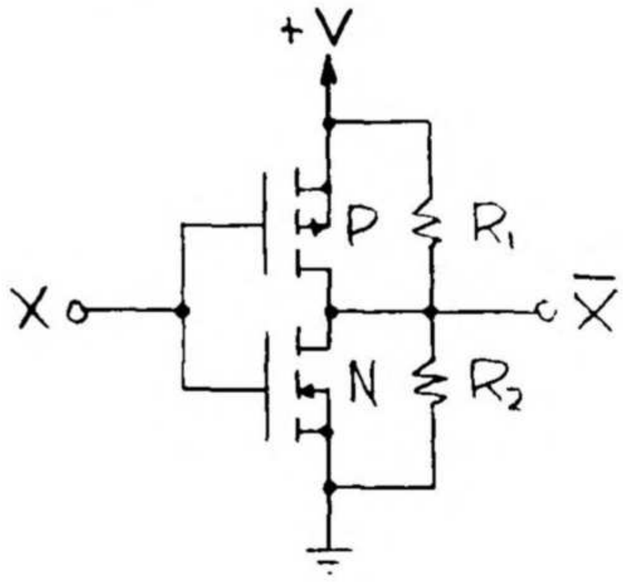


Fig. 3

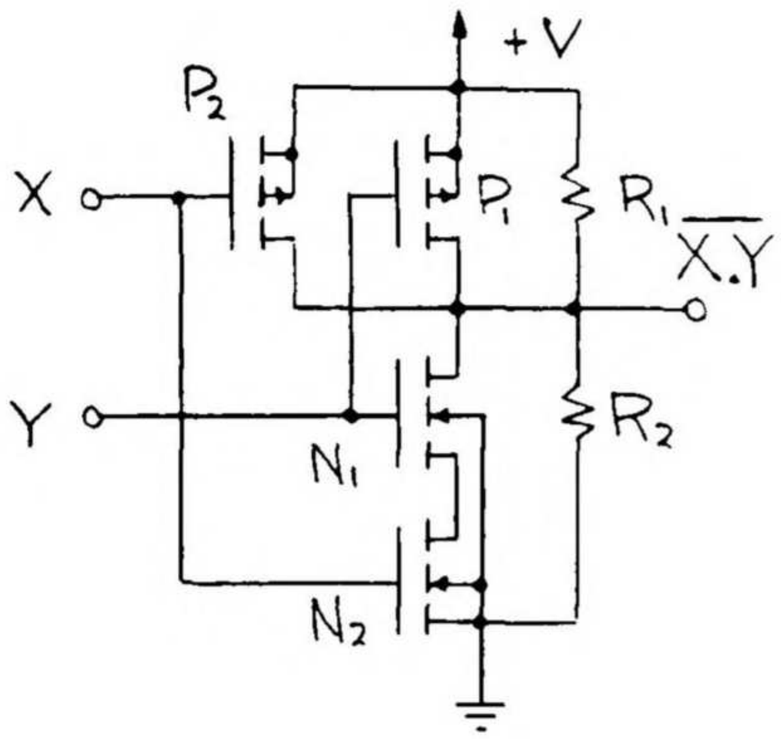


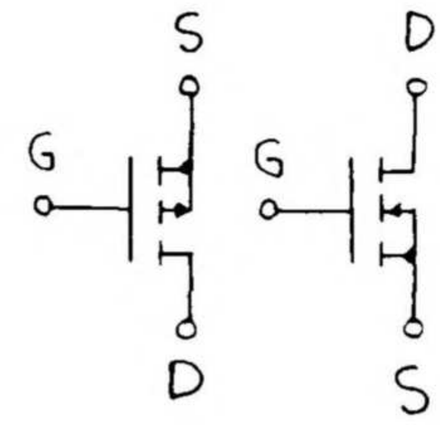
Fig. 4

Each of these gates has been built and tested using 4007, 4069, and 4011 IC's with power supply V=1V and $R_1=R_2=50K$.

IV. Fault Analysis

Before we proceed to fault analysis it is necessary to establish a fault model: first of all the conventional single fault assumption is adopted, that is, that at any instant there exists at most one fault.

It is considered that a fault may be either a *resistor fault or a transistor fault. A resistor* fault results in either a resistor short condition or a resistor open condition. A transistor fault results in one of the following three conditions: source-drain (SD) shorted, SD open, or SD always conducting. Further such a fault is assumed to derive from explicit device interconnection failures. As shown by Fig. 5, if any one of the connections S, D, and G is open or if any two of them are shorted, the equivalent effect will be one of the three fault conditions: SD short, SD open, or SD always conducting*. The two conditions of SD short and SD always conducting are distinguished in view of the fact that for SD always conducting the equivalent SD resistance is not zero.



Cause	Effect
D open	SD open
S open	SD open
G open	SD open or SD conducting
DG short	SD conducting
GS short	SD open
SD short	SD short

Fig. 5

With the fault model described, the fault characteristics of the new 2-of-3-valued circuits can be evaluated. The results of analysis (and experimental verification) are shown in Tables 3, 4, 5, and 6, for Inverter 1, Inverter 2, NAND 1, and NAND 2, respectively.

In these tables, the notation "S" is used to denote a resistor short or a transistor SD short, "0" is used to denote a resistor open or a transistor SD open, and "C" is used to denote a transistor which is always conducting.

		mid-seeking				mid-rejecting				masked	
x	$\bar{x}$	P_o	N_o	R_{1S}	R_{2S}	P_s	N_s	P_c	N_c	R_{10}	R_{20}
0	1	½	1	½	½	1	0	1	1	1	1
½	½	½	½	½	½	1	0	1	0	½	½
1	0	0	½	½	½	1	0	1	0	0	0

Table 3

		mid-seeking		mid-rejecting							
x	$\bar{x}$	P_o	N_o	R_{1S}	R_{2S}	P_s	N_s	P_c	N_c	R_{10}	R_{20}
0	1	½	1	1	0	1	0	1	1	1	1
½	½	½	½	1	0	1	0	1	0	0	1
1	0	0	½	1	0	1	0	1	0	0	0

Table 4

---

* It has to be noted that there could be a fourth condition, that is, SD always cut off. However in this case the current is so small that it can be considered as zero. Thus SD always cut off is considered equivalent to SD open.

					mid-seeking				quasi-mid-seeking				mid-rejecting				masked	
x	Y	$\bar{Y}$	P_{10}	P_{20}	N_{10}	N_{20}	R_{1S}	R_{2S}	N_{1S}	N_{1C}	N_{2S}	N_{2C}	P_{1C}	P_{2C}	P_{1S}	P_{2S}	R_{10}	R_{20}
0	0	1	1	1	1	1	½	½	1	1	1	1	1	1	1	1	1	1
0	½	1	½	1	1	1	½	½	1	1	1	1	1	1	1	1	1	1
0	1	1	½	1	1	1	½	½	1	1	1	1	1	1	1	1	1	1
½	0	1	1	½	1	1	½	½	1	1	1	1	1	1	1	1	1	1
½	½	½	½	½	½	½	½	½	½	½	½	½	1	1	1	1	½	½
½	1	½	½	½	½	½	½	½	0	0	½	½	1	1	1	1	½	½
1	0	1	1	½	1	1	½	½	1	1	1	1	1	1	1	1	1	1
1	½	½	½	½	½	½	½	½	½	½	½	½	1	1	1	1	½	½
1	1	0	0	0	½	½	½	½	0	0	0	0	1	1	1	1	0	0

Table 5

			mid-seeking		quasi-mid-seeking				mid-rejecting							
x	Y	$\bar{Y}$	P_{10}	P_{20}	N_{10}	N_{20}	N_{1S}	N_{1C}	N_{2S}	N_{2C}	P_{1C}	P_{2C}	P_{1S}	P_{2S}	R_{1S}	R_{2S}	R_{10}	R_{20}
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	½	1	½	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	½	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
½	0	1	1	½	1	1	1	1	1	1	1	1	1	1	1	0	1	1
½	½	½	½	½	½	½	½	½	½	½	1	1	1	1	1	0	0	1
½	1	½	½	½	½	½	0	0	½	½	1	1	1	1	1	0	0	1
1	0	1	1	½	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	½	½	½	½	½	½	½	½	0	0	1	1	1	1	1	0	0	1
1	1	0	0	0	½	½	0	0	0	0	1	1	1	1	1	0	0	0

Table 6

Furthermore, following Definitions 3, 4, 5, and 6, all single faults have been classified into one of the four types.

As mentioned in Section II, for mid-seeking faults, both 2-of-3-valued combinational systems and 2-of-3-valued synchronous sequential systems are totally self-checking. Accordingly our goal is to arrange to make the set of mid-seeking faults as large as possible.

For quasi-mid-seeking faults, only the 2-of-3-valued combinational system is totally self-checking. In a 2-of-3-valued synchronous sequential system, quasi-mid-seeking faults must be treated as hard-core. On the other hand, in both the combinational system and synchronous sequential system mid-rejecting faults must be tested off-line. Thus quasi-mid-seeking faults are preferable to mid-rejecting faults.

Since masked faults do not produce errors immediately at the system output, they are undetectable by conventional means. They can however be detected using other techniques utilizing power supply current measurement. Since the accumulation of masked faults will ultimately produce errors, they must be analysed carefully.

In the inverter shown in Fig. 1, there are two masked faults, R_{10} and R_{20}. If only one of them has occurred, the system continues to operate correctly. However if both R_{10} and R_{20} occur, and input $x=\frac{1}{2}$ is applied, then output $\bar{x}$ becomes floating (indeterminate) instead of $\frac{1}{2}$. When the circuit is under test, this constitutes an error. Furthermore this will cause the circuit to lose its self-testing ability. In other words, if a third fault occurs, even a mid-seeking fault, the system is not self-testing.

For the NAND gate shown in Fig. 2, the situation is similar. However the inverter shown in Fig. 3, and the NAND gate shown in Fig. 4, have no masked faults.

V. Scheme Comparison

To provide a meaningful comparison of the two schemes for self-checking circuits, some quantitative measures appropriate to 2-of-3-valued circuits are required.

Such has been the attempt by Lu in [6], in which some measures for self-checking circuits are defined. However they are not suited for 2-of-3-valued circuits. Thus a different approach based on the size of the four fault sets has been adopted. For each fault set, a self-checking factor C is assigned. For mid-seeking faults, the self-checking factor C_s takes value 1 since the circuit is totally self-checking. Likewise, for mid-rejecting faults, the self-checking factor C_r will be 0 since the circuit is not self-checking. For quasi-mid-seeking faults, the self-checking factor C_q takes on a value smaller than 1, yet larger than 0.

For masked faults, the value of the self-checking factor C_m varies from a negative value (see below) to a positive value less than 1 depending on the situation. If the system is used in an environment in which periodic off-line test is impossible and the mission time is quite short, masked faults are preferred to mid-rejecting faults and quasi-mid-seeking faults, since they do not cause an error at the output. Thus, $C_m > C_q$. On the other hand, if periodic off-line test is possible, and the mission time is quite long then mid-rejecting and quasi-mid-seeking faults are preferable, because masked faults are more difficult to test even in an off-line manner and because the accumulation of masked faults will ultimately cause errors. In this situation, $C_m < C_r$, requiring that it takes on a negative value.

Now let us compare the two schemes presented in Section III.

For the case in which the periodic off-line test is impossible and the mission time is quite short, the following values are assigned: $C_s=1$, $C_m=0.6$, $C_q=0.3$, and $C_r=0$. Note that the absolute values are somewhat arbitrary.

The self-checking factor for the entire circuit is: $C=C_S\cdot\frac{N_S}{N}+C_q\cdot\frac{N_q}{N}+C_r\cdot\frac{N_r}{N}+C_m\cdot\frac{N_m}{N}$, where N is the total number, N_S is the mid-seeking fault number, N_q is the quasi-mid-seeking fault number, N_r is the mid-rejecting fault number and N_m is the masked fault number.

For Inverter 1, N=10, $N_S=4$, $N_q=0$, $N_r=4$, and $N_m=2$.

Thus, $C=1\times\frac{4}{10}+0+0+0.6\times\frac{2}{10}=0.52$.

For Inverter 2, N=10, $N_S=2$, $N_q=0$, $N_r=8$, and $N_m=0$.

Thus, $C=1\times\frac{2}{10}+0+0+0=0.2$.

For NAND 1, N=16, $N_S=6$, $N_q=4$, $N_r=4$, and $N_m=2$.

Thus, $C=1\times\frac{6}{16}+0.3\times\frac{4}{16}+0+0.6\times\frac{2}{16}=0.525$.

For NAND 2, N=16, N_S=4, N_q=4, N_r=8, and N_m=0.

$$\text{Thus, } C=1x\frac{4}{16}+0.3x\frac{4}{16}+0+0=0.325$$

Obviously on this basis, scheme 1 is better than scheme 2 when off-line test is impossible and mission time is quite short.

However, if periodic off-line test is possible and the mission time is quite long, the following values can be assigned: C_S=1, C_q=0.3, C_r=0, and C_m=-0.3 in which case: For Inverter 1,

$$C=1x\frac{4}{10}+0+0+(-0.3)x\frac{2}{10}=0.34$$

For Inverter 2,

$$C=1x\frac{2}{10}+0+0+0=0.2.$$

For the NAND 1,

$$C=1x\frac{6}{10}+0.3x\frac{4}{16}-0.3x\frac{2}{16}=0.41.$$

For the NAND 2,

$$C=1x\frac{4}{16}+0.3x\frac{4}{16}+0+0=0.325.$$

Thus even for this situation, scheme 1 is still better than scheme 2. However it should be noted that scheme 2 requires only a single power supply. As well scheme 2 has no masked faults. Thus in these respects scheme 2 may be preferred to scheme 1.

II. Conclusions

In this paper, the important concepts of 2-of-3-valued circuits are reviewed and two new schemes for implementing 2-of-3-valued circuits are proposed. An "open-short-conducting" fault model is developed. Fault analysis is persued using this model. Finally a quantitative measure based on the size of each fault set is proposed. Two new schemes are compared using this method.

References

1) Mou Hu and K.C. Smith, "On the Use of CMOS Ternary Gates to Realize a Self-Checking Binary Logic System". Proceedings of the Eleventh International Symposium on Multiple-Valued Logic. pp. 212-217, May 1981.

2) K.C. Smith, "The Prospects for Multivalued Logic: A Technology and Application View", IEEE Trans. on Computers, Vol. C-30, No. 9, pp. 619-634, Sept. 1981.

3) F.F. Sellers, Jr., Mu-Yue Hsiao, and L.W. Bearnson, "Error Detecting Logic for Digital Computers", McGraw-Hill Book Company, pp. 143-145, 1968.

4) Mou Hu and K.C. Smith, "A New Type of Self-Checking Synchronous Sequential Machine Based on 2-of-3-Valued Logic Circuits". Proceedings of 12th International Symposium on Multiple-Valued Logic, pp. 139-145, May 1982.

5) H.T. Mouftah and K.C. Smith, "Injected Voltage Low Power CMOS for Three-Valued Logic", submitted for publication.

6) D.J. Lu, "Quantitative Measures and Figure of Merit for Self-Checking Circuits", CRC Technical Report No. 81-8, Stanford University Aug. 1981.