Development and Integration of a Micro-Computer based
Image Analysis System for Automatic PCB Inspection

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Abstract

Automated inspection of Printed Circuit Boards(PCB's) is essential if 100% repeatible inspection is to be carried out. The cost of most commercially available systems for automatic visual inspection of PCB's are beyond the reach of many small to medium manufacturers. The principle objectives of our research is to develop and integrate a micro-computer based image analysis system specifically for these manufacturers. The feasiblility of using a low-cost hardware system is under investigation, while efficient inspection techniques based on software are being developed in the Robotics and Automation Laboratory(RAL) at the University of Toronto.

1. Introduction

Research in the area of PCB inspection has been on-going since the nineteen-seventies, with many of these research projects yielding commercially-available inspection systems [1,2]. Despite the availability of such systems, the majority of small to medium size PCB manufacturers still use manual labour to perform the board inspection [3]. The main objective of our research, reported in this paper, is to develop a low-cost and cost-efficient image analysis system for these manufacturers.

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1.1 Reference and non reference inspection systems. The different types of PCB inspection systems developed can be classified into two main categories. These are the reference and the non-reference inspection systems. Reference inspection systems compare some of the features of the board being inspected with those of a known "good" board. Non-reference inspection systems, on the other hand, use design rules to analyze the image of the board. Each of the above has its advantages and disadvantages.

An example of a reference inspection system is image subtraction [4]. With this technique, a stored binary image of a "good" board is compared with the binary image of the board being inspected. The differences between these two images is then analyzed to determine if any flaws have occured. The advantage of this system is that it is easy to implement with hardware, and therefore high processing rates are possible. Another advantage of this system is that large defects (ie. missing conductor wires, etc.) can be detected whereas the non-reference systems will not detect these. The main disadvantages of this system are: 1) normal variations in the PCB production will cause many false alarms in the system, and 2) accurate alignment of the board is essential, which requires a very precise mechanical device to move the board.

Examples of non-reference inspection techniques are: run-length based analysis, template matching, and morphological techniques.

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In run-length based analysis, the circuit board is scanned and run-length information on the board is processed [5]. The run-length information extracted may include the maximum and minimum conductor width encountered, the inter-conductor spacing, etc. The run-length analysis can be implemented in hardware, and therefore can be carried out very fast.

Template matching inspection techniques use a collection of templates of known good (or bad) features of the board [6]. The features of the board are extracted, and compared to these templates. By matching the templates, the location and type of flaws in the image can be determined. This method has the advantage of greatly reducing the image data for storage, and at the same time reduces the sensitivity of analysis of the gray- scale data.

Morphological techniques use well known expansion and contraction operations on the binary PCB image [7]. The expansion process tends to fill in pinholes and scratches on the conductor, while the contraction process tends to eliminate shorts between circuits. The resulting image after the morphological processing is then analysed to determine if there are any flaws present.

1.2 Future inspection sytems. With the performance/cost ratio of modern computers increasing, as well as with the cost of image processing equipment decreasing, it should soon be possible to produce a Printed Circuit Board (PCB) inspection system that is cost effective for the small to medium size PCB manufacturers.

Such a system is being developed at the RAL. The current system consists of a Matrox video-digitizer, a JVC CCD camera, a Canon 100mm Macro-lens, an IBM-AT compatible computer, various fiber-optic illumination equipment, an X-Y table, as well as image processing software. A SUN workstation is also being used for software development. The work carried out in the development of the inspection systems has been divided into three

main areas. These main areas are: 1) illumination, 2) filtering, and 3) flaw detection. Each of these areas are discussed in detail in the following sections.

2. Illumination

The lighting of the PCB is critical to the flaw detection process. The aim of the lighting is to maximize the intensity of the reflection of light from the conductor onto the camera, while minimizing the intensity of reflection of light from the substrate (i.e. maximize contrast). This is used to reduce the complexity of the image processing. In order to produce the best contrast of the image, the spectral reflective properties of the conductor and the substrate must be investigated. The differences in the spectral responses of the conductors and the substrate must then be capitalized on. Ideally, the two materials will have completely different spectral profiles, as in figure 1. As can be seen, a simple wavelength cutoff of the
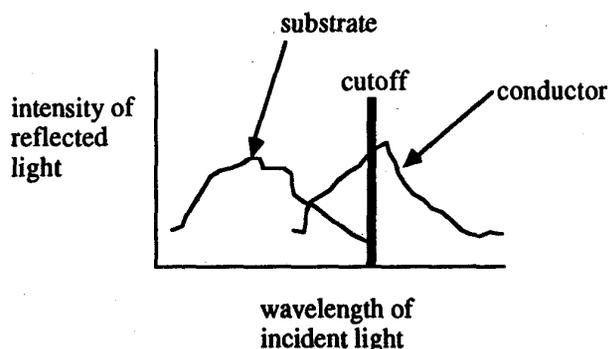

Figure 1. Ideal spectral response of board

reflected light will produce a good image of the conductor. However, unless the substrate has been specially treated, this will not be the case.

Silver conductors reflect light across the visible spectrum. Since the substrate has similar reflective properties, we have not found the use of special band-pass filters effective. The lighting of the conductor and the substrate must, thererefore, capitalize on the differences in the intensities of reflection from the conductors and substrate.

Insofar as acquisition of a quality image is concerned, the main parameters which characterize suitability of lighing are its spectral distribution, intensity, uniformity, and directionality. The relative importance and optimaization of these parameters and the degree to which each must be controlled is largely governed by the surface characteristics of a given PCB, and the constraints imposed by the camera.

2.1 The Final Lighting Design. Several different lighting techniques were tested at the RAL. The techniques included the use of a fluorescent ring light, fiber-optic ring lighting, fiber-optic side illumination, as well as back lighing. Each of these were evaluated at various angles and positions, with and without diffusers of various shapes. The PCB used to evaluate the illumination included boards with several different types of solder-masks, as well as boards with no solder mask.

The best images we obtained were from PCB's with a smooth lightly coated solder-mask. Good images were also obtained from boards without a solder-mask. The optimum illumination determined for these types of boards is shown in figure 2. In the case of PCB's without a solder-mask, incident light in the range of $\theta = 45$ to $\theta = 90$ (θ is the angle from the normal of the substrate) was required to detect those conductor parts with high oblique angles (relative to the normal of the substrate). However, doing this substancially decreased the signal to noise ratio and was therefore unacceptable.

The beam splitter was inserted into the system to reflect light directly down onto the board surface. This, combined with the ringlight, resulted in incident lighting on the board from $\theta = 0$ to $\theta = 45$ degrees. Without the beam splitter, the middle of the conductors, corresponding to the flat horizontal conductor surfaces, showed false voids.

For the PCB's with glossy heavily-pitted solder masks, the method shown in figure 2 produced unacceptable images. For this type of board, the signal to noise ratio was at an optimum level when the board was omni-directionally illuminated with the range of $\theta = 0$ to $\theta = 25$ degrees.
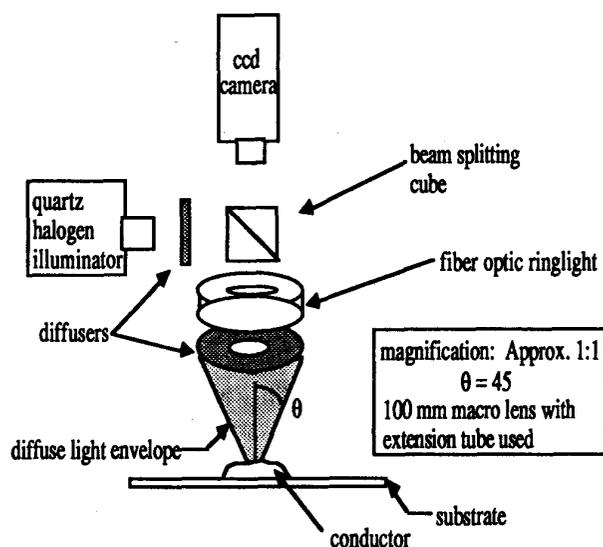

Figure 2. Diffused illumination.

For most PCB's, the experimental work done so far strongly seemed to indicate that the method of figure 2 was very close to having optimized three of the four main parameters related to the regulation and manipulation of light (i.e. intensity, uniformity, and directionality).

Insofar as spectral distribution of light is concerned, selection of a quartz halogen source is fairly compatible with the CCD camera used. It is suspected that the conditioning of light using colour and/or polarizing filters should

help to improve quality of some images, but not enough experimental work has been done to give reliable conclusions. More research will be carried out in order to optimize this part of the illumination.

3. Filtering

The objective of the filtering process is to output a binary image of the PCB that is suitable for processing by the flaw detection algorithms. It is also essential that this binary image be output as quickly as possible.

For the PCB inspection system, there are two processes required in the production of the binary image. One process is the transformation of the image from gray scale to binary. The second process required is the enhancement of the image. This image enhancement is carried out before and after the gray scale to binary image transformation. The following sections describe the binary image extraction algorithms, followed by a description of the image enhancement algorithms.

3.1 Binary Image Extraction. Two methods of transforming the gray scale image to a binary image were examined. The two methods tested were edge detection and thresholding. In edge detection, the gray scale image is scanned, and the edge of the conductors are determined. The pixels inside the conductor edges are assigned a one value, and all other pixels are assigned a zero value. In thresholding, all pixel values below a cutoff value are assigned the value zero, and all other pixels are assigned the value one. Both of the above methods were evaluated in order to determine the most suitable process for our system.

In our research, using the lighting as described previously, we determined that the use of edge detection algorithms produced rough edges with interspersed gaps. Laplacian edge detection algorithms produced thin lines with many gaps [8]. Sobel and Robert's edge detection algorithms gave wide band edges [9]. In both cases the results were difficult to interpret and cumbersome to use. It was found that if good edges could be pulled from a gray scale image,

the use of thresholding would result in an even better binary image which was less sensitive to noise.

As described above, the thresholding method of transforming the gray scale image into binary form involves simply setting all pixel values to a value of zero or one depending on whether the individual pixel gray scales values were above or below a specified cut-off (or threshold) value. The difficulty with this method is knowing what the cut-off value should be. Subsequent work has pursued the development of automatic threshold selection algorithms.

The first automatic thresholding technique developed capitalizes on the fact that the optimum cut-off value lies somewhere between the average gray scale values of the conductors and the average gray scale value of the substrate. The cut-off value to be determined would, therefore, most likely occur in the region where the conductors and the substrate meet (i.e. the edges). By using a Laplacian edge detection algorithm, followed by a normalization routine, and then a thresholding, the approximate location of the conductor edges can be found. These edge pixels gray scale values can then be averaged, and multiplied by a constant. The resulting number would be the required threshold value. The value of the multiplication factor depends on the technique used to find the edge pixels. The median value of several readings from a sample set of boards can determine the thresholding value for that batch of boards.

Another technique for automatically determining a threshold cutoff value is presently being evaluated. A known conductor pattern on the PCB is imaged. The image is then continually processed at different cut-off values, until the binary image matches some preset standard. Different evaluation standards are possible. The current standard under evaluation is the matching of a measured conductor width with that of a stored width.

3.2 Image Enhancement.

Various algorithms were tested to determine the optimum image enhancement filters for our system. A low pass filter, such as a median filter (or averaging, homomorphic, or logarithmic filter[8]) was found to have a beneficial effect on unmasked boards with rough conductors when used before the image was converted to binary form. The rough surface of the conductors reflected light such that a straight thresholding of the image produced false lines and voids on the conductors. The median filter had a smoothing effect and resulted in a significant improvement in the subsequent binary image. Median filters were not found to be as effective on masked boards since the masks already acted as low pass filters. However, since inspection of the PCB after the appplication of the solder-mask complicates board rework, the inspection should normally be carried out before the mask application.

Other image enhancement operations were performed after the image was converted to binary format. The noise inherent in the operation of the system and caused by the imperfect lighting conditions was removed by shrinking and expanding the white conductors of the binary image [10]. This was done with convolution algorithms [9]. For binary images with only fine noise, modified expansion or contraction convolutions were used.

4. Inspection

As described previously, various effective image analysis techniques have been developed to automatically detect flaws in printed circuit boards. Reference inspection systems compare features of a known good board to features of the board being inspected. As the exact position of the PCB must be known, these reference inspection systems require an expensive and precise X-Y table. Non-reference inspection systems, on the other hand, do not require the exact positioning of the PCB. The X-Y table used to move the PCB is therefore not required to be as precise as those required for the reference inspection systems. In order to minimize cost, a non-reference inspection system is being investigated. The present system under development in the RAL uses a combination of template matching and dimensional verification for flaw detection.

A list of the types of flaws that occur on PCB's is shown in Table 1. This table also includes the probable rate of occurance of these flaws. Using the data shown in Table 1, the majority of PCB flaws can be located by searching for the first four flaws. The present system has been developed to detect all of the shown flaws, with the exception of: missing wire, wrong size of hole, hole missing, and incorrect spacing of holes. Inspection for the above flaws are not critical as long as the PCB is designed well and the "first" board produced is closely inspected.

PCB FLAW	OCCURENCE OF FLAW	PCB FLAW	OCCURENCE OF FLAW
MOUSEBITE	H	OVERETCH	M
OPEN CIRCUIT	H	UNDERETCH	M
SHORT CIRCUIT	H	WRONG SIZE OF HOLES	L
BREAKOUT	M-L	CONDUCTORS TOO CLOSE	L
MISSING WIRE	L	CONDUCTORS TOO CLOSE	L
SPURIOUS COPPER	L	HOLE MISSING	L
PINHOLE	M-L	SPACING OF HOLES	L

OTHERS: - CRACKS,CHIPS OR BULGES ON BOARD SURFACE
- WARP OR TWIST OF BOARD
- CRACKING OF WALLS OF HOLES
- SPURS OR WHISKERS

H = HIGH
M = MEDIUM
L = LOW

Table 1. PCB Flaws

4.1 Flaw detection algorithms.

In the normal use of dimensional verification, the dimensions of the conductors, the dimensions of the pads, as well as the inter conductor spacing are measured, and compared against pre-set tolerances. To implement this technique, the conductor edges must be located, and then, if minimum and maximum conductor tolerances are

specified, the orientation of these edges must also be determined. The cross-sectional dimensions of the conductors can then be measured.

In order to speed up the dimensional verification processing, the number of points measured along the conductors must be minimized. One technique of doing this is to measure the dimensions of the conductor every Nth pixel length along the conductor. The appropriate N value depends on the minimum conductor width as well as the tolerances specified. However, the use of this technique may overlook such flaws as open circuits or short circuits.

The present technique being investigated at the RAL is to use template matching of the conductor edges to determine the locations of the required measurements. The template matching method assumes that the edge pattern of the flaws will be non-uniform. By comparing conductor edge patterns with a small table of good template edge patterns, the areas of potential faults can be detected. There is obviously a relationship between the number of templates used and the number of locations to be measured with dimensional verification. The greater the number of good templates used, the smaller the number of dimensional measurements that will be required. This relationship is presently being investigated to determine the optimum set of templates. The use of filtering techniques to reduce the number of templates required is also being investigated.

The template matching method being developed therefore does not attempt to locate the PCB flaws, but tries to eliminate the measurement of conductor dimensions in locations where the likelyhood of a flaw occurance is low. The succesful implementation of this method is very dependent on the lighting and filtering techniques used.

4.2 Tolerance generation. Two different techniques can be used to generate the tolerances used by the inspection system. The conductor dimensions and tolerances can be input manually, or an automatic self-programming tolerance procedure can be used. This automatic self-programming procedure is valuable when the board to be inspected does not follow simple dimensional rules.

In the automatic tolerance input procedure developed, the PC board is broken into physical zones, corresponding to the areas to be inspected. Each individual zone is then scanned, and the zone average of the conductor width, inter-conductor spacing, as well as the hole parameters is determined. When conductors of different width are present in the image, width averages are calculated for each seperate conductor. In this way, the conductor tolerances are determined for each seperate zone. This data is used to generate absolute tolerances (in pixels) for each seperate zone. The conductor width, inter conductor specing, as well as the hole and land diameter tolerances are all set as a percentage of the measured dimensions. The operator also has the option of changing these pre-set tolerances as required.

5. Conclusions

An automatic inspection system based on dimensional verification and template matching is being developed. This system is targeted for the small to medium size PCB manufacturers. Considerable work has been done in the development of the illumination and filtering used by this system. As processing costs diminish it will soon be possible that, by optimizing the balance between hardware and software, a cost effective inspection system will be developed for the small to medium size PCB manufacturers.

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