V. Conclusion

An experimental video 10-bit ADC has been designed and fabricated using BiCMOS circuit and process technology. The test chip does not include the sample-and-hold function. The new subranging configuration utilizing CMOS analog switches and bipolar high-speed high-accuracy comparators has been adopted. The results are a 10-bit 10-MHz operation, less than 4 mV of the linearity error, and -75 dB of the noise level with a 30-kHz bandwidth. The possibility of realizing a video 10-bit ADC has been confirmed. As the used design rule is only 3 μm, we can expect a higher frequency operation and a smaller chip size by using a further reduced version of the devices. Problems left for the future are to achieve 20-MHz operation, protection circuitry, and on-chip sample and hold.

References

[1] T. Takemoto *et al.*, "A fully parallel 10-bit A/D converter with video speed," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp. 1133–1138, Dec. 1982.

[2] F. Goodenough, "Single-chip 10-bit flash ADC samples at a 50-MHz rate," *Electron. Des.*, vol. 35, no. 20, pp. 49–52, Sept. 3, 1987.

[3] T. Fleming, "Analog/digital and digital/analog data converters," *EDN*, vol. 31, no. 11, pp. 102–116, May 29, 1986.

[4] T. Shimizu *et al.*, "A 10b 20MHz two-step parallel ADC with internal S/H," in *ISSCC Dig. Tech. Papers*, Feb. 1988, pp. 224–225.

Using Active Components to Perform Voltage Division in Digital-to-Analog Conversion

CHU PHOON CHONG, KENNETH C. SMITH, FELLOW, IEEE, AND ZVONKO G. VRANESIC, SENIOR MEMBER, IEEE

Abstract **— A new design of a voltage-mode D/A converter using only fabrication steps required by the MOSFET's is described. The new D/A converter is implemented using a new basic-circuit-building block called the Three-Input AMPlifier (TIAMP) which can perform voltage addition and voltage division by two without using any passive component.**

I. Introduction

General trends in the development of digital systems clearly predict the continuing emergence of highly complex, sophisticated, or "intelligent" chips. They will incorporate both complex digital assemblages and analog (sub) systems for interfacing and (possibly) special signal processing. Such on-chip analog (sub) systems certainly include A/D and D/A converters. But, since the digital system is likely to be complex and therefore to occupy most of the chip, any special fabrication steps required by the analog part will significantly impact the cost. Therefore, for such a hybrid chip, one needs analog techniques that do not use precise, well-matched, or highly linear passive components, nor employ corresponding processing steps unnecessary for digital circuits. This paper addresses the issue of such low-cost analog subsystems with emphasis on D/A conversion.

One important process of D/A conversion involves voltage division (by 2) and summation. Conventionally, voltage normally uses passive components. Consequently, at present, all voltage-mode D/A converters require linear well-matched components, resistors (nickel chrome), or capacitors (double polysilicon) whose processing cost is high.

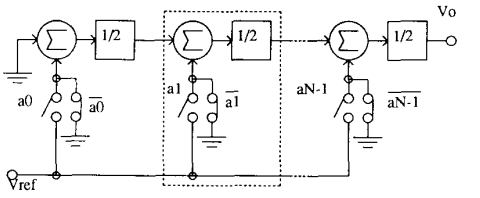

Fig. 1. D/A converter using voltage summers.

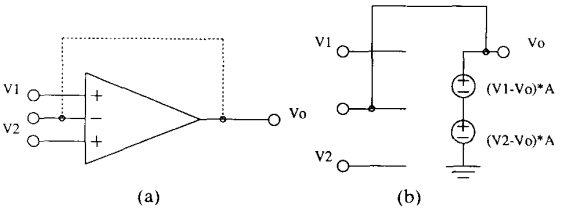

Fig. 2. (a) The TIAMP and (b) its equivalent circuit.

In this paper, we describe a voltage-mode D/A conversion technique that eliminates the need for passive components in performing voltage division. Any fabrication process designed for digital circuits may be used to implement the proposed technique with accuracy appropriate for telecommunication applications.

II. A New D/A Converter Implementation

Conceptually, the simplest and most straightforward form of D/A converter can be modeled as a cascade of voltage summers as shown in Fig. 1. Each summer sums the output of the preceding one with the ground potential or the reference voltage,[1] depending on the corresponding bit. Half the corresponding sum is provided as the output voltage of each stage. The output voltage of the entire D/A converter, which appears at the end of the amplifier cascade, may be written as

$$V_o = 1/2 V_{\text{ref}} \left\{ a_{N-1} + a_{N-2} 2^{-1} + \cdots + a_1 2^{2-N} + a_o 2^{1-N} \right\}. \quad (1)$$

The long signal path traveled by the least-significant-bit (LSB) voltage requires the use of fast voltage summers to ensure a reasonable speed of operation. Nevertheless, for an accuracy better than 0.5 LSB, the LSB component of the output voltage of the D/A converter must settle only to 50 percent. Since all but the last of the voltage summers drive an internal node with very small parasitic capacitance, any reasonable amplifier with suitable compensation should allow operation at 100 kHz or above.

The only parameter that affects the (differential and integral) linearity of the D/A converter is the gain of the voltage summer. Modest accuracy requires the use of a voltage summer with reasonably well-controlled gain (for example, less than 0.2-percent gain error for an 8-bit accuracy).

It is obvious that the voltage summer may be implemented using operational amplifiers and a number of well-matched resis-

Manuscript received November 15, 1988; revised May 2, 1989.

The authors are with the Department of Electrical Engineering, University of Toronto, Toronto, Ont., M5S 1A4, Canada.

IEEE Log Number 8929347.

[1] In some cases, the ground potential may be varied to bias the voltage summer in a more linear region of operation.

0018-9200/89/0800-0999$01.00 ©1989 IEEE

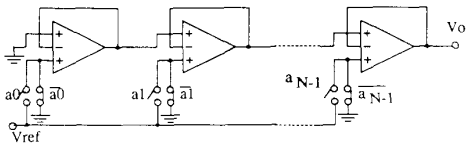

Fig. 3. D/A converter using three-input amplifiers.

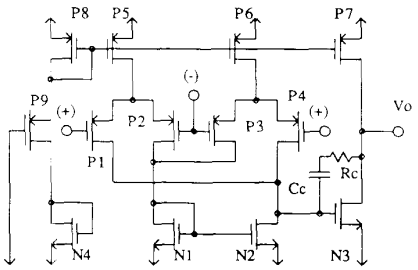

Fig. 4. Basic TIAMP implementation.

tors, which, however, are difficult to implement on chip. A more appropriate approach is to use the Three-Input AMPlifier (TIAMP) shown in Fig. 2 [1]. The TIAMP has two channels which are ideally perfectly matched. If the gain of each of the two channels is A, then the output voltage of the TIAMP may be expressed as

$$V_o = \frac{V_1 + V_2}{2}\left[\frac{2A}{1+2A}\right]. \tag{2}$$

If $A \gg 1$, then $V_o = (V_1 + V_2)/2$. Thus, the TIAMP, connected in a closed-loop configuration, acts as a voltage summer with a gain of one-half or, alternatively, as an averager.

If we denote the open-loop gain of each channel as $A = A_o/j\omega$, then (2) becomes

$$V_o = \frac{V_1 + V_2}{2}\left[\frac{2\omega_u}{2\omega_u + j\omega}\right]. \tag{3}$$

It follows that the closed-loop 3-dB bandwidth of the voltage summer is twice that of the open-loop unity-gain bandwidth of each channel. The extension of the closed-loop bandwidth beyond the open-loop unity-gain bandwidth is uniquely a characteristic of the TIAMP. From (2), the closed-loop-gain error due to the finite open-loop gain may be expressed as $\epsilon = 1/(1+2A_o)$, which shows that the closed-loop-gain error is at least twice less sensitive to the open-loop gain than an equivalent circuit implemented using an op amp [1]. It is obvious that the TIAMP, with its wide closed-loop bandwidth and lower sensitivity of closed-loop gain to open-loop gain, is an ideal building block for the implementation of the voltage summer used in the cascade D/A converter. The resulting D/A converter, implemented using the TIAMP, is shown in Fig. 3.

III. Circuit Implementation of the TIAMP

The TIAMP may be realized simply as shown in Fig. 4. The input stage consists of two differential pairs. Unlike the situation in the conventional operational amplifier, the voltage across the inputs of each differential pair is not zero, but rather half of the difference of the two input voltages of the voltage summer. To accommodate the large input voltage swing inherent in this mode of operation, the biasing gate–source voltages of the differential pair must be large. This requires the use of MOSFET's having a small aspect ratio. The relationship of the transistor sizes and the input-voltage swing is best summarized by the following equation [1]:

$$V_{i\max} = 2\left[\frac{T_{5,6}}{T_{1,4}}\right]^{1/2}\left(V_{gs5} - V_T\right) \tag{4}$$

where $T_{1,4}$ is the aspect ratio of P_1–P_4, $T_{5,6}$ is the aspect ratio of P_5 and P_6, and $V_{i\max}$ is the maximum voltage drop across the two inputs of a differential pair. We note that by splitting the connection between the gates of P_2 and P_3 to create an additional input, a four-input amplifier known as a "differential difference amplifier" can be created, as has been proposed independently by Säckinger and Guggenbühl [2].

Mismatches can occur only in the input stage since the second stage is common to both channels. The following relationships have been shown in [1].

1) Mismatches in $P_1 - P_4$ result in nonlinearity, rather than simply the nonzero offset voltage correspondingly produced in a conventional operational amplifier. Close study also shows that only matching between P_1 and P_3, and P_2 and P_4 is required.

2) Small mismatches of N_1 and N_2 cause negligible nonlinearity.

3) A fixed amount of mismatch of tail-end biasing currents leads only to a nonzero offset voltage. However, if the output impedance of the tail-end biasing-current source is not large enough, the mismatch in tail-end biasing currents will be a function of the input common-mode voltage. This in turn leads to nonlinearity.

4) Mismatch of threshold voltages due to the body effect does not lead to undesirable results, provided that the intrinsic threshold voltages of the MOSFET's are equal. However, if the body-effect parameter is too large, a nonlinearity due to a degradation of the output impedance of P_5 and P_6 may result from excessively large gate-to-source voltages applied to $P_1 - P_4$.

These relationships have been used in the design and optimization of a practical TIAMP. In general, the combination of input transistor sizes and biasing current levels provides a suitable linear region of operation for the purpose of minimizing nonlinearity. The particular choice of the biasing current will be covered in more detail in the next section.

The only passive components used in the TIAMP in Fig. 4 are for the purpose of frequency compensation. Thus, they do not have to be highly linear or well-matched. The associated resistor may be implemented using a MOSFET biased in the triode region. The associated capacitor may employ the parasitic capacitance of a large MOSFET.

The TIAMP has been simulated using SPICE. For use in the D/A converter, the region of zero-gain error was selected to be around -2.5 V. The simulation results summarized in Table I clearly indicate that the TIAMP design has wide bandwidth and fast settling time. The relatively small open-loop gain is due mainly to the small transconductance of the input stage. How-

TABLE I
Simulated Performance of the Three-Input Amplifier

A_o	1048 V/V or 60.4 dB
ω_u	3.9 MHz
ϕ_m	62.5°
settling time	0.7 μs (20pF)
offset voltage	0.716 mV

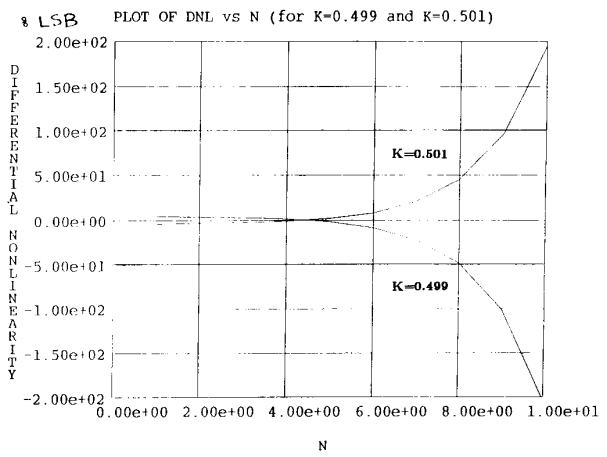

Fig. 5. Differential nonlinearities at major carries.

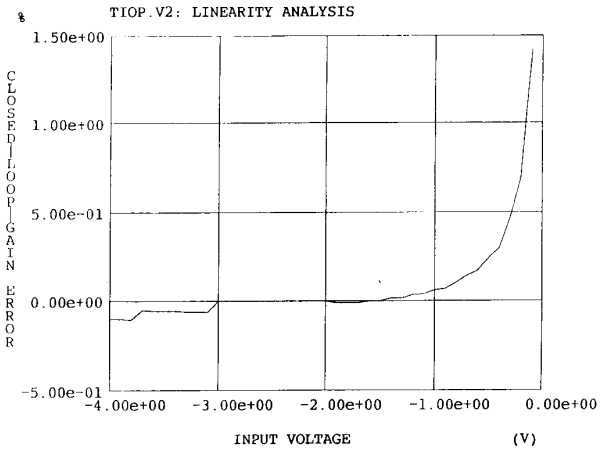

Fig. 6. Overall linearity of the TIAMP.

ever, its effect is partially cancelled by the lower sensitivity of the closed-loop gain to open-loop gain.[2]

IV. Differential Nonlinearity Considerations

The differential nonlinearity of the D/A converter at the first major carry ($011\cdots1$, $100\cdots0$) can be expressed as

$$\begin{aligned}\text{DNL} &= k^{1-N} - \{k^{2-N} + k^{3-N} + \cdots + k^{-1} + 2\} \\ &= k^{1-N} - \frac{k^{2-N}-1}{1-k} - 2 \end{aligned} \tag{5}$$

where k is the closed-loop gain of the TIAMP.

For a given value of k not equal to $1/2$, generally speaking, the magnitude of DNL increases with increasing values of N. This is illustrated by the curves shown in Fig. 5.

From these curves, we may deduce that the DNL is most sensitive to the gain error of the TIAMP at the first major carry. It follows that the TIAMP should be biased in such a way as to minimize the DNL at the first major carry. For both input codes $011\cdots1$ and $100\cdots0$, input voltages for all TIAMP's are either zero or very close to the reference voltage. Thus, to minimize the DNL at the first major carry, the TIAMP design should be optimized to have very small closed-loop-gain errors for large input voltages. This requires large biasing currents which lead to large closed-loop-gain errors for small input voltages. The closed-loop-gain errors for small input voltages affect conversion accuracy of other input codes (such as $00\cdots01$ and $100\cdots01$) which causes some of the TIAMP's to have small input voltages. However, fortunately, the DNL associated with these codes is relatively insensitive to the closed-loop-gain error. This is illustrated by considering, for example, the DNL at ($100\cdots0$, $100\cdots01$) which is given by

$$\text{DNL} = (2k)^{i} - 1 \tag{6}$$

where $i = N - j - 1$ and $j = \log_2(V_{\text{ref}}/V_{\text{critical}})$. The variable V_{critical} is the input voltage below which the closed-loop-gain errors of the TIAMP become significantly large.

Simulation of the circuit in Fig. 4 indicates that closed-loop-gain errors are below 2 percent for input voltages lower than -71 mV. Using a reference voltage of -2.5 V, with $N = 8$ and for a DNL less than 0.5 LSB, the maximum closed-loop-gain error allowed according to (6) is 22 percent. Thus, large closed-loop-gain errors present in the TIAMP for small input voltages are not a major concern.

While the use of large biasing currents for the input stage helps to improve the transconductance matching of the transistors [3], random variations of the transistor sizes due to finite lithographic resolution will produce a random component in the DNL. From SPICE simulation, the closed-loop-gain error of the TIAMP for input voltages between -2 and -3 V is negligible (see Fig. 6). It follows that, according to (5), for an 8-bit D/A converter with a differential nonlinearity of 0.5 LSB, a closed-loop-gain error of 0.2 percent due to process variation is allowed.

VI. Experimental Results

Five samples of an experimental 12-bit D/A converter have been fabricated at Northern Telecom using their 3-μm CMOS process through the service provided by the Canadian Microelectronics Corporation. These five D/A converters achieve resolutions of 10 bits (DNL = 0.30 LSB), 8 bits (DNL = 0.44 LSB), 7 bits (DNL = 0.37 LSB), 7 bits (DNL = 0.38 LSB), and 6 bits (DNL = 0.50 LSB), for peak-to-peak negative output-voltage swings no larger than 3 V. The total area occupied by a D/A converter is 1.96 mm^2, which can be reduced easily to 1.4 mm^2 by simply placing the amplifiers closer to one another.

Fig. 7 shows the first-major-carry transition of the output voltage of the 7-bit resolving D/A converter configured to have 8 bits. The glitch shown is due both to a skew in the digital-input signals and the different path lengths traversed by bit signals within the D/A converter. The digital crosstalk seen due to imperfect grounding on the printed-circuit test board was measured to be 4-mV peak to peak. From the waveform shown in Fig. 7, the D/A converter in the 8-bit configuration is found to have a DNL of slightly less than 1 LSB. Using a linear-ramp test, the maximum rate of conversion was measured to be approximately 1 MHz. This relatively high speed of operation is due mainly to the very small input capacitance of the TIAMP and the use of an output buffer. The static power dissipation of a 12-bit converter is approximately 50 mW.

[2]The minimum open-loop gain required for 8-bit accuracy is about 250 V/V [1].

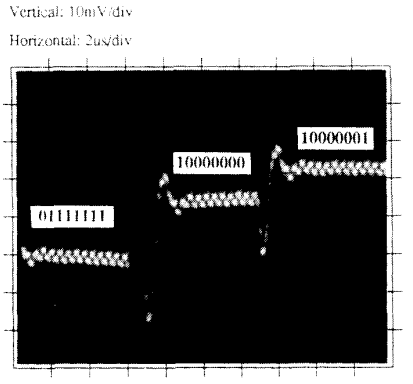

Fig. 7. Output waveform of an 8-bit DAC at the major-carry transition.

VII. Conclusion

This paper has demonstrated the feasibility of the use of active components to perform the sum of two voltages, and division by two, as required in some approaches to digital-to-analog conversion. The technique described here has been used to implement a 12-bit D/A converter for which five samples have been tested with accuracies ranging from 6 to 10 bits. Accuracy is limited in the present design by the relatively small sizes chosen for the input transistors. The maximum conversion rate of the present prototypes has been measured to be approximately 1 MHz with a static power dissipation of 50 mW.

References

[1] C. P. Chong, "A/D and D/A converters using no precise or well-matched passive components," M.A.Sc. thesis, Dept. Elec. Eng., Univ. of Toronto, Toronto, Ont., Canada, 1988.

[2] E. Säckinger and W. Guggenbühl, "A versatile building block: The CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 287–294, Apr. 1987.

[3] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 1057–1066, Dec. 1986.