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CMOS integrated circuits for multivalued logic

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The use of CMOS integrated circuits in the design of multivalued logic systems is extended. Circuit design of basic quaternary operators (inverters, NAND, NOR, cycling and inverse cycling gates) is presented. These basic quaternary operators can be used as building blocks in four-valued digital systems. The extension of these circuits to implement five-valued systems is also discussed.

1. Introduction

Although much work has been reported on the design and implementation of multivalued logic, very few authors have used complementary metal oxide semiconductor (CMOS) integrated circuits in their designs for systems with radix higher than three (Mouftah and Jordan 1977, Huertas and Carmona 1979, Huertas and Sanchez-Gomez 1981, Donoghue *et al.* 1983, Freitas and Current 1983). Moreover, in all previous designs, authors have used voltage power supplies higher than the threshold voltage of the p- and n-channel MOS transistors. Only recently, a new family of three-valued CMOS circuits has been reported (Mouftah and Smith 1982) which is not restricted to the use of power supplies at the above-threshold voltages. This design reduces power consumption and offers a new degree of freedom in the creation of multivalued logic circuits.

In this paper both approaches, the use of power supplies below threshold as well as supplies above threshold, are followed in order to design multivalued logic circuits with a radix higher than three. Circuits of a four-valued inverter, NAND, NOR, cycling and inverse cycling gates are described. The possibilities for five-valued circuits are also considered.

2. The inverter

A quaternary inverter circuit is shown in Fig. 1. The circuit is composed essentially of two sections, namely the above-threshold voltage (ATV) section and the below-threshold voltage (BTV) section. The ATV section is driven by a voltage power supply (± 3 V), at a level chosen to be higher than the threshold voltage of the p- and n-channel transistors, and is composed of four transistors (T_3–T_6). On the other hand the BTV section, which is composed of only two transistors (T_1 and T_2), is driven by a voltage power supply (± 1 V), at a level chosen to be lower than the threshold voltage of both the p- and the n-channel transistors. The output z can take any one of four voltage levels, two from the ATV section (± 3 V) and two from the BTV section (± 1 V).

Following one of many possible conventions, we shall label the four voltage levels -3 V, -1 V, $+1$ V and $+3$ V as logic 0, 1, 2 and 3, respectively. Thus the

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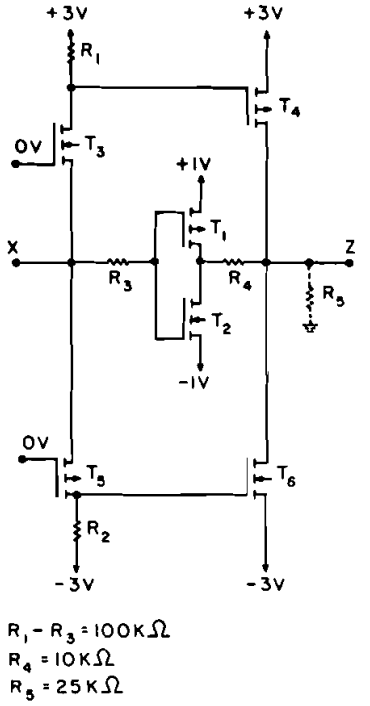

Figure 1. Four-valued (five-valued) inverter.

quaternary inverter is defined by

$$\bar{X} = P - X \tag{1}$$

where $P = n - 1$, and n is equal to 4 here.

The operation of this quaternary inverter is summarized in Table 1. As an example, when the input X is at logic level 3, transistor T_1 will be off while T_2 will be on. At the same time, transistor T_3 will be off, keeping the gate of transistor T_4 at $+3$ V which will force it to be off. On the other hand, transistor T_5 will be on, forcing the gate of transistor T_6 to be at $+3$ V and causing it to turn on. The existence of the resistance R_4 in this situation will cause the output Z to be at logic level 0, which is the inverse of the input signal X. Resistances R_1 and R_2 are used here for proper transistor biasing, while R_3 is used to reduce the input voltage to within the operating range of the BTV section when the input X is at logic level 0 or 3. It has to be noted that R_3 is used here only for prototyping with the MC14007 CMOS integrated circuits, and is not required in custom integrated circuit design.

A five-valued inverter can also be implemented using the circuit of Fig. 1 with the addition of a shunt resistor of suitable value (e.g. 25 kΩ) connecting the output Z

X	T_1	T_2	T_3	T_4	T_5	T_6	Z
3	off	on	off	off	on	on	0
2	off	on	off	off	off	off	1
1	on	off	off	off	off	off	2
0	on	off	on	on	off	off	3

Table 1. Truth table for the four-valued inverter.

to the ground. The fifth state is obtained by the ground voltage level (0 V). In this state all transistors will be off and the output Z will be established at the ground voltage level (0 V) through R_5 which is connected to ground. The levels of the voltage power supplies of the BTV section will have to be slightly modified (to $\pm 1{\cdot}5$ V) in order to produce equally spaced symmetrical voltage levels. In the latter case the substrate of the p-channel and n-channel transistors of the BTV section have to be connected to $+3$ V and -3 V, respectively, in order to keep the threshold voltages of both transistors of this section higher than the voltage power supplies ($\pm 1{\cdot}5$ V). Equation (1) will also hold here with $n = 5$.

3. NOR and NAND gates

By applying the same methods introduced above, quaternary NOR and NAND gates have been realized as shown in Figs. 2 and 3, respectively. As in the quaternary inverter, both circuits are composed of an ATV section and a BTV section. The number of transistors used in each circuit is equal to the number of transistors used in the quaternary inverter multiplied by the number of inputs to the gate. Since the number of inputs in Figs. 2 and 3 is two (X and Y), the number of transistors used in this case is double that of the quaternary inverter, i.e. twelve.

In both circuits the BTV and ATV sections are composed of transistors T_1–T_4 and transistors T_5–T_{12}, respectively. In the quaternary NOR circuit (Fig. 2) T_1 and

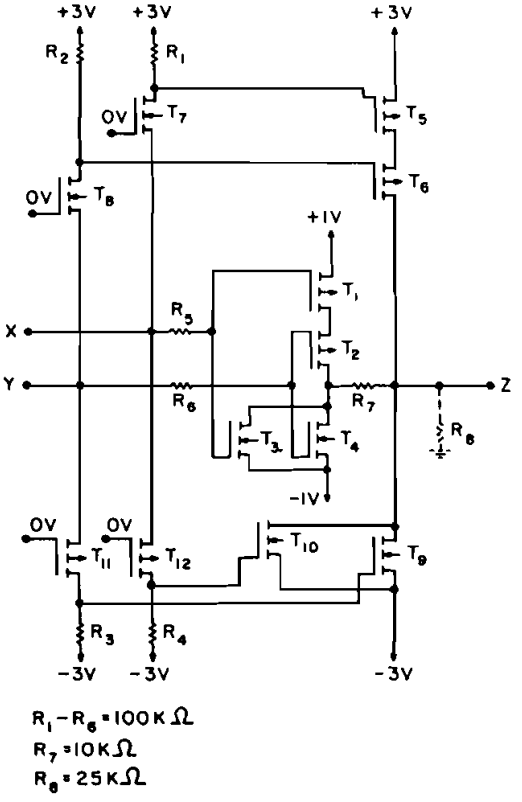

Figure 2. Four-valued (five-valued) NOR gate.

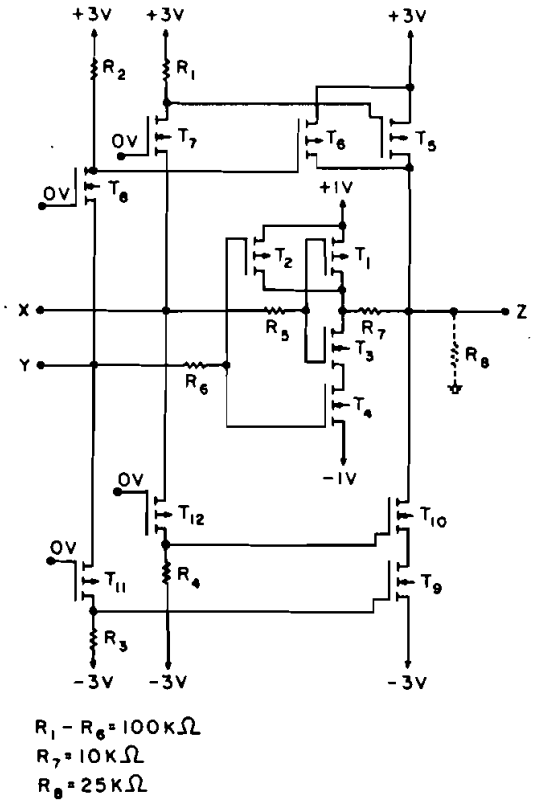

Figure 3. Four-valued (five-valued) NAND gate.

T_2, in the BTV section, are connected in series while T_3 and T_4 are connected in parallel. In the quaternary NAND, these connections are exactly the opposite. This also applies to the ATV section which has, in the case of the NOR gate, T_5 and T_6 connected in series while T_9 and T_{10} are connected in parallel. However, the biasing transistors of the ATV section (T_7, T_8, T_{11} and T_{12}) are connected exactly the same way for both the NOR and NAND circuits. The quaternary NOR and NAND functions are defined, respectively, by

$$\overline{(X \vee Y)} = \overline{\max(X, Y)} \tag{2}$$

$$\overline{(X \wedge Y)} = \overline{\min(X, Y)} \tag{3}$$

As an example of circuit operation, consider the quaternary NAND circuit of Fig. 3. If the two inputs X and Y are at logic 0 and 2, respectively, T_1 and T_4 will be on while T_2 and T_3 will be off; thus the output of the BTV section will tend to go to logic 2. However, in the ATV section, T_5 will be on and T_6, T_9 and T_{10} will be off, because T_7 will be on while T_8, T_{11} and T_{12} will be off. Thus the output of the ATV section will tend to go to logic 3 and, because of R_7, will force the output Z to take the logic level 3. Therefore, Z is the inverse of the minimum value of X and Y.

An improved version of the NOR gate can be obtained by replacing T_9 and T_{10} (Fig. 2) by a single transistor T'_9 which has its gate connected to the drains of both

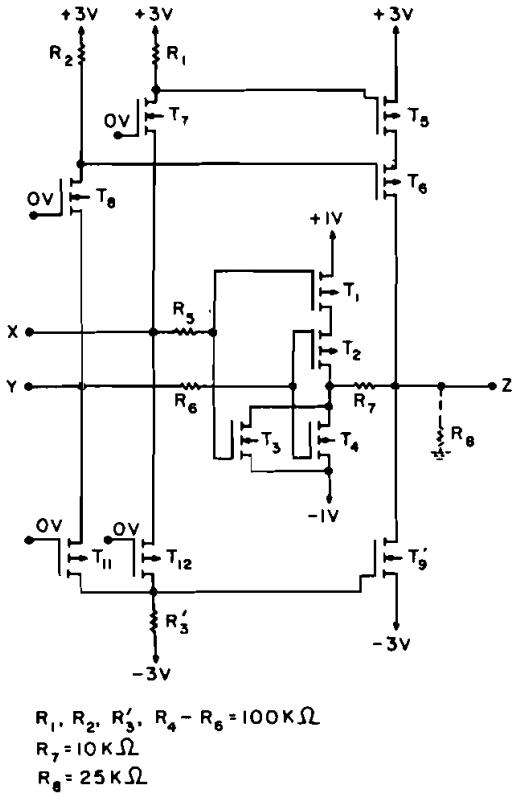

Figure 4. Improved four-valued (five-valued) NOR gate.

T_{11} and T_{12} and a pull-down resistor R'_3 as shown in Fig. 4. The operation of this circuit is exactly the same as that of Fig. 2 even though the number of components has been reduced. Similarly, an improved version of the NAND gate can be obtained by replacing T_5 and T_6 (Fig. 3) by a single transistor, and R_1 and R_2 by a single resistor with the drains of T_7 and T_8 connected together. Since it is straightforward extension, the improved version of the NAND gate circuit has not been included here.

Corresponding to the five-valued inverter, five-valued NOR and five-valued NAND gates can be realized using the circuits of Figs. 2 and 3, respectively, with the addition of a shunt resistor of suitable value (e.g. 25 kΩ) connecting the output Z to ground. Again, the fifth state is obtained by the ground voltage level (0 V). In this state all transistors (T_1–T_{12}) will be off and the output Z will get the ground voltage level (0 V) from the added resistor which is connected to the ground. To have equally spaced symmetrical voltage levels, the voltage power supplies of the BTV section will be $\pm 1{\cdot}5$ V and the substrates of the p- and n-channel transistors will be connected to $+3$ V and -3 V, respectively. Equations (2) and (3) will hold also in this case and the circuit operation will be exactly the same as described above with the added fifth state.

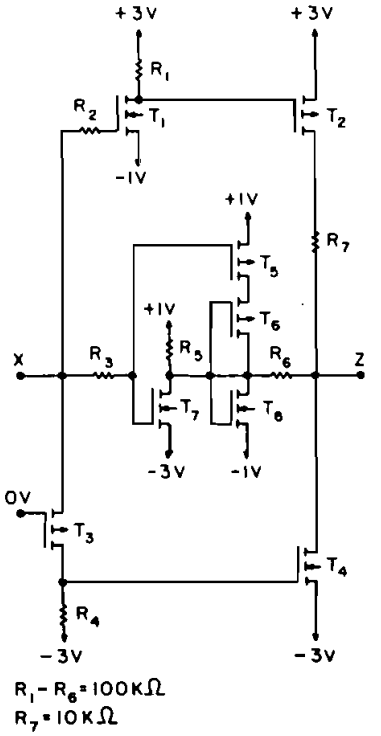

Figure 5. Four-valued cycling gate.

4. Cycling gates

The cycling and inverse cycling gates are defined, respectively, by

$$X' = (X + 1) \bmod n \tag{4}$$

$$X'' = (X - 1) \bmod n \tag{5}$$

where n is the radix number, and the positive and negative signs represent arithmetic addition and subtraction, respectively.

The circuits of the quaternary cycling and inverse cycling gates are shown in Figs. 5 and 6, respectively. The design of these circuits is a little bit different from that of the inverter described above. Although these circuits can still be considered to be composed of an ATV and a BTV section, the input stage of both sections contains an element with a voltage power supply opposite to the one of that section (T_1 for the ATV section and T_7 for the BTV section). The circuit of Fig. 6 is the dual of that of Fig. 5 and can be obtained by replacing every transistor by its dual (i.e. p- by n-channel transistor and vice versa) and every voltage power supply by its opposite value in polarity. In both circuits of Figs. 5 and 6, an additional resistor may be used to connect the drain of the T_7 to the gates of both T_6 and T_8 in order to limit the backward current. Only the operation of the cycling gate will be described here.

Table 2 summarizes the operation of the circuit of Fig. 5. As an example of the circuit operation, consider that the input X is at logic level 2. In this case, the output of the BTV section will be in a high impedance state since T_5 and T_6 are off and T_7

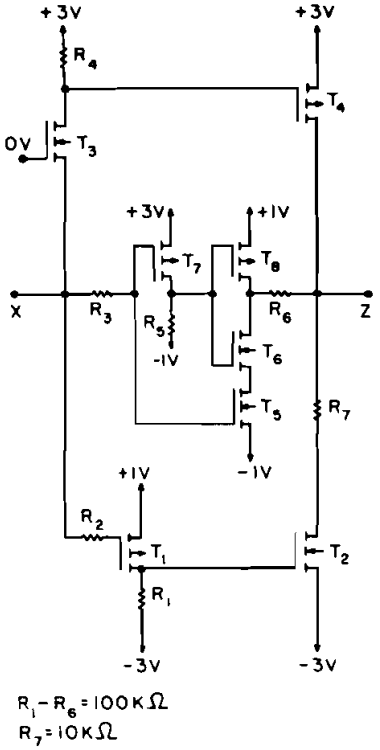

Figure 6. Four-valued inverse cycling gate.

is on forcing transistor T_8 to be also off. At the same time, in the ATV section, T_1 and T_2 will be on while T_3 and T_4 will be off; thus the output Z will be at logic level 3.

Finally, it should be noted that for all four-valued circuits, all p-channel substrates are connected to +3 V for the ATV section and +1 V for the BTV section, while all n-channel substrates are connected to −3 V for the ATV section and −1 V for the BTV section, with the exception mentioned above for the cycling gates where the substrates of T_1 and T_2 are connected to their source. In the case of five-valued circuits, all p-channel substrates are connected to +3 V, while all n-channel substrates are connected to −3 V. All circuits presented have been realized with the MC14007 CMOS integrated circuit.

X	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	Y
3	on	on	on	on	off	off	on	off	0
2	on	on	off	off	off	off	on	off	3
1	off	off	off	off	on	on	on	off	2
0	off	off	off	off	on	off	off	on	1

Table 2. Truth table for the four-valued cycling gate.

5. Conclusions

The use of CMOS integrated circuits in the design of some four-valued and five-valued basic operators has been presented. These multivalued basic operators are strong candidates for use as building blocks in multivalued digital systems.

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