Simple digitally-controlled variable-gain linear d.c. amplifier

A. Sedra, Doctoral Candidate and
K. C. Smith, Associate Professor,
University of Toronto

IN DESIGNING programmable waveform generators the problem arises of digitally controlling the signal amplitude. The amplifier described here represents a simple and accurate solution for this problem. Apart from that special need, it has a large number of applications, some of which are outlined or referenced here.

First, the required transfer-function of the device is stated and the scheme used for implementing this function is presented. A discussion of design considerations follows, together with the circuit diagram of the apparatus built. Experimental results are then stated and interpreted. Finally some applications of the device are discussed.

1 Gain control function

The required transfer-function for the system as defined in Fig. 1 is

$$V_o = KPV_s \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

i.e. the amplifier gain $G = V_o/V_s$ is given by

$$G = KP \quad \ldots\ldots\ldots\ldots\ldots\ldots (1a)$$

where

V_s is the bipolar input signal; V_o is the bipolar output signal; both V_s and V_o are limited by the amplifier used to the range ± 10V, K is a constant representing the size of the step variation in gain and P is the decimal equivalent of the binary control signal. For an n-bit binary signal, P is given by

$$P = 2^0a_0 + 2^1a_1 + 2^2a_2 + \ldots\ldots\ldots\ldots + 2^{n-1}a_{n-1} \quad (2)$$

where each a assumes the value 0 or 1 according to its corresponding bit.

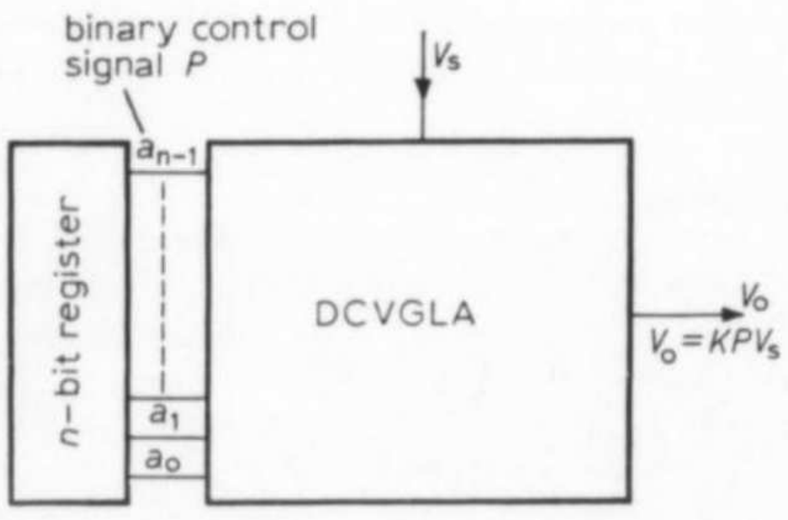

Fig. 1 Transfer-function of digitally-controlled variable-gain linear amplifier (DCVGLA), $V_o = KPV_s$

2 Implementation

Fig. 2 shows the scheme used for implementing the control function of equation (1). Half the input signal V_s is fed to the non-inverting terminal of the operational amplifier by the potential divider $R_1 - R_2$. The inverting terminal is connected to the signal source V_s by a resistance R_{f1} equal to the feedback resistance, R_{f2}, and to ground by a series of 8 binary weighted resistors, 2^1R, through switches controlled by the 8 bit binary signal.

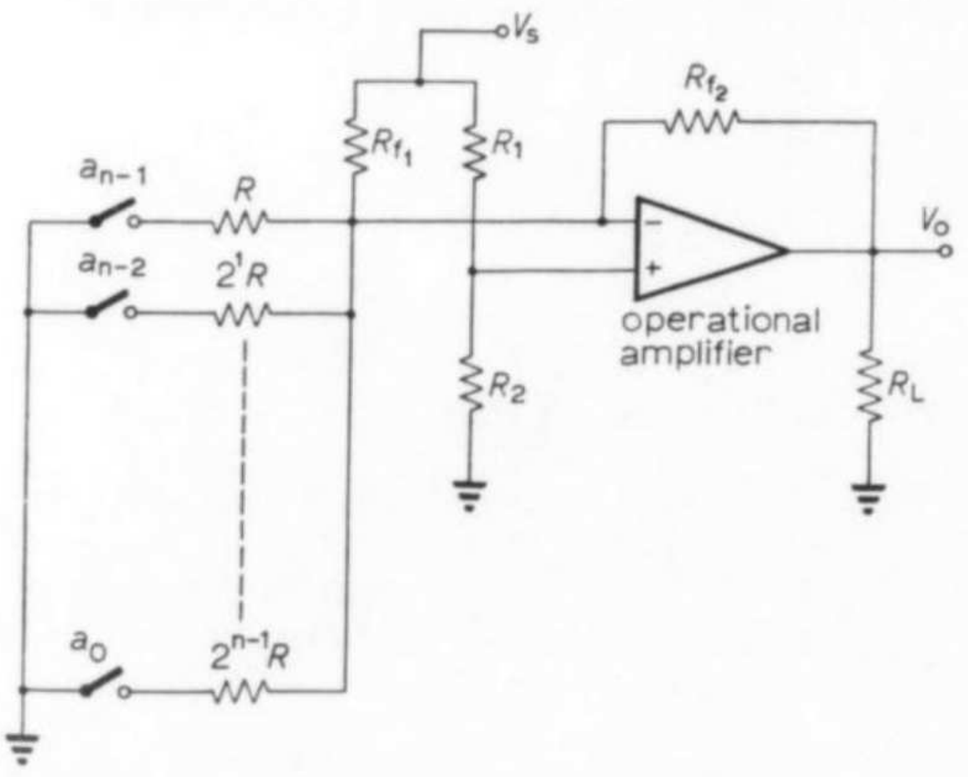

Fig. 2 Scheme for implementing transfer-function in Fig. 1

This article describes a d.c. amplifier whose gain can be varied between 0 and 25·5 in steps of 0·1 (256 steps). The gain setting is determined by an 8-bit binary number. The output is accurate within $\pm 1\%$ of its nominal value for bipolar input signals within the range of $\pm 0{\cdot}1$ to ± 10V. The bandwidth is limited by the operational amplifier used which can be chosen, within reason, to satisfy any required frequency characteristic.

Cet article décrit un amplificateur à courant continu dont le gain peut être modifié entre 0 et 25,5 par plots de 0,1 (256°). Le réglage du gain est déterminé par un nombre binaire à 8 chiffres. Le degré de précision de la sortie est de $\pm 0{,}1$ à ± 10 volts. La largeur de bande est limitée par l'amplificateur opérationnel utilisé, ce dernier pouvant être choisi, dans des limites raisonnables, pour répondre à n'importe quelle caractéristique de fréquence voulue.

Der Bericht behandelt einen Gleichspannungsverstärker, dessen Verstärkungsfaktor sich in 256 Stufen von 0,1 zwischen 0 und 25,5 einstellen läßt. Der Verstärkungsfaktor wird durch eine Binärzahl von 8 bit bestimmt. Die Ausgangsspannung ist im Bereich $\pm 0{,}1 - \pm 10$ Volt genau. Die Bandbreite des Verstärkers ist nur durch den Operationsverstärker begrenet, der jedoch im Hinblick auf den gewünschten Frequenzbereich gewählt werden kann.

Assuming an ideal differential amplifier with infinite gain and infinite input impedance it can be easily shown that for n bits

$$V_o = \frac{R_f}{2^n R} PV_s \quad \text{..... (3)}$$

which is the required function stated in equation (1) with the gain step K given by

$$K = \frac{R_f}{2^n R} \quad \text{..... (4)}$$

and $$R_f = R_{f1} = R_{f2}$$

3 Design considerations

(a) Operational amplifier

The operational amplifier used should have very low offset current and voltage as it has been assumed, in the derivation of the control function above, that the inverting terminal potential will track that of the noninverting one at all signal levels.

Another very important criterion for choosing a suitable operational amplifier is a very low capacitance between both input terminals and ground, otherwise large errors would be expected for a.c. input signals. It should be noted that the circuit bandwidth is a function of the operational amplifier used; thus the latter should be chosen to satisfy the frequency characteristics desired.

For the present application the Philbrick P85AU operational amplifier has been used. This has a small-signal unity gain bandwidth of 2 MHz and a large-signal full-output maximum frequency of 10 kHz (see experimental results for corresponding performance).

(b) Resistor values

In choosing the resistor values used one should keep in mind that the highest value of the binary weighted series (corresponding to the least significant bit) should be low enough to ensure current value much larger than the sum of the reverse currents of all the off switches. For 8 bits control signal, let $R = 500\Omega$. This makes the highest resistance 64 kΩ. Thus, if the lowest expected signal magnitude is 100 mV, the lowest current step is $50/64 \simeq 0{\cdot}8\ \mu$A, which is much larger than the reverse current of the silicon transistors to be used. The reverse current is typically of the order of few nanoamperes at low signal levels.

If the desired gain step $K = 0{\cdot}1$, then using equation (4), $R_{f2} = 12{\cdot}8$ kΩ.

It is obvious that to obtain high accuracy, highly precise resistors should be used.

(c) Switches

The design of an accurate switching system for this equipment is of prime importance. The main requirements imposed upon the switches are the following:

(i) should be bipolar, as the amplifier handles bipolar signals;

(ii) should have very low closure voltage. In fact this voltage enters directly in determining the amplifier accuracy. Large errors would arise at low signal levels if the closure voltage was not very small;

(iii) the off current of the switches should be very low (a few nanoamperes maximum).

In spite of these strict requirements a very simple switching system is possible. Only one bipolar transistor connected in the inverted manner and operated in saturation proves to be quite satisfactory. This fact is demonstrated by Fig. 3 which shows plots of the saturation voltage versus the switched current for two values of base current drive. Two curves are drawn for each drive representing the extremes among a group of eight transistors of the same type used. The current ranges used are those encountered in the present application. It is clear that in the low current regions, where the maximum errors are expected, saturation voltages of only a fraction of a millivolt are found for both current polarities.

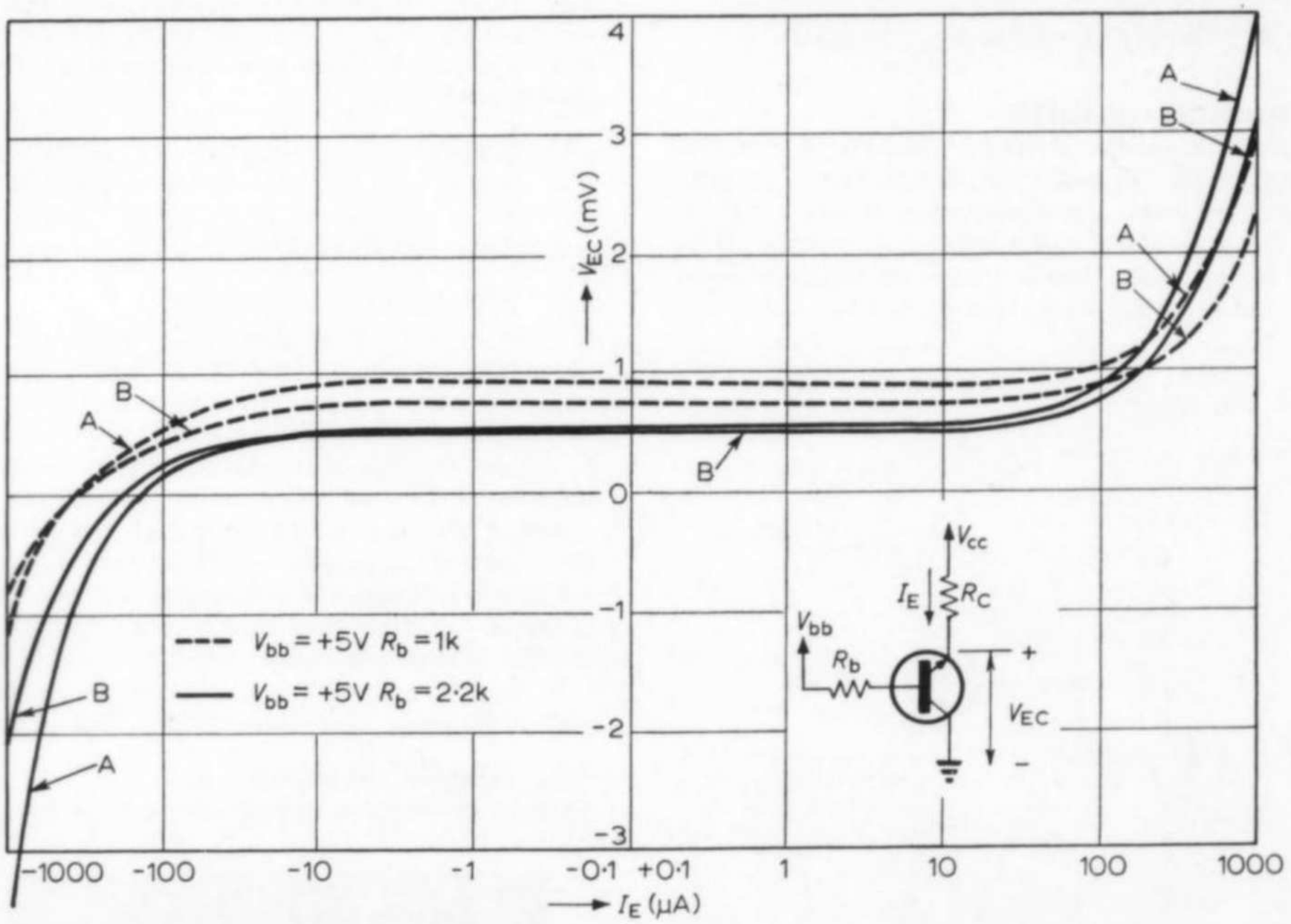

Fig. 3 Saturation characteristics of inverted transistor showing two extreme devices A and B among tested group of 8 transistors type 2N3642, for two values of base current drive

Concerning the choice of logic levels, the low value (corresponding to cut-off) should be more negative than half the maximum negative signal magnitude to ensure cut-off, (that is < -5 V). A diode is added in series with the base lead (Fig. 4) to protect the emitter-base junction against high reverse-bias voltages. The upper logic level should be chosen together with the base resistance to provide the required amount of base drive established by reference to Fig. 3.

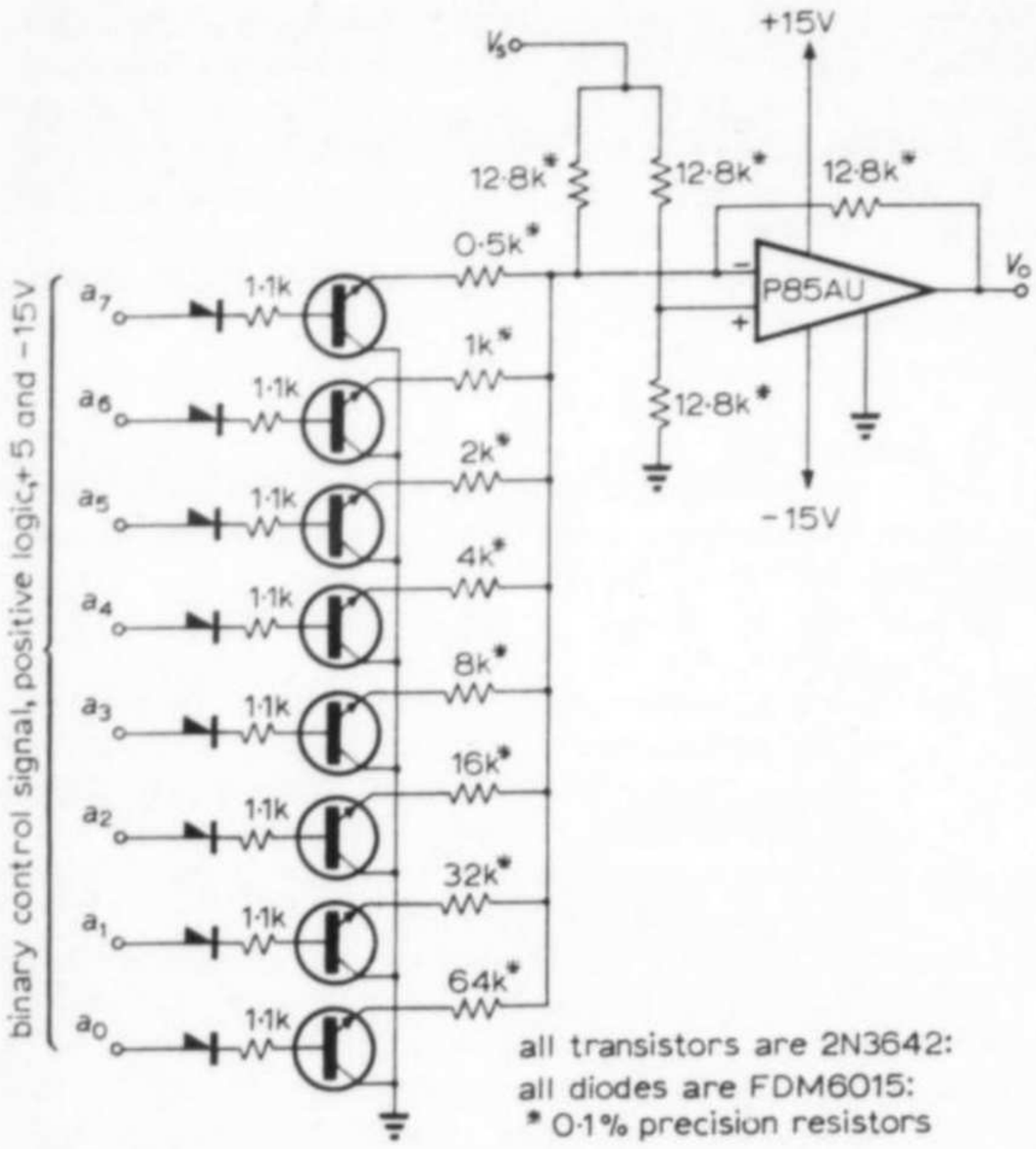

Fig. 4 Complete circuit diagram of DCVGLA

4 Experimental results

Following the design method described, the circuit shown in Fig. 4 has been built. In order to provide operation with Fairchild micrologic levels, the driving stage shown in Fig. 5 is used to shift the logic levels to 0·3 and 0·7 V, as required by this family of logic circuits. The amplifier was tested with d.c. input signals and the percentage error in output is calculated from

$$\text{percentage error in output} = \frac{\text{measured output} - KPV_s}{KPV_s} \times 100$$

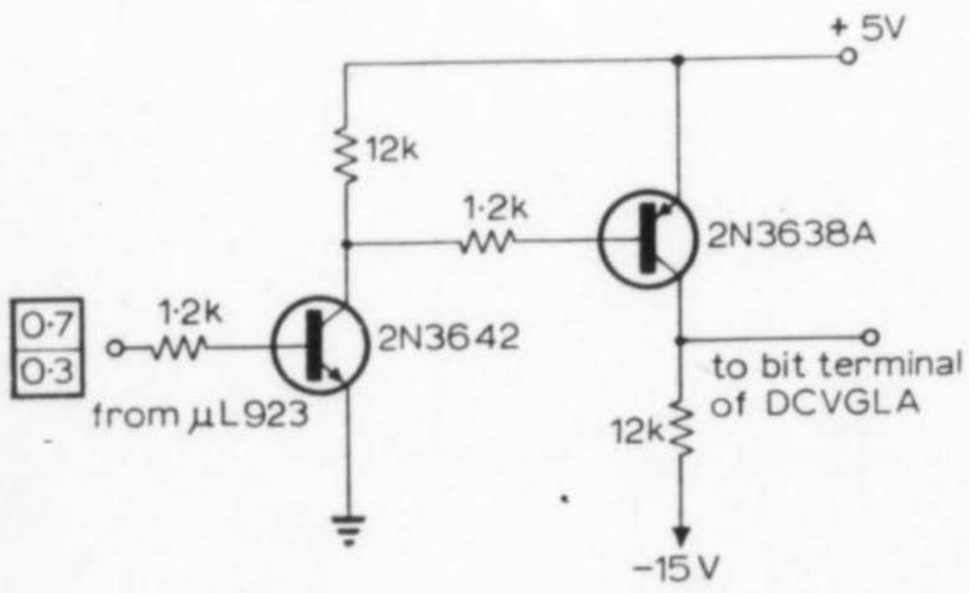

Fig. 5 Driving stage used to shift logic levels of DCVGLA to that of Fairchild micrologic

This error is plotted in Fig. 6 versus the control signal P for various values of input signal levels (of both polarities). It follows from this plot that the error is less than the specified value of 1% for signal magnitudes > 100 mV. Due to switch and amplifier offsets the percentage error increases greatly for very small signals. It is about 10% for signals of 10 mV, for example. When testing the amplifier with a.c. input signals, the full undistorted output was obtained at a maximum frequency of 12 kHz. This agrees with the specifications of the operational amplifier used.

Some of the results obtained for tests with a.c. input signals will be presented in the next section in connexion with particular applications.

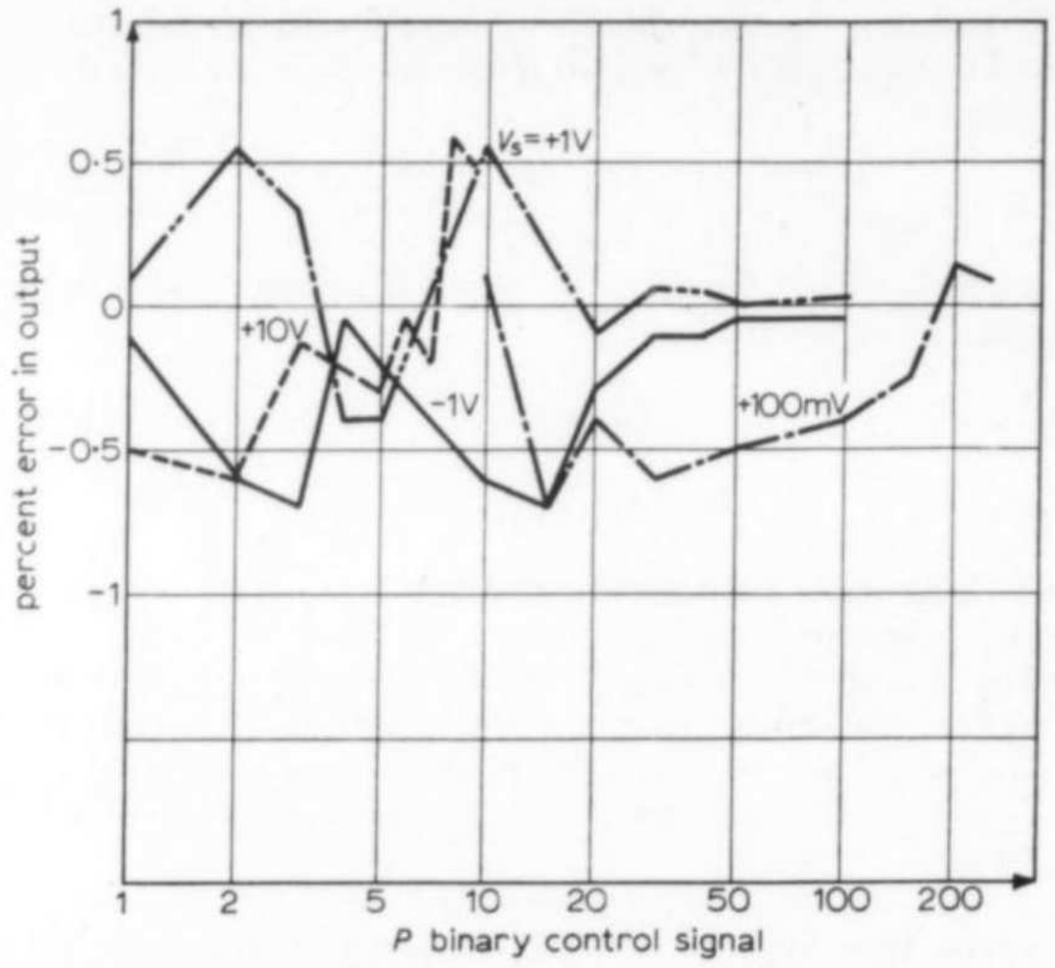

Fig. 6 Percentage deviation of output from nominal value for various values of input signal

5 Applications

Apart from the major requirement for which this device is constructed, namely for use in programmable waveform generators, it has many applications, of which the following are examples:

(1) Digital-to-analogue conversion

The variable gain amplifier can be considered as an accurate multiplying d-a converter or a d-a converter[1] having a reference of variable magnitude and polarity.

(2) Waveform generation

It can be used for generating some particular waveforms such as staircase, ramp or triangular with controllable amplitude and frequency. To generate a staircase, a d.c. voltage is fed to the signal input terminal and a recycling counter of any particular number of bits (according to the number of steps required in the staircase) is used to provide the binary control signal. If the number of steps is high enough (256 for 8 bits), the staircase approaches a ramp (see Fig. 7). The ramp amplitude is changed by varying the d.c. input signal while the frequency is determined by the counter input. If a reversible counter is used a triangular waveform will be obtained.

It should be noted that the linearity of these waveforms is within the accuracy of the amplifier, that is, within 1%.

(3) Amplitude sweeping

In some applications such as testing the linearity of a network,

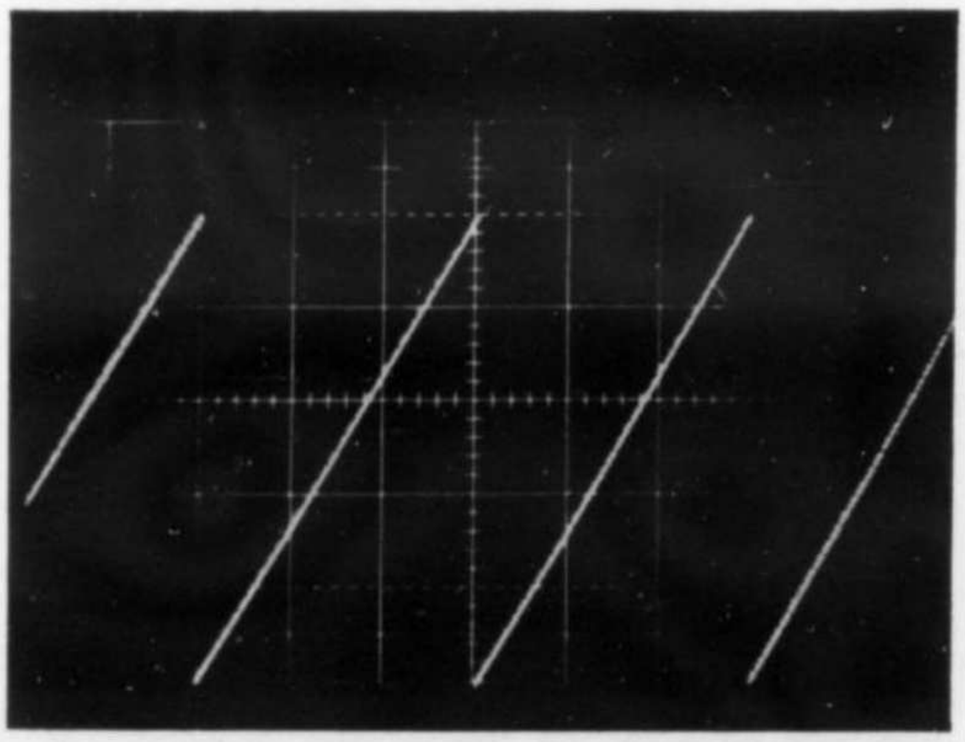

Fig. 7 Ramp generated by DCVGLA, vertical scale 2 V/division, horizontal scale 2 ms/division

one requires a signal (sinewave or a pulse-train for example) of linearly rising amplitude. This could be easily generated by feeding the signal whose amplitude is to be swept to the signal input terminal and at the same time using it to trigger the recycling counter feeding the binary control signal. Fig. 8 shows the waveform obtained using a 3-bit counter and a sinewave input signal.

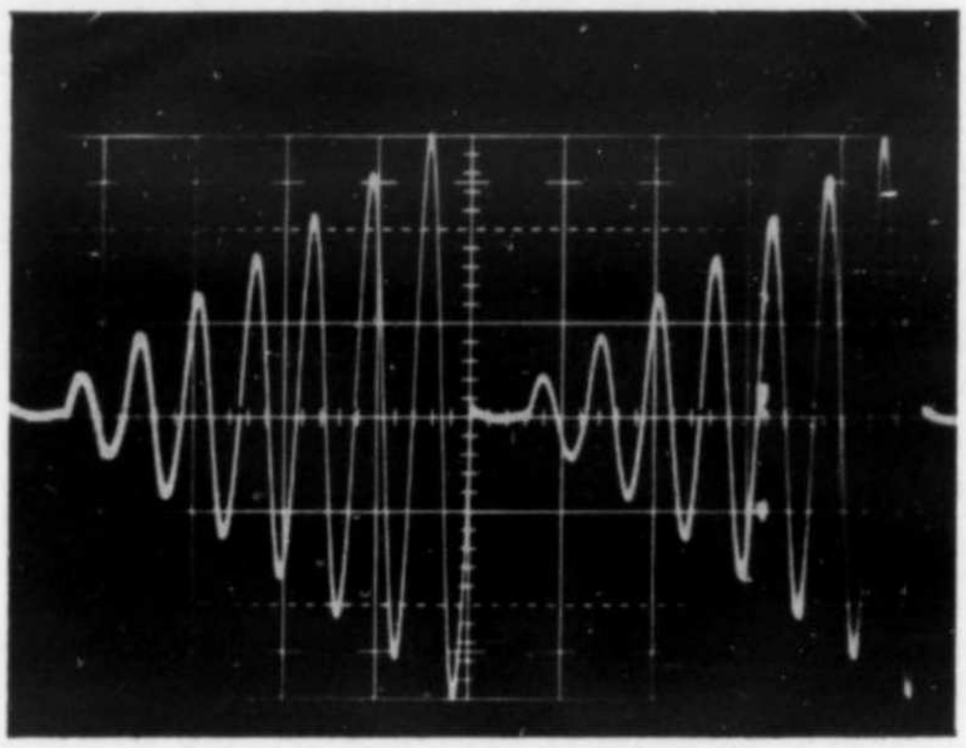

Fig. 8 DCVGLA used with 3-bit counter to sweep linearly amplitude of sinewave, vertical scale 2 V/division, horizontal scale 1 ms/division

(4) Conic display generator

By utilizing the inherent property of this apparatus, namely multiplication of analogue input signals by time (when a recycling counter drives the control input), one can generate a parabola represented by its time parametric equation. Other conic sections could be then generated by transformation of the basic parabola. The result is a 'conic display generator' which has been described in a recent article.[1]

(5) Other applications

Other applications include digital filter control (e.g. for speech synthesis),[2] parametric switching and optimization[3] and various hybrid analogue-digital computing schemes.[3, 4]

Conclusion

A simple digitally-controlled variable-gain linear amplifier is described and some of its applications are outlined. A discussion of the design considerations is given. Although this amplifier is able to handle bipolar signals with high accuracy a very simple switching system has been used.

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Time-constant variable over a large range

J. Clarke, B.Sc., Ph.D.

Ministry of Technology, Royal Radar

Establishment, Malvern (formerly at University of Birmingham)

The two-element resistor-capacitor network is somewhat unsuitable for providing a time-constant that may be varied over a large range. Another simple *RC* network is described and is presented as a better alternative.

Le réseau à résistance-capacité à deux éléments est plutôt inapproprié pour fournir une constante de temps qui peut être variée sur une gamme étendue. Le réseau résistance-capacité simple présenté par l'auteur constitue, à son avis, une meilleure variante.

Ein aus einem Widerstand und einem Kondensator bestehendes Netzwerk ist als Verzögerungsglied, dessen Zeitkonstante über einen großen Bereich verändert werden kann, etwas ungeeignet. Als eine bessere Lösung hierfür behandelt der Bericht eine andere einfache RC-Schaltung.

ONE OF THE simplest networks used to provide a time-constant in electrical networks is the series combination of a single resistor and a single capacitor. A typical example of the use of this network is the cross-coupling used in a multivibrator. In practice, if the time-constant is to be varied it is seldom convenient to use variable capacitors and often the range of resistance permissible is limited by other factors (the resistor may be providing a bias current, as in the case of a multivibrator). As an alternative, a slightly more complicated network is presented here whose time-constant can be varied over a very large range by means of the variable resistor that it contains.

1 Proposed network

The proposed network is shown in Fig. 1. The variable resistor R is shunted across the smaller capacitor C and the larger capacitor C_o connects these two elements to the output resistor R_o. The ratio of the capacitances determines the ratio of time-constants obtainable from the network. For the purpose of this paper, $C_o \gg C$, so that a large range of time-constants is obtainable.

A simple explanation for the operation of the network is as follows. If R is small the network reduces to a simple time-constant network of capacitor C_o and resistor R_o with time-constant C_oR_o. If R is large then the network reduces to a