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INVITED PAPER *Special Issue on Multiple-Valued Integrated Circuits*

Prospects for Multiple-Valued Integrated Circuits

Kenneth Carless SMITH† *and* **P. Glenn GULAK**††, *Nonmembers*

SUMMARY The evolution of Multiple-Valued Logic (MVL) circuits has been inexorably tied to the rapid technological changes induced by evolving needs and emerging developments in computing methodologies. Unfortunately for MVL, the numbers of designers of technologies and circuits whose lives are dedicated to the improvement of binary techniques, are large and overwhelming. Correspondingly, technological developments in MVL typically await the appearance of a problem or technique in the larger binary world to motivate and/or make possible some new advance. Such opportunities are inevitably quite transient since each such problem is simultaneously attacked by many others of a more conventional bent, and, as well, each technological change begets yet another, quickly. It is in the sensing of this reality that the present paper is written. Correspondingly, its thrust is two-fold: One target is the possibility of encouraging a leap ahead through modest technological projection. The other is the possibility of identifying application areas that already exist in this unbalanced competition, but which are specially suited to multiple-valued solutions. For example, it has been clear for decades that one such area is that of arithmetic. Correspondingly, we in MVL must strive quickly to concentrate our efforts on applications that exploit such demonstrable strengths. Some such applications are included here; others are visible historically, many probably remain to be found: Search on !

key words: *multiple-valued logic (MVL), current-mode circuits, BiCMOS, multiple-valued signal processing, multiple-valued field-programmable arrays (FPGAs), digital filtering, band-limited communications*

1. Introduction

As Minoru Nagata[24] and others have noted, the essential feature of integrated-circuit (IC) technology is its potential for reduction in interconnection cost through simplified processes for mass assembly. Correspondingly, it is toward capturing the possible dimensions of the interconnection issue that this paper on the prospects for multiple-valued (MV) circuit techniques proceeds.

Of necessity, the context of what follows must be the status quo, that situation now established by the rapid evolution of binary-oriented technologies and circuits. Thus this paper must concern itself with a broad range of issues oriented toward, and evolved in, a binary context. These range from a concern for the current trend toward customization in systems design, to reduced device-feature size, to reduced power-supply voltage, as well as for the perceived needs for, and possibilities of, hybrid technologies (exemplified by BiCMOS) at the component end of the scale.

While this emphasis on binary in an exposition on multiple-valued techniques may seem anomalous, it is also essential ! For at present, we cohabit a binary reality; whether it pleases everyone or not, it is binary technology which sets the standard against which any other technique will be (and perhaps must be) measured. Beyond reminding the reader that binary, being simply a degenerate case of the richer multiple-valued situation, is inevitably less intriguing, what can I say ? It is to motivate a more explicit appreciation of both the possibility and utility of MV integrated circuits that this paper is written.

2. Changing Times

Early in the history of the integrated circuit, observers of technological trends were captivated by Moore's Law concerning the exponential growth of IC complexity. That the idea has held so long and been so broadly productive has been quite remarkable ! Thus on a derived basis, one can now project that by the year 2000 (or so) one will see 2 Gb DRAM chips, and single-chip mainframe computers embodying 10^9 to 10^{10} transistors all fabricated in 0.1 μm silicon technology.[22],[24],[28] Reassuringly, there is a lot of detailed data concerning work in progress to support these possibilities in other ways as well.

Yet, while such predictive schemes have proven remarkably robust in the face of relatively dramatic technological developments, the reasons that they do so are possibly somewhat special. There certainly is concern now (as of course there has been before, but incorrectly, then) that particular physical limits are being reached. One might argue that a growing interest in nanoelectronics[40] is a productive response to that possibility, whose implicit aim is to leapfrog it. Alternatively, one might ask another question related to perceived continuity, concerning, for example, to

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† The author is with the Departments of Electrical and Computer Engineering, Computer Science, Mechanical Engineering, University of Toronto, M5S1 A4, Toronto, Ontario, Canada.

†† The author is with the Departments of Electrical and Computer Engineering, Computer Science, University of Toronto, M5S1 A4, Toronto, Ontario, Canada.

what degree the two-decade-long emphasis on microprocessors and random-access memory is responsible.[10] That such may indeed be the case, that we revel in a self-fulfilling prophecy, is at least of passing concern !

Although a case against the continuing dominance of microprocessors and memory in general is unarguable, it may be that the leading-edge super-fast super-big will ultimately diminish in relative importance. Certainly, in 1991, Minoru Nagata of Hitachi[24] can be seen to support that possibility in presenting his view that "what a customer actually wants is not complex state-of the-art chips but rather some particular function that he needs. They want ··· (useful systems). But they do not care whether 64 Mb DRAMs or 100 MIPS RISC processors are in them". He goes on to say that "the real goal of (integrated-circuit) engineers in the future will be mixed analog/digital integration, rather than scale integration".

Also in 1991, William Carter of Xilinx[7] presented an arguably related idea when he stated that "within 5 years ··· most digital logic will be designed using only three types of standard parts; microprocessors, memories and programmable logic".

While in these observations, both Nagata and Carter express an element of concern for static adherence to the view of simple continuity, there is certainly room for other evidence: Such evidence was presented by Tsugio Makimoto of Hitachi Semiconductor in an idea labelled "Makimoto's Wave" by David Manners, in Electronics Weekly.[21]

As indicated in Fig. 1, Makimoto suggested the existence of a 10-year half-cycle in the nature of semiconductor products, incorporating an exchanging emphasis between the customized and the standardized, beginning with the development of the transistor in 1947 at the start of the first half cycle of customization. Following the successive half-waves of standardized products, first of EIA-registered discrete devices, then of memories and microprocessors, he sees, around 1987, the emerging emphasis on customization through mask-programmable ASICs, leading, as the decade wanes, to emphasis on standardization through field programmability.

Certainly there can be no doubt about the ascendancy of Field-Programmable Gate Arrays (FPGAs) as exemplified by the large number of startup companies in the last year, each (Makimoto would agree) attempting to become the originator of the defacto standard product. Certainly, the emerging importance of FPGA technology was evident to Carter who made the statement attributed to him above in 1991.[7]

3. The Utility of Complex Logic Blocks

A recent set of experimental studies of the impact of logic-block architectures[43] on the performance of binary FPGAs provides some useful insights for multiple-valued extensions. The study is predicated on the inherent existence of nonoptimizable additional delay in field-programmable linkages. The dominant general conclusion presented there is that big blocks (such as a multi-input universal logic element) are most effective and, conversely, that fine-grain blocks (such as a two-input NAND) are less effective, by a factor of 3 or so in the study cited. Interestingly, it is not simply that speed-performance improves with the multiplicity of block inputs, but rather that block

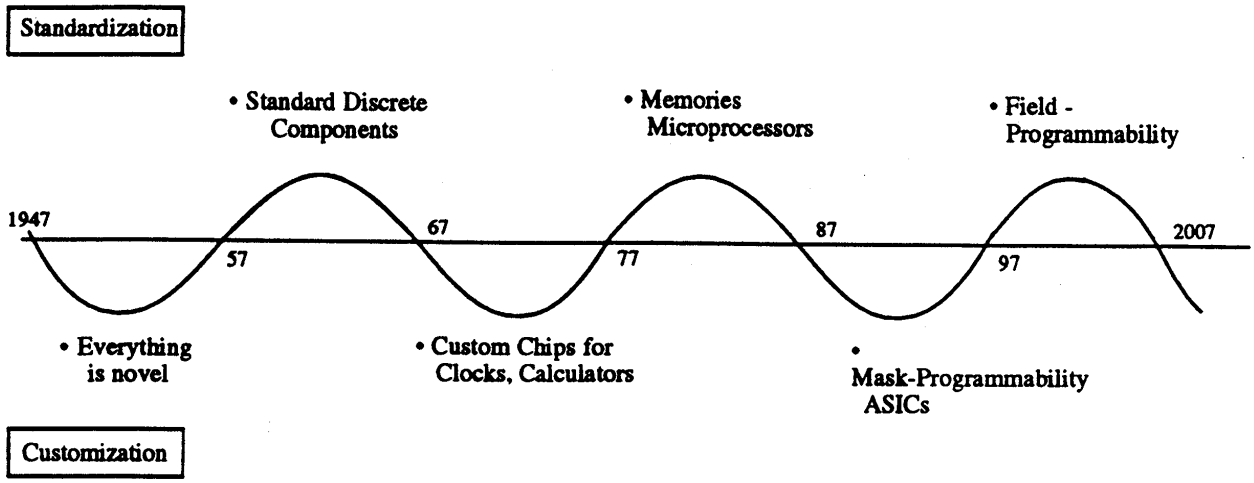

Fig. 1 Makimoto's wave: (So-called by David Manners, Electronics Weekly.) Tsugio Makimoto from Hitachi Semiconductor suggested the alternation of standardized and cutomized semiconductor products with a 10-year half-cycle.

functionality is critical as well: Thus multiple-input NAND blocks are not significantly better than two-input ones. A particular conclusion of extendible relevance is that multiple-input lookup tables provide a very high level of performance, with the improvement being most dramatic in the change from 2 to 3 inputs, and approaching insignificance at 5 or 6 inputs. It would seem therefore that our goal, certainly for binary, and possibly for multiple-valued systems, should be relatively high-level functional modules, with at least 3 inputs.

The MVL full-adder modules described in Refs. (18) and (33), are interesting examples of such a possibility. Our challenge, of course, is to identify more of these.

Field Programmable Gate Arrays (FPGAs)

Binary FPGAs: The immense interest in binary FPGAs since their first introduction in 1985 by the Xilinx Company is well-represented in a very recent book by Brown, Francis, Rose, and Vranesic at the University of Toronto.[5] Rather than being the more usual collection of recent papers, it is written as a text which provides a very timely overview of the field, focusing on the principles underlying the products of 10 of the nearly two dozen current commercial producers. As well, it provides a good up-to-date view of basic research in FPGA architectures and application tools (with references into 1992 for example). Of considerable interest in the present context is a set of empirical studies of the performance of a parameterized variety of available architectures with respect to area and speed performance over a range of applications:

The benchmark circuits, on which the comparisons are based, vary in complexity over a range corresponding to two-input NAND implementations requiring from 400 to 2000 gates. The basic logic blocks in the architectures considered include Look-Up Tables, AND-OR networks (PLAs), Multiplexors and NANDs. Most of the tradeoffs revealed relate to aspects of programmable signal routing, the space it requires, and the fact that the delay in a programmable connection far exceeds that in a direct-wire link.

On the basis of the binary studies reported, some very interesting conclusions can be drawn, conclusions which are of direct relevance to the possibilities for multiple-valued (MV) extensions: Generally speaking, for improvement in overall average performance as measured in terms of increased area utilization or speed:

(1) Fine-grain logic blocks, with low functionality, such as the 2 input NAND, are universally a poor choice due to their associated connection-space and connection-time overheads.

(2) More complex logic blocks are generally better, although overly-complex blocks, requiring too many input pins, are a poor choice. In particular, Look-Up Tables (LUT) are likely to be best, with 6 inputs possibly being optimal, but with 4 inputs showing a large fraction of the total improvement available.

(3) Performance is best measured on the basis of logic functionality per pin. Thus, for example, a multi-input NAND is a poor choice; but for a NAND of any size, the addition of an inverting output option will improve performance. Likewise, overly-wide AND-OR structures are not effective.

(4) Non-homogeneous arrays may be a direction for improvement. That is, variety in logic-block structure and functionality may be of some use.

(5) Hierarchical organizations involving a variety of programmable-connection lengths may be better than flat ones, since local connections are clearly more efficient, requiring both less space and less time.

Multiple-Valued FPGAs: In the context of the overview of binary FPGA performance characteristics just presented, it is interesting to consider the possibilities which multiple-valued technology present. Some potential benefits are immediatly apparent: Certainly, multiple-valued radix-r signal encoding will increase the overall information efficiency, since each programming switch and each line in the interconnect structure will carry $\log_2 r$ times the information available in a binary link. Certain, as well, is the likelihood that MV logic blocks will have greater functionality per input, than their binary counterparts. Furthermore, table-lookup is a relatively straightforward technique as indicated by Refs. (2), (5) and detailed shortly. Interesting, as well, is the existence of a relatively long history of research concerning MV and PLA structures of various kinds.[32]

4. Technological Change

While, shortly, we hope to show that selected partially multiple-valued techniques can offer some advantages over exclusively binary approaches, technology is (and will likely always be) binary-logic-driven. Thus we see a rapid trend to reduction in feature size suited to maximizing the packing density and speed of inherently information-limited binary circuits.[31] Regrettably, however, device scaling is not straightforward: One important non-linear aspect is the increasing importance of hot-electron effects at high field intensities.[24],[26] This fact, together with power-supply considerations for portable equipment, motivate a concern for operation at reduced power-supply voltages.[8],[38]

Yet the inherent device thresholds limit available options. Thus, while BiCMOS is a straightforward improvement at large supply voltages (5 volts),[17] it is less obviously relevant at very low ones. As well, though MOS device thresholds can be reduced by implants, sub-threshold conduction then becomes a more critical issue. On yet another front, down-scaling

of long interconnections is not straightforward (Ref. (28) versus Ref. (49)) due to the effects of line capacitance and crosstalk. Thus interconnection begins to dominate, even more than in the past, in both relative speed and space occupied. One solution available is that of additional metal layers.[28] Of course, yet another is multiple-valued signalling,[3],[4] as we shall shortly explore.

At the same time, at the system level, there is an increasing trend to mixed-signal ICs incorporating both digital and analog technology.[1],[12] Clearly, such a trend tends to support the possibility of a multiple-valued environment. For related reasons at the signal-processing level, there is an increasing acceptance of modular (cafeteria-style) processing in which technology variety is accepted, and even encouraged, for particular purposes. Thus one sees for example the existence of both complementary bipolar and complementary MOS IC processes available together.[14] A trend related to both the mixed-signal and modular-processing mindsets is toward the availability of dielectric isolation employing so-called bonded wafers. Another similarly-motivated trend is toward an increasing complementarity in design, of which the universality of CMOS, the emergence of combined CBJT with CMOS,[16],[35] and the use of complementary signalling in memory[39] and communication over even modest intra-chip distances[47] are diverse examples. All of these trends, in general, and in detail, provide implicit support for the possible selective use of multiple-valued techniques together with explicit tools for their application.

There are as well far more dramatic changes,[46] which while falling short of the potential impact of nanotechnology,[40] would open new vistas in IC design, both binary and multiple-valued. Amongst these is the potential for mixed-material fabrication, such GaAs on Si,[27] which opens up the possibility of optical intra-chip clock distribution and global critical-signal transfer in large chips, for example. Other possibilities include Silicon-Carbide technology[25] for high-temperature operation and increased chip dissipation, as well as the potential for high-temperature superconductors[25] for both signalling and logic.

5. Coping with Reduced Supply Voltages

As noted earlier, an inevitable trend with which MV ICs must cope is toward lower and lower supply voltages, certainly 3.3 V or so, and likely even lower.[38] The immediate consequence is the need for the MV community to take an appropriate decisive step *now* in order to be able to focus its energies:

Basically speaking, voltage-mode-dominated multiple-valued logic (MVL) will be increasingly difficult. Maintaining the traditional dependence in voltage-mode MVL circuits on multiple device thresholds will limit the available radix as supply voltages reduce. Some variable-threshold MOS ideas may be marginally more viable, but device tolerances and noise margins at low voltages combine to reduce available options. An interesting possible exception is a selected fraction of the possible applications of the neuron transistor (νMOS) device recently introduced by Shibata.[36] In this device, shown in Fig. 2, a floating gate, whose potential can be established through the tunneling and hot-carrier mechanisms employed in Flash EPROM,[23] is interposed between a multiplicity of input gates and the MOS device channel. Now, through the (possibly weighted) capacitive network formed by the input gates and the floating gate, signals corresponding to limited-valued input voltages can be added and subtracted to provide an unconstrained signal-derived voltage on the floating gate. Thus, for example, if the floating gate is common to both devices of a CMOS inverter, a controllable-threshold threshold-logic gate results. For binary inputs, operation is straightforward, with a compatible binary output produced with a very widely controllable threshold. For multiple-valued input voltages, the input voltage and value set are constrained by the supply as usual. As noted elsewhere,[37] other options are available as well.

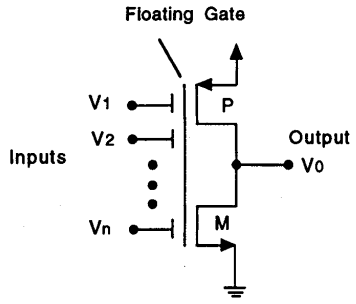

Fig. 2 A floating-gate CMOS inverter using νMOS transistors: This threshold circuit accommodates multiple area-weighted inputs with both preset and adjustable thresholds, using the floating-gate preset potential and one or more of the V_i inputs. Specifically, the floating-gate net gate potential is $\Phi_f = (\sum C_i V_i) / (\sum C_i + C_o) + \Phi_{fo}$.

Thus, with the exception of some ways of using νMOS and like devices, evolving multiple-valued circuits will be dominantly current-mode,[42],[45] emphasizing current mirroring[11],[48] and current splitting.[6] But why is this ? The basic underlying issues are illustrated in Fig. 3 which presents a set of transfer characteristics representative of both devices and circuits. For some interpretations, it is useful to think of the axes representing the same variable, either voltage or current, with the horizontal axis for input and the vertical for output, both on the same scale. In the latter context, the straight line at 45° illustrates the property of input-output compatibility which characterizes the usual

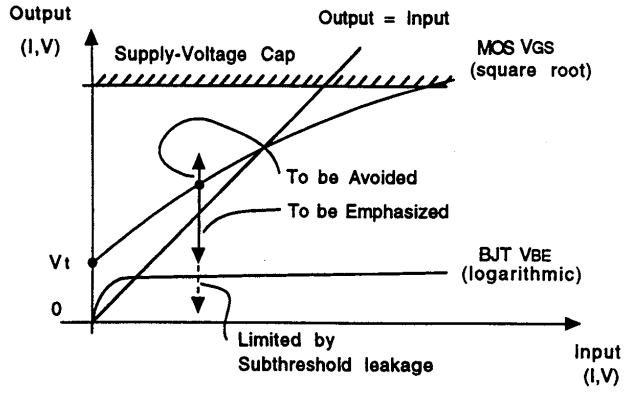

Fig. 3 Schematic input/output signaling and device characteristics.

(non-inverting) logic gate. Note that the possible effect of limited power-supply is indicated by the voltage cap on the output axis. The corresponding input voltage cap is not included for several reasons, including the possibility of a floating gate as used in the νMOS device. As well, there are depicted the V_{BE} and V_{GS} voltages of BJT and MOS devices respectively. The BJT can be seen to represent all V_{BE} ($\approx$0.7 volt) characteristic of a particular semiconductor material (silicon), with the current scaled suitably. On the same voltage scale, a range of possible V_{GS} is indicated, with the normal zero-current voltage value, V_t, being higher than the typical value of V_{BE}.

While it is possible with suitable implants to reduce the value of V_t, the available range is limited by subthreshold leakage (particularly at elevated chip temperature), and the acceptable chip-power level.[8] That the normal V_{GS} curve is drawn higher than V_{BE}, and diverging from it, is indicative of the low g_m which characterizes the FET structure of similar size.

There are several broad conclusions to be derived from Fig. 3. *First*, for low values of input, that V_{GS} is above the 45° line is indicative of the possibility that operation is not possible at very low voltages. *Second*, that the V_{GS} curve is shown to intersect the voltage cap defines the maximum range of operation both for device output voltage and input current. *Third*, note that, with low enough V_{GS} and high enough g_m, the current limitation can be made as remote as one wishes (but that large devices and extra-large subthreshold currents can result). *Fourth*, note that for a BJT using supply voltages greater than 1 volt or so, the limited output voltage has no immediate direct effect on the device (input) current. Now, overall, two possible very-general conclusions result: One is that for a multiple-valued system, current might logically be the nominal variable, since its range is less limited by the combination of device and supply properties (at least at the input). The other is that in such a current-mode circuit, design might be easier with BJTs than with MOS devices.

Now it is obvious that normal BJT β is limited, while FET β is essentially infinite. Thus, broadly speaking, we conclude that BiCMOS operating in current-mode circuits is likely to be the best simple choice, but that high-β BJTs may be preferred. Obviously, a complementary-BJT combined process (CBiCMOS)[14] would be the most flexible for multiple-valued design.

6. BiCMOS

As noted earlier, the long-term viability of BiCMOS seems virtually assured, although there are those who believe it to be a technological expedient relevant only to the particular current stage of development of CMOS. Presently, with emphasis on relatively high supply voltages (from 3.3 V to 5 V, but particularly the latter), relatively simple circuits allow a digital system to benefit quite easily from the superior g_m of BJTs at reasonable cost.[17] In fact, the return on the investment of an additional 4 or 5 masks to a system already using from 15 to 18, obviously allows the possible extension of life of an earlier less-costly technology. For example, it is presently acknowledged that in a fairly general context, BiCMOS at 0.8 μm can outperform generic CMOS at 0.5 μm.[17] Certainly as some future reduction in feature size reaches a sharp rising-cost threshold, the availability of such a relatively orthogonal improvement will continue to be of interest.

Particularly of interest to multiple-valued designers, as well, is the apparent general acceptance of BiCMOS in the analog-circuit community.[12],[34] Certainly the relatively high g_m, high r_o, low V_{BE} with its exponential behaviour over a wide range of currents, and good matching, provide a remarkable set of incentives, of direct relevance to multiple-valued designers. Of course, the important major disadvantages of BJTs are relatively low β and the negative aspects of saturating behaviour, namely a non-zero offset voltage, charge storage, and recovery delay. Note that the fact that the negative effects of saturation are relatively easily avoided in analog applications, makes it less-than-straightforward to draw conclusions on the viability of multiple-valued BiCMOS from success there.

Solutions to the problems of BJTs in digital circuits at lowering supply voltages appear to lie generally in the direction of the use of complementary BJTs and/or cunning circuits,[16] with the issue of low β being much less serious in binary than in multiple-valued systems, as noted below:

7. A New Challenge: BiCMOS and Current-Mode Logic

Let us begin by recalling and reinterpreting the rise and fall of binary I^2L, and with it the failure of what seemed at the time to be potentially commercial MVI^2L. It is useful to note that the failure of MVI^2L

was coupled in several ways directly to the fate of binary I^2L.[10] In that context, it is important to recall the origins of I^2L as an early logic form, offering very-low-voltage operation and ease of low-cost fabrication utilizing the multiemitter BJT techniques evolved in the creation of T^2L. Thus, in summary, binary I^2L was a time-stamped technological expedient offering a variety of relevant features including low-cost fabrication, low delay-power product, and the possibility of speed-power exchange. While the rapid development of MVI^2L was very exciting, it took some time to realize that it was in multiple jeopardy. First, MVI^2L really required a much higher current gain than was needed in regular I^2L, and, in particular, much more gain than the small multi-emitter transistors could provide in inverted-mode operation. Secondly, subsequent improvements in binary I^2L, aimed at speed improvement through the use of Schottky diodes, were not extendible to the multiple-valued situation. As we all know, the net result of this, aided by other circumstances, was the rapid demise of MVI^2L. The importance of reminding ourselves of this piece of history, is to dispel any sense of deja vu that may otherwise accompany an exploration of BJTs in low-voltage current-mode MVL, such as interesting new developments recently reported in Refs. (42), (45).

8. Directions for Circuit Implimentation

8. 1 T-Gate Implementations

The T-gate, as a multiple-valued multiplexer, appears to be a fitting candidate for an MV-FPGA building block. The T-gate has a long history,[41] being first proposed in 1956 by Lee and Chen,[19] prior to the most recent resurgence of interest in multiple-valued logic (MVL), as a versatile component of a complete MV logic set. In its usual form in radix r, it uses $(r+1)$ inputs, one of which controls the connection of the others to its single output.

Interestingly, in the studies cited earlier,[5] in which a general conclusion was drawn concerning the possible benefits of building blocks of intermediate complexity, relatively good overall performance was found for multiplexer-based basic blocks. In particular, a two-level multiplexer topology by Actel[9] was found to offer quite superior performance. It consists essentially of three two-input binary multiplexers in two levels, with a total of four logic inputs and three elemental controlling inputs. The possibilities which this suggests for multiple-valued implementation are intriguing: For example, in 4-valued logic, a basic block using a 4-input single-level multiplexer as input would provide for $4^4=256$ input combinations, rather than only $2^4=16$ combinations as available in the binary case, yet would employ only a single controlling input ! Being an obviously more flexible extension of a binary multiplexer, and intrinsically field-programmable, the T-gate appears to be a worthy candidate for further exploration in this context.

8. 2 A Coordinate-Selectable Programmable Multiple-Valued Signal Source

The early use by Intel[44] of multiple-valued signalling in a binary-interfaced MV-ROM was a significant development in its time. However, the technique used, namely MOS sizing in a radix-4 design, though appropriate in the technological context then, was relatively inflexible, and, being somewhat of a technological expedient, was used for only a short time. Other designs, employing gate implants[30] for radix four, appeared transiently, but were technologically difficult at the time. More recently, the latter idea of threshold variation was extended[13] to multiple-valued applications in pattern matching using writeable floating-gate devices. A generalization of the use of such devices, encouraged in part by developments in binary Flash EEPROM, is the recent work of Shibata[37] noted earlier.

The possibilities of the use of the basic floating-gate device in the creation of the multiple-valued output of a multiple-valued FPGA, are shown in Fig. 4. Note that the presentation there is relatively conceptual: Detailed design is highly dependent on the floating-gate control scheme used, and is beyond the scope of this paper.

In Fig. 4, T_{ij} is the floating-gate device shown to be accessed by binary selection signals on orthogonal (row and column) lines labelled G_i and D_j. The sketch is intended to indicate that the sources of a number of such devices are connected in common (to node S), and then to a readout mechanism involving transistor T_O. While there may be some merit in making it also a floating-gate device, it is shown here as a conventional one. In operation, one the devices in

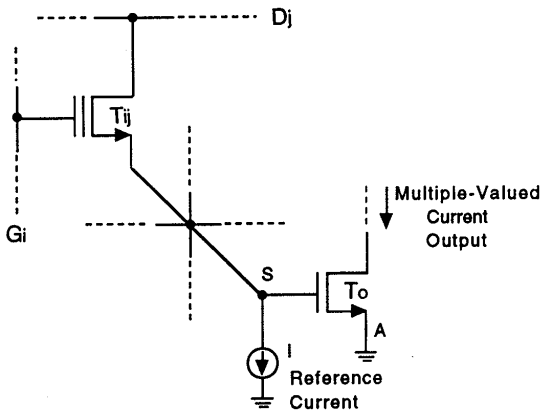

Fig. 4 A multiple-valued current-output circuit: It embodies an AND mechanism for selection by binary-valued control signals in a lookup-table structure.

the array (T_{ij}) is selected by raising signals on the appropriate G and D lines. The stability of the voltage on the D-line, which conducts the sense reference current I, need not be particularly great. On the other hand, the upper voltage level on the G-line, is quite critical, although the G-line itself is only capacitively loaded. The voltage on G could be established, for example, using a switched current source and a MOS-diode clamp for each G-line. The particular T_{ij} unit selected, accepts the reference current I for which it establishes a particular value of V_{GS} and a corresponding voltage at node S, in association with the stable upper voltage value on G.

Transistor T_O provides the corresponding output current whose value depends on the V_{GS} of T_{ij}, established by its programming. Incidentally, programming of T_{ij} from an initial "erased" state is conceived to proceed in an iterative multistep process, and to involve (and calibrate) T_O, I and the upper voltage level on G. Thus the properties of the equivalent of T_O, I and the G-source must be stable, but not otherwise precisely known.

8.3 Selective Connection of the Programmable Multiple-Valued Source

Application of the programmable signal source described above (or its functional equivalent) involve the design of an effective selection mechanism. Here, we will describe one suited to the table-look-up application introduced earlier, as a possibly effective approach to multiple-valued FPGA design. As noted in that context, the need is for control of table access by a small number of multiple-valued variables. A scheme for 2-input variables, which is particularly suited to the coordinate-accessed element in Fig. 4, is indicated in Fig. 5. While the idea is relatively radix-independent, it is illustrated in radix 4 for reasons both

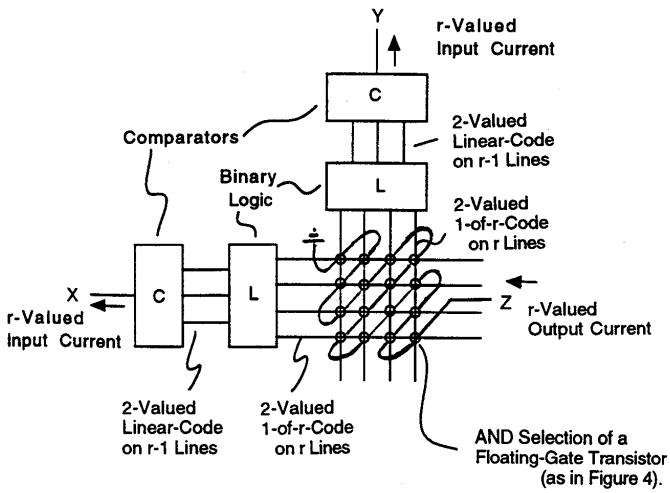

Fig. 5 Schematic organization of a lookup table (or multiple-valued ROM): It accepts two r-valued inputs and provides one r-valued output.

of convenience and potential utility.

In Fig. 5, the multiple-valued generating element is notated as a circle at the line intersections of the $r \times r$ selection array at the lower right. As noted earlier, the selection signals are 2-valued. The diagonal "snake" line, resembling the sense line in ferrite-core memories popular in the middle ages of binary computing, is representative of the common output-current path implied in Fig. 4. The remainder of the elements in the schematic are more conventional. Each r-valued (current) input is fed to a bank of $(r-1)$ current comparators (C) whose collective output is a two-valued linear-coded (or "thermometer-coded") signal on $(r-1)$ lines. These binary signals are supplied to a relatively simple logic network whose output is a binary 1-of-r code on the r lines which define one axis of the square $r \times r$ AND-selection array embodied in the selected floating-gate device.

Note that the idea can easily be extended to 3 or 4 inputs using another layer of explicit AND arrays. However, the two-input scheme shown is intrinsically more elegant, and more basic.

Possibly more intriguing than the demonstrated fact that two (4-valued) inputs are structurally convenient, is an interesting numerological relationship to the general conclusions concerning binary FPGA structures cited above. In particular, recall that 4-input binary tables were observed to produce an important performance improvement over 2-, and even 3-input versions, and that 5- and 6-input tables were better, but not by much. Now, it is possibly significant that for the binary case, with $r=2$ and $n=4$, a direct measure of internal complexity is $2^4=16$, while for the multiple-valued example case above, in which $r=4$ but $n=2$ the complexity measure is $4^2=16$, as well ! Note, interestingly, that for a 6-input binary table $r^n=2^6=64$, while for a 2-input, 8-valued table $r^n=8^2=64$ also ! Obviously, particularly for devotees of numerology, this result is potentially very significant in indicating possible directions for future study !

9. Multiple-Valued Applications

There follows a very limited selection of relatively universal, but specific, application areas for multiple-valued techniques. The attempt is merely to exemplify the potential for applications having *three* important properties: *First*, being consumer-oriented, they are perceived to represent large possible markets. *Second*, they incorporate the intrinsic attributes which I will call "radix separability", in that their multiple-valued nature need not be visible, but can be separated from the basic "digital" behaviour, by operating either in total isolation, or in a form conveniently interfaced to conventional binary signalling or processing systems. *Third*, they embody some special capability or strength of multiple-valued techniques (such, for example, as

ease of linear and truncated summation).

9. 1 Digital Filtering

Digital filtering combines a variety of properties of direct relevance to the question of IC implementation of multiple-valued circuits, and does so in a wide range of significant applications:[18]

(1) The operations, being dominantly arithmetic, are well-suited to the acknowledged strengths of multiple-valued processing.

(2) There is a need for memory, both of coefficients and for delayed versions of signal samples, for which multiple-valued capacitor-based storage is well-suited.

(3) The combination of current-mode signalling and voltage-mode capacitor storage in current-replication cells,[48] of increasing importance in modern sampled-analog signal processing, is well-established.

(4) Such current-replication cells, which incorporate and absorb the nonlinearity of a device control characteristic, provide an inherent voltage-compression capability of considerable relevance to low-voltage integrated circuits.

(5) The digital-filtering application is a classic case of the use of logic continuously at a fixed speed, where a straightforward analysis of the relative importance of static and dynamic power contributions is possible.

(6) In the usual binary implementation, there is a marked tendency to use coefficients which are convenient powers of two, in order to simplify multiplication. A corresponding approach in a multiple-valued implementation is conjectured to lead to interesting simplifications, both in the multiplication process and coefficient storage.

Note that attribute (5) above, together with the reduction in gate count inherent in multiple-valued signalling, combine to make it possible that a high-gate-count binary-CMOS implementation operating continuously at high-speed can consume more power than a suitably-configured multiple-valued current-mode equivalent!

9. 2 Analog Delay Lines

There are a variety of conceivable applications of an analog delay line or its conceptual equivalent. These include signal retiming, filtering, and other processing functions. Obviously a contender for the rote consists of a combination of an A-to-D converter at the input, a binary memory, and a D/A converter at the output. While, conceptually, the data moves in the memory as in a large shift register, in practice one would use a binary RAM, with address pointers, one indicating the location in which to place the next sampled input, and the other indicating the next location from which an output sample is to be taken.

While such a scheme is quite straightforward, it may be unnecessarily complex for some high-volume applications where the overhead of the converters of appropriate speed is relatively high. Obviously an alternative exists in the form of an analog memory requiring no converters. For all the reasons that a binary RAM is normally used, an analog RAM would likely be a suitable organizational choice.

Regrettably, in practice, analog memory is typically subject to a variety of decay mechanisms which allow stored values to change (in a possibly uncontrolled way). For some systems, in which the inherent data rates are sufficiently large and cells are rewritten at short intervals with new data, the basic scheme is appropriately straightforward. However such is not always the case! In the event that the natural replacement interval is somewhat longer than appropriately-precise analog samples can be sustained, some special action must be taken. Note that the possibility exists of quantizing the stored signal, and then using some creative multielement multiple-value-computed error-correction scheme to extend the useful storage interval. A simple early version of this idea, spanning only a single memory element, appears in Ref. (20).

9. 3 Bandwidth-Efficient Communications

There is a long history of interest in the use of multiple-valued signaling in communication systems founded on an attempt, through the use of waveshaping techniques, to reach (and ultimately to exceed) Nyquist's limitation of at most 2 (binary) symbols per second per Hz of channel bandwidth. In such a system, a symbol (either a 0 or a 1) is represented by a (shaped) pulse of unit amplitude and either negative or positive polarity. At a relatively early stage, it was realized that varying the amplitude of the pulses would allow greater information to be packed per unit of time and bandwidth. However, for such systems, called, then and there, multilevel or M-ary, the improved performance did not appear to justify the perceived cost of equipment and increased noise sensitivity, and increased error rates. Thus, early on, such multiple-valued systems were mere curiosities.

Then in 1963, or so, a new idea called correlative or partial-response signaling[29] was introduced, in which memory of the previous symbol(s) sent is used to modify the one next transmitted. The situation first explored was based on the most common ± 1 unit binary-pulse form, but incorporated the simple idea of modifying each (pulse) sample symbol sent to have a value equal to the sum of that of the present and the immediate-past pulses. It is apparent that for an original ± 1 sequence, the modified result is 3-valued, having amplitudes ± 2 and 0. This signal form is called duobinary. Having two extreme and one intermediate values, it can be observed to tend to be

bandwidth-conserving, simply by the fact that all major transitions between the extreme signal values are moderated by the intervention of the intermediate value, making the output signal somewhat "smoother". However for this simple scheme, the detection process, which depends on subtraction of the previously-received from the presently-received value, will propagate errors.

Shortly after this problem was perceived, its solution was conceived by Lender[29] who introduced a non-linear precoding scheme using a feedback mechanism operating on the original conventional binary (0, 1) data. In this scheme, the present binary output is formed from the Exclusive OR [the Mod-2 sum] of the current binary input with the previous binary output. This output value is then doubled and 1 subtracted to produce a ± 1 unit sequence which is then fed to the process described above, of summing the current and immediately-past signal samples, as in the original scheme. The combination of the feedforward and feedback processes results in the elimination of the effect of history (and of propagated error) of the received data: Either positive or negative received data represents logic zero, while a zero received value is interpreted as logic one. Interestingly, this system, called modified duobinary, has some special signal properties which make it even more easily handled in a bandwidth-restricted system, namely: It has no dc component; Adjacency of positive and negative values does not occur: Positive and negative values are separated by an odd number of center-value samples; Peak values of the same polarity are separated by an even number of center values. Amongst possible application of these properties includes the possibility of relatively simple transmission-error detecting mechanisms. These ideas are directly extensible to M-ary systems in which the number of output levels is $[2M-1]$.

In M-ary systems in general, the multiple-valued operations required are dynamic storage, summation, mod-M summation and thresholding. Generally speaking, the use of memory in an M-ary partial-response coding scheme reduces the number of levels needed. For example, in the popular case of $M=2^k$, a data-rate packing of k bits/s/Hz is available directly using a zero-memory direct multiple-valued (M-valued) system having 2^k output values. Alternatively, only $[2(2^{k/2})-1]$ output values would be needed from a correlative system using memory. For example, 4 bits/s/Hz data packing would require 16 output levels in a zero-memory system, but only 7 levels in a correlative system. Finally, even-more-complex processing can be used in systems which extend the partial-response coding idea over several sample intervals, in structures that begin to look more and more like (and are) special-purpose digital filters.

Thus we see the possibility of using multiple-valued memory and signalling in a self-contained system of relatively high commercial utilization, in modem and related applications.

10. Conclusions

This paper has attempted to provide a context for possible future developments in Multiple-Valued IC circuits (MVICs). In order to focus available energy, and make the conclusions more immediately useful, the detailed discussion has been restricted, for the most part, to relatively direct extensions of existing silicon-based techniques.[31]

Notwithstanding that choice, the development is based to some degree on a sense of the possible effect of currently-exotic techniques.[15] On that basis, one can conclude a variety of general trends: The *first* is that complementary-device technologies will be readily available,[16] as will composite processes on a cafeteria-style basis. Thus fully-complementary BiCMOS will be accessible provided cunning MVL designs can be found to use it. However, the need to pack more and more higher-speed inefficient binary circuits in an affordable package will force the attention of manufacturers to smaller and smaller feature sizes. This pressure, and the emphasis on portability, will force readily-available IC processes toward restricted lower-voltage operation.

There will of course be exceptions, motivated in part by the intrinsically higher-voltage needs of analog design. However, the increasing importance of mixed analog and digital in mainstream ICs will tend to dampen and delay this process, to a degree which depends on the current (high) growth rate of switched current-mode techniques. This is doubly fortunate, since some of the techniques forced on analog designers are very relevant to MV design. Nevertheless, the trend will inexorably be, as it always has been, toward technologies which satisfy the dominant needs of binary digital practitioners. It is a combination of the overall current trend to customization, with the accompanying modular cafeteria-style technology selection, which may allow an enlarged window-of-opportunity for MV designers. However, to ensure success, more is needed: In particular it is *essential* that a major effort be launched, by those intrigued by MV logic, to identify uniquely-MV-adapted solutions to important problems of known interest to industry.

Toward this end, an attempt has been made here to identify some candidate applications and circuit techniques appropriate to their solution. In general, the emphases identified, include the use of current-mode signals, coupled and controlled by capacitor-based dynamic memory, in conjunction with flash-technology-based programmability in field-programmable MV systems, which are invisibly-digital or radix-distinguished, being either self-contained or

binary-interface adapted.

Thus, as usual, multiple-valued digital is in a game of opportunity with binary digital, but a new one in which analog has yet to definitely choose sides. The good news is that the playing field is getting bigger and flatter; The bad news is that the ground is getting harder. If we fall now, we might hurt ourselves permanently!

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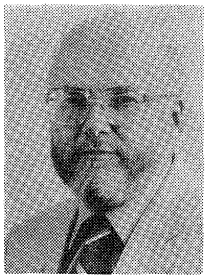

Kenneth Carless Smith obtained his PhD in (Solid-State) Physics in 1960 from the University of Toronto, where he is presently a Professor of Electrical Engineering, Mechanical Engineering, Computer Science, and Library and Information Science. As well, he has extensive industrial experience in the design and application of computers and electronic circuits, as employee, manager, administrator, entrepreneur, consultant, and educator. His research interests currently include analog VLSI, multiple-valued logic, flexible manufacturing, machine vision, instrumentation, array architectures, human factors, and reliability. He is widely published in these and other areas, with well over 150 journal, proceedings, books, and book contributions. He was elected Fellow of the IEEE in 1978 for "Contributions to Digital Circuit Design," and Honorary Professor at the Shanghai Institute for Railway Technology in 1989.

P. Glenn Gulak is an associate professor in the Department of Electrical Engineering at the University of Toronto. His research interests are in the areas of circuits, algorithms and VLSI architectures for digital communications and signal processing applications. He has twice received the computer science Students Union undergraduate teaching award for courses he has taught on computer architecture. Dr. Gulak received his Ph. D. from the University of Manitoba while holding a Natural Sciences and Engineering Research Council of Canada Postgraduate Scholarship. From 1985 to 1988 he was a research associate in the Information Systems Laboratory and the Computer Systems Laboratory at Stanford University. Since 1990 he has served on the ISSCC program committee (signal processing sub-committee).