Through the Looking Glass II—Part 1 of 2

Trend Tracking for ISSCC 2013

What follows is a sampling of recent analyses and predictions by selected subcommittees of the International Solid-State Circuits Conference (ISSCC) 2013: Analog, Data Converters, RF, Wireless, and Wireline.

Trends and predictions by the remaining subcommittees (EED, HPD, IMMD, Memory, and TD) will be published in the Spring 2013 issue of this magazine.

Introduction

There is a long tradition at ISSCC of striving to extend the conference's role as the foremost global forum for the presentation of advances in solid-state circuits and systems-on-a-chip (SoCs). But this implies a great deal of effort on the part of many people. One of the most important elements of this effort is the structuring and organization of the Program Committee, including its subdivision into ten subcommittees, each focusing on diverse technical areas, and their dynamic growth and adaptation through the selection of world-renowned specialists. One of the many techniques used by each subcommittee to remain at the forefront of evolving technology is the identification and maintenance of trend information, on the basis of which new developments become startlingly clear.

The intent of this article is to share with members of the IEEE Solid-State Circuits Society (SSCS), a sampling of the views held by the diverse group of experts represented within the Program Committee, which for ISSCC 2013 is composed of 161 members, including ten subcommittee chairs. These members are divided into ten subcommittees whose size ranges from 12 to 18 people. This year, the subcommittees are focusing on the following areas: analog; data converters; energy-efficient digital; high-performance digital; imagers, microelectromechanical systems (MEMS), medical, and displays; memory; radio frequency; technology directions; wireless; and wireline. What follows is a sampling of recent analyses and predictions from each of the ten subcommittees.

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Analog

Analog techniques continue to have a critical role in evolving modern electronics. The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy must fundamentally be performed with analog systems. As a result, the key technologies for power management are predominantly analog. For example, currently there is much interest in wireless power transmission for battery charging applications, such as for mobile handsets and for medical implants. Increased efficiency in wireless power transmission is enabling faster charging over longer distances. As well, there is an explosion of technologies that permit energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers. Here, the significant focus is on analog circuits which harvest submicrowatt power levels from energy sources at tens of millivolts, providing autonomy for remote sensors or supplementing conventional battery supplies in mobile devices. To achieve this, extremely low power must be consumed by the attendant analog circuits so that some energy remains to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of such low power systems. Fast power up and power down are also required of these circuits to permit high energy efficiency during intermittent operation. In combination, these analog power-management technologies will permit devices to be powered indefinitely from sustainable sources, opening the door to many evolving applications, including ubiquitous sensing, environmental monitoring, and medical instrumentation.

Analog circuits also serve as bridges between two worlds—the digital computational and the analog real. Just like road bridges, analog-circuit bridges are often bottlenecks, and their design is critical to the overall performance, efficiency, and robustness of the system they support. Nevertheless, digital circuits such as microprocessors drive the semiconductor market; thus, semiconductor technology has been optimized relentlessly for the past 40 years to reduce the size, cost, and power consumption of digital circuits. Correspondingly, analog

circuitry has proven increasingly difficult to implement using these optimized-for-digital integrated circuit (IC) technologies. For example, as the size of transistors reduced, the range of analog voltages they can handle decreased, and the variation observed in their analog performance increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies that may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency-lighting applications. However, other applications dictate full integration of both analog and digital circuits in the smallest-feature-sized modern digital technologies. One important example is microprocessors where multiple cores are able to reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are represented in Figure 1 by movement toward the top right.

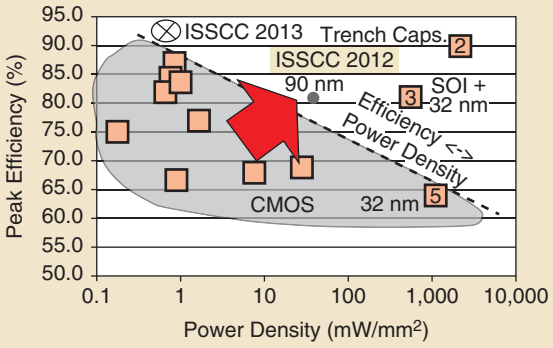

FIGURE 1: The development of integrated power conversion: each year, more and more is integrated in standard CMOS technologies, optimizing efficiency versus power density. At ISSCC 2013, these trends are evident in a shift to higher performance, as shown by the arrow directed to the upper right. (Adapted courtesy of ISSCC 2012 Paper 5.4.)

Thus, we see analog techniques continuing to thrive while expanding in support of new demands for power efficiency driven by digital developments.

Data Converters

Data converters serve as key building blocks in almost all known applications that bridge the analog physical world with the digital circuits that dominate modern integrated circuits. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be key drivers for innovation, as evidenced by the data converters presented at ISSCC 2013.

Figure 2 shows energy efficiency expressed as power dissipated relative to the effective Nyquist sample rate (P/f_{snyq}) as a function of the analog-to-digital converters (ADCs) signal-to-noise ratio (SNDR). For low- to medium-resolution converters, energy is primarily expended to quantize the signal; the efficiency of this operation can be measured as the energy consumed per conversion step -the so-called Walden figure of merit (FoM)]. The dotted trend line in Figure 2 represents the benchmark of 10fJ/conv-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of the signal-to-noise ratio, as shown by the solid line. For ISSCC 2013, contributions are indicated by the colored dots representing various converter architectures, with previous years denoted by the smaller dots. (Note that a lower P/f_{snyq} metric represents a more efficient circuit.) Several new SAR-based converters at various SNDR design points continue to extend the limits of energy efficiency, and push into previously unchartered territory.

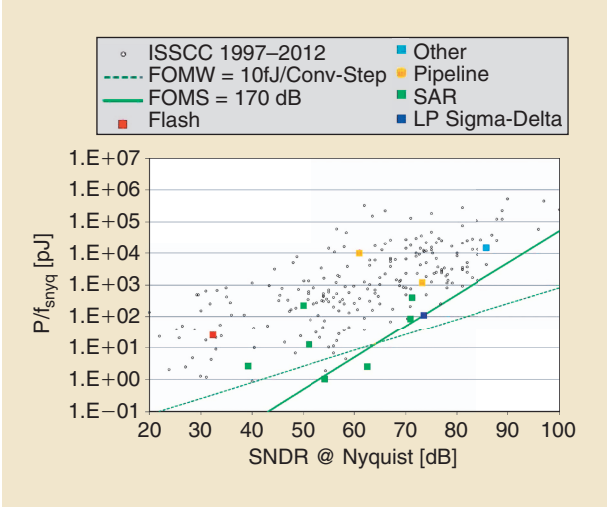

FIGURE 2: Power efficiency versus SNDR (highlighting ISSCC 2013 results).

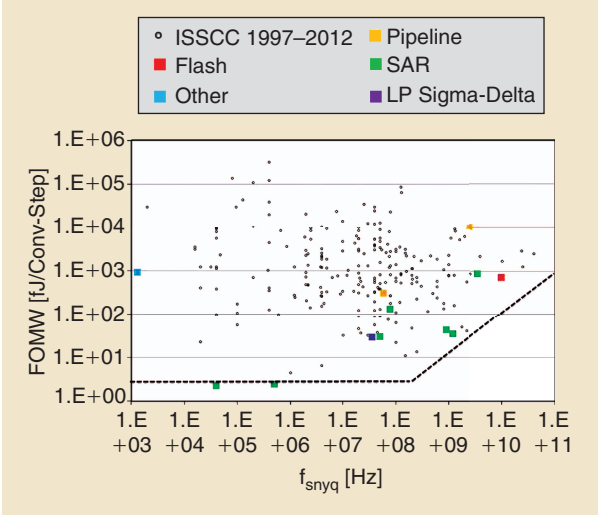

FIGURE 3: FoM (energy per conversion step) versus Nyquist bandwidth for various converter.

Figure 3 shows energy per conversion step versus the effective sample rate. This figure elucidates the difficulties of high-speed operation for a given technology. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the spectrum of conversion rates.

Finally, Figure 4 shows achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nevertheless, at ISSCC 2013, we see many examples that set new records in this metric, utilizing several different converter architectures.

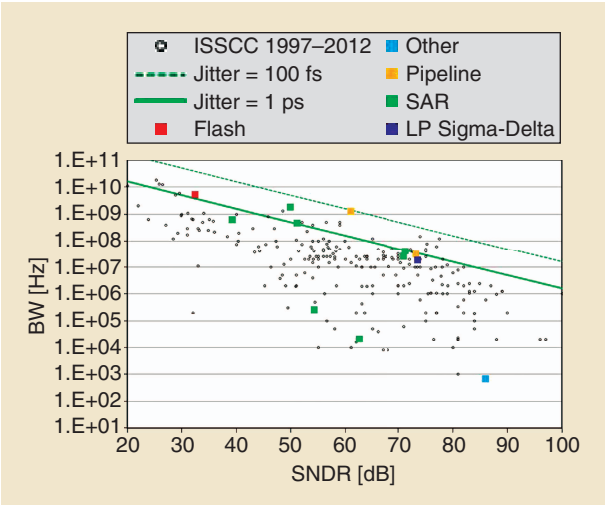

FIGURE 4: Bandwidth versus SNDR.

Converters continue to evolve in support of the increasing demands of new applications motivated by the availability of faster decreasing cost digital circuits.

Radio Frequency (RF)

Across the broad spectrum of RF applications in all frequency bands, this year ISSCC 2013 provides evidence of increasing integration and technical maturity, while at the same time, innovation proliferates. What follows outlines emerging RF trends to be revealed there.

There is an ongoing drive toward increasing levels of integration in all areas of RF design, from mm-Wave, to cellular, to imaging, to wireless sensors. In mm-Wave designs, higher system complexity (including front-end, synthesizer, and baseband) is increasingly being integrated onto a single die. In cellular, the push for integration has led to a strong trend toward architectures, allowing better linearity and coexistence of these multiple bands and standards. A related trend has been increasing research directed toward removing costly and bulky SAW filters and duplexers. Some of these efforts include the creation of highly linear blocker-tolerant receivers, mixer-first receivers, feedback blocker cancellation, feed-forward blocker cancellation, N-path filters, and electrically balanced hybrid transformers. Strong effort continues toward the integration of CMOS PAs, while delivering viable power-efficiency performance. Overall, this year at ISSCC 2013, there has been a marked appearance of a significant number of chips in 65-nm CMOS as opposed to other technologies. This observation can be noted across all frequency ranges and all circuit topologies. It is evident from ISSCC 2013 that RF devices will continue to see larger levels of integration at the chip- and package-level for years to come.

Over the past decade, the papers submitted to ISSCC have indicated a clear trend toward higher frequencies of operation in CMOS and BiCMOS. This year, this continues for oscillators, mm-Wave amplifiers, and PAs. Another trend is toward the increasing complexity of systems operating in the 60-to-200-GHz range; this push to ever-higher frequencies is being pursued by both industry and academia for various applications, such as high-data-rate communication. With the low-GHz frequency spectrum already overcrowded, researchers are continuing to target frequencies above 60 GHz. Other applications for products operating in these frequency bands include imaging and

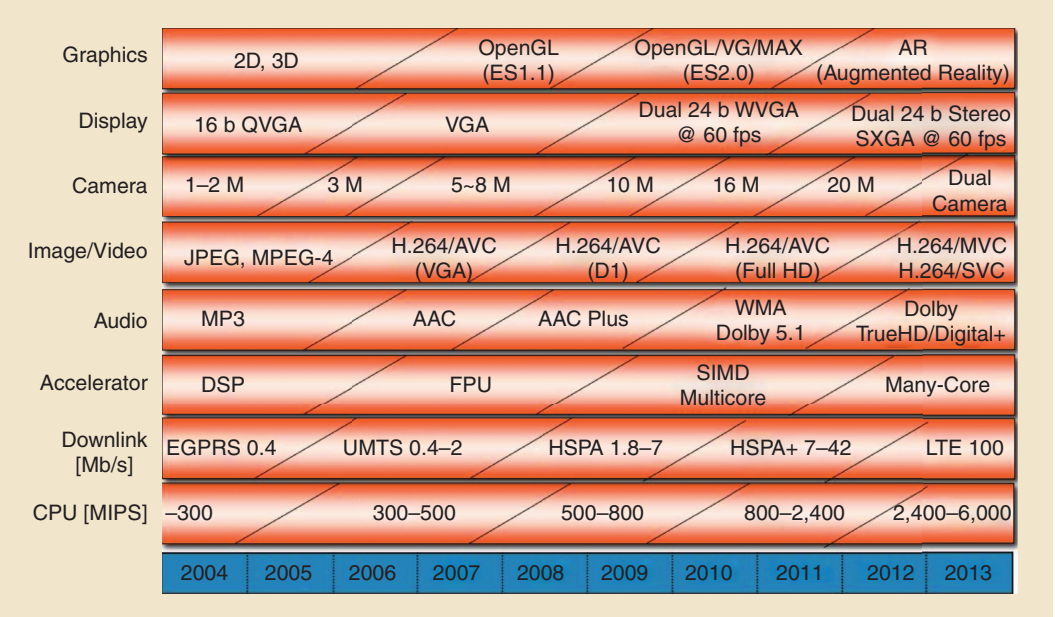

FIGURE 5: Developments in application processors for smartphones.

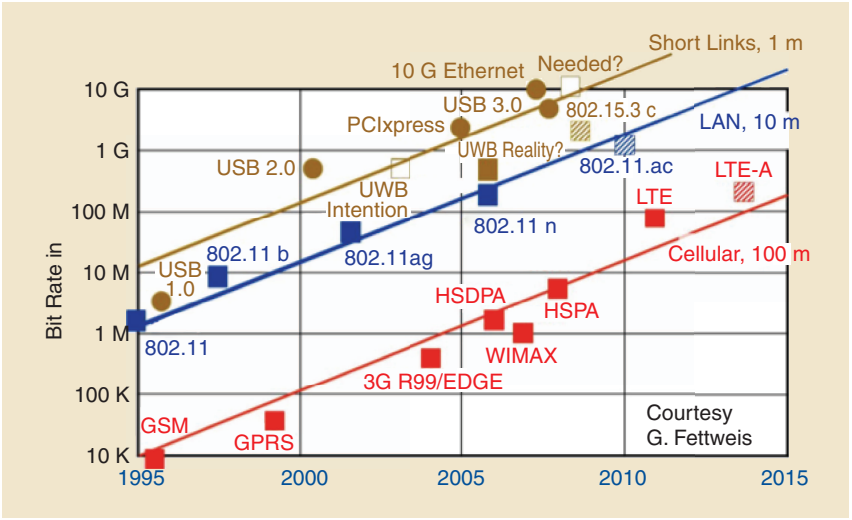

FIGURE 6: Wireless and wired data rates over time.

radar; these frequencies are desirable for such products due to their high spatial resolution and facilitation of small antenna dimensions, allowing efficient beam-forming arrays. This integration of mm-Wave antennas into silicon substrates is another increasingly visible trend.

As a consequence of the trends to increase integration and to higher frequencies, a new class of fully-integrated application-driven systems have emerged. The availability of many RF and mm-Wave building blocks in CMOS and BiCMOS is motivating fully integrated solutions for specific emerging applications in the RF and mm ranges. Single-chip radars in RF and mm-Wave frequencies with improved resolution, improved efficiency, and showing increasing levels of integration, are appearing. Similarly, new systems are being developed for ultra-wideband radar and mm-Wave wireless sensing. Developments in the biomedical field are clearly moving from the simple measurement of electrical parameters toward the measurement of real medical properties in realistic environments through the use of systems-in-package (SiP).

Complexity and Maturity in the mm-Wave and Sub-mm-Wave Ranges

The high cutoff frequency of bipolar transistors and highly downscaled MOS transistors has enabled the realization of circuits and systems operating in the mm-Wave range. In the past few years, high-data-rate communication in the 60-GHz band and car radar around 77 GHz have garnered much attention. While the integration level in these domains is already quite high, we see an improvement in the performance of various building blocks (such as the output power of PAs and the spectral purity and tuning range of VCOs).

The 100-GHz barrier for the operation of silicon circuits was breached a few years ago. Whereas initially elementary building blocks such as VCOs and amplifiers operating above 100 GHz have been realized, we now witness the trend of increasing complexity in circuits operating there. Meanwhile, the electrical performance at the building-block level has improved. As shown in Figures 17 and 18, the output power of mm-Wave and sub-mm-Wave sources and PAs has increased; as well, VCOs are operating at ever-increasing frequencies with a higher tuning range.

Coexistence and Efficiency for Cellular Applications

RX and TX Linearization

In the past few years there has been an increasing interest in techniques for improvement in the linearity of transmitters and receivers. Improved linearity of receivers will ease the requirements on RF filtering of out-of-band blockers, requiring, for example, only the use of a programmable notch filter in the RF path. Transmitter linearity improvements will benefit performance parameters such as error-vector magnitude (EVM), ACLR, and spectral purity.

PA Efficiency

PA efficiency improvements demonstrated this year at ISSCC 2013

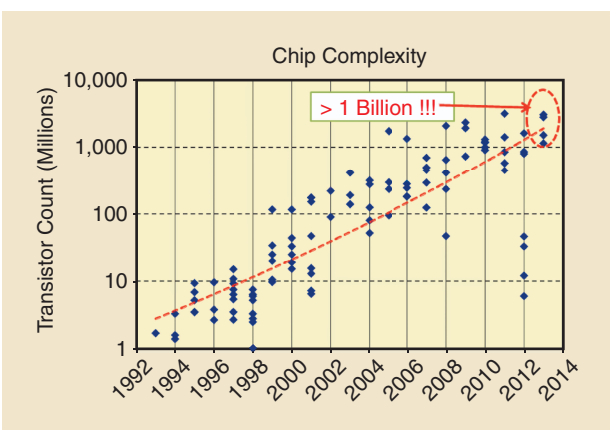

FIGURE 7: Chip complexity.

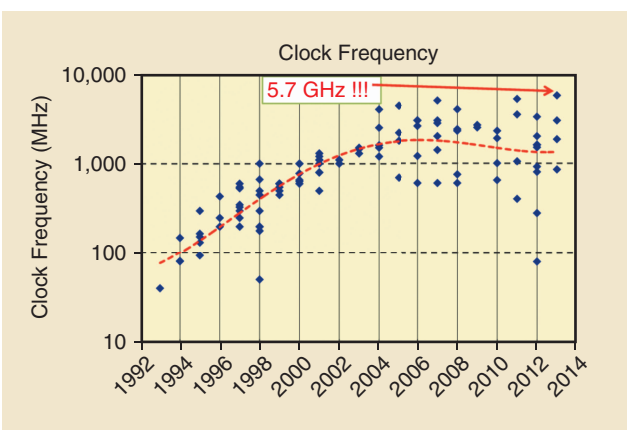

FIGURE 8: Clock frequency.

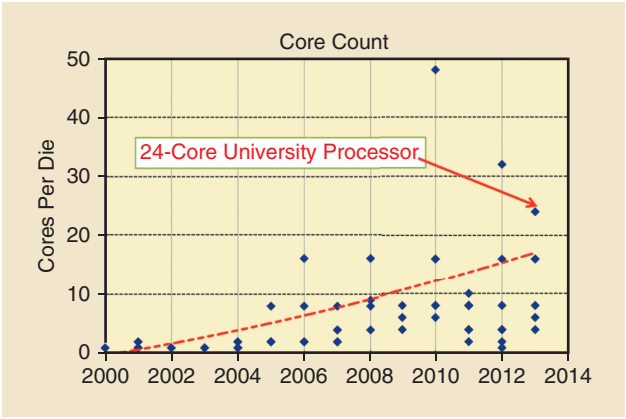

FIGURE 9: Core count.

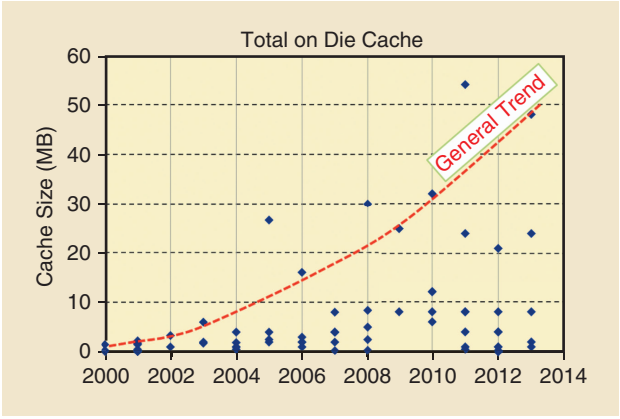

FIGURE 10: Total on-die cache.

will directly impact the battery life in portable applications. These efficiency-improvement techniques include analog and digital predistortion, dynamic biasing, and envelope tracking.

Digitally Assisted RF

The trend toward digitally assisted RF continues and is increasingly applied in mm-Wave chips. More digitally-assisted calibration techniques are being demonstrated to improve the overall performance of transceivers by reducing the impact of analog impairments at the system level. These techniques include spur cancelation/reduction, IIP2 improvements, and digital predistortion.

VCOs

There is a continuing trend toward improvements in phase-noise FoM and power consumption through circuit techniques used in Class-C and Class-D VCOs. Figure 19 shows trends in VCO FoM performance of some of the most significant VCOs published over the past decade. As can be seen, ISSCC 2013 demonstrates clear contributions to this field.

Thus, overall, we see both the improvement of sustaining RF techniques, and the dramatic extension and growth of RF toward new areas of application at ever-higher frequencies.

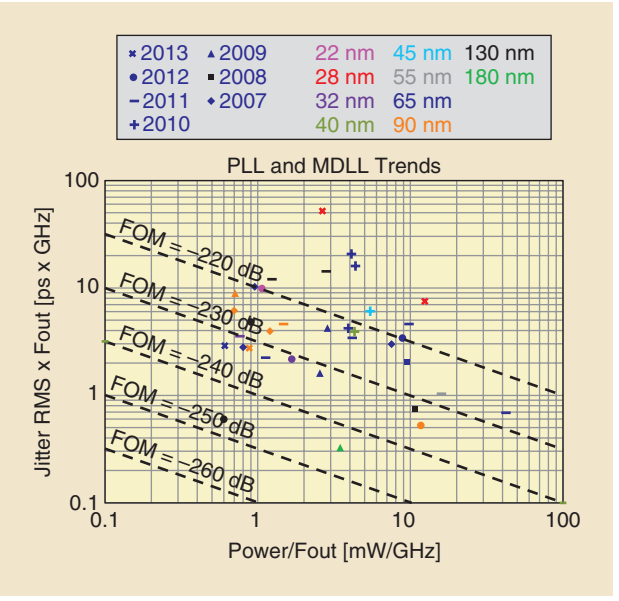

FIGURE 11: PLL and MDLL trends.

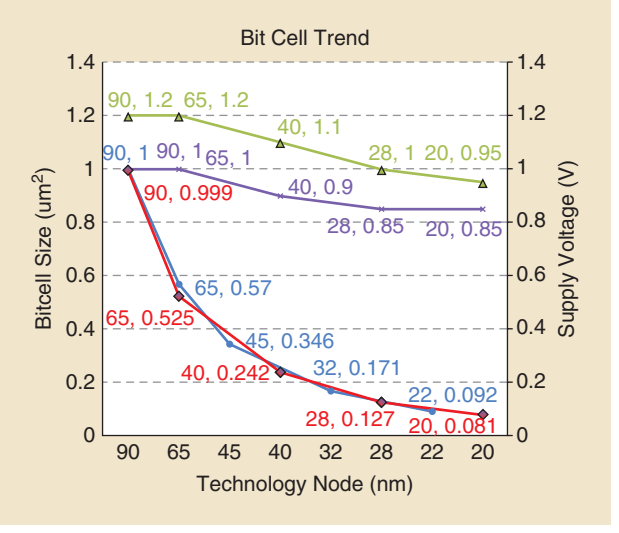

FIGURE 12: SRAM bit-cell size and supply scaling range from major semiconductor manufacturers.

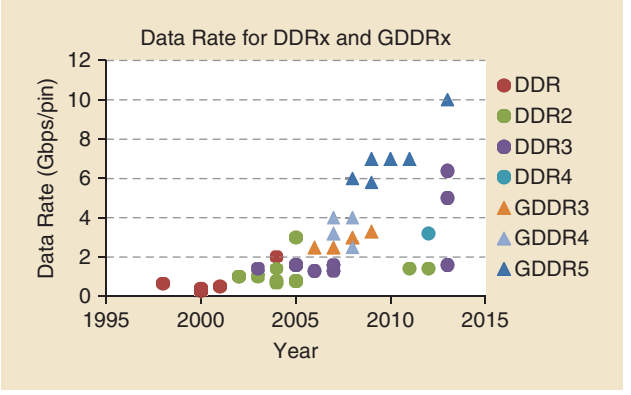

FIGURE 13: Trends in DRAM data rate per pin.

Wireless

Data rates for modern wireless standards are increasing rapidly. This is evident from the pace of the introduction of cellular standards shown in Figure 20. Note that the data rate has increased 100 times over the last decade, and another ten-fold increase is projected for the next five years. This trend is partly supported by the use of more-complex modulations [such as using orthogonal frequency division multiplexing (OFDM) for better spectral efficiency] at the cost of digital signal processing (DSP). In addition, the expansion of channel bandwidth has helped to achieve the data rate increase. This is exemplified for 802.11× in the wireless connectivity chart shown in Figure 21. The channel bandwidths for the WLAN standards has increased from the traditional 20 MHz (802.11 g) all the way to 2.16 GHz (802.11 ad). Because the available spectrum is limited in the low GHz range, for >1 GHz channel bandwidth, the carrier frequency has moved from 2.4/5 GHz (802.11a/b/g/n/ac) to 60 GHz (802.11 ad), in the mm-Wave range. With the available spectrum in the 6-GHz range, data rates up to 6.76 Gb/s can be achieved. However, design at mm-Wave frequencies comes with significant challenges with academic research oriented to the reduction of power, while industry focuses on product-quality robustness and standards compliance. Currently, a new generation of chip sets, compliant with WiGig and 802.11 ad, is ready for production.

Since spectrum is scarce, new carrier-aggregation techniques are being developed that can combine available channels in a flexible way, such as combining noncontiguous channels, or even channels in different frequency bands. Correspondingly, the new 802.11 af standard aims to utilize "TV white space," unused legacy analog TV frequency bands below 1 GHz. This will be implemented, first using a database of available channels per geographical location, but eventually high-sensitivity spectrum sensing will be used to confirm the availability of the spectrum. The possibility of opening up this large amount of spectrum generates radio challenges, such as the need for highly linear transceivers that can cover a very wide frequency range and various channel bandwidths. As a consequence of high-linearity and wideband design requirements, distortion cancellation and tunable RF channel-selection techniques are very critical. Most transceivers in this category are adopting digital calibration and analog-feedback techniques to increase the linearity performance for a flexible and tunable front end to cover a wide range of frequencies.

As wireless technology lowers in cost, it can be deployed in many

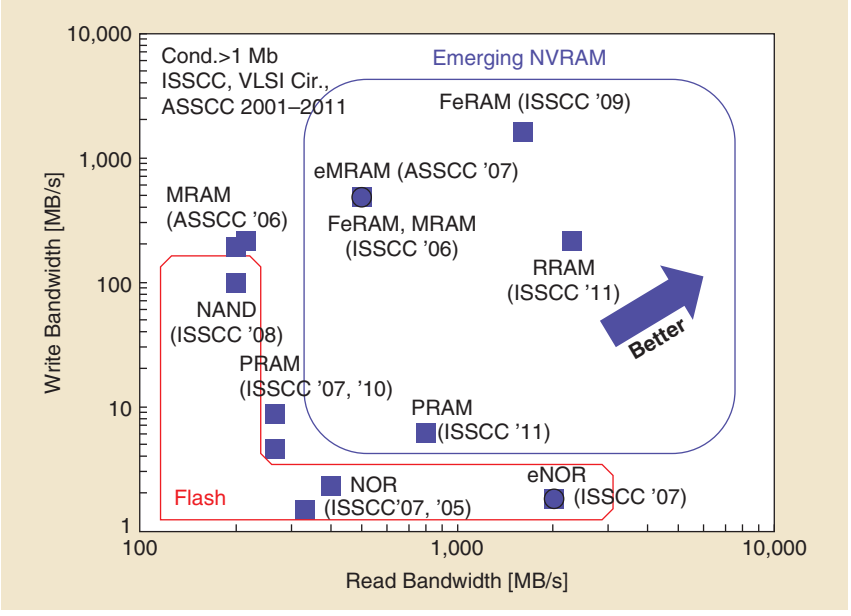

FIGURE 14: Read and write bandwidths comparison of nonvolatile memories.

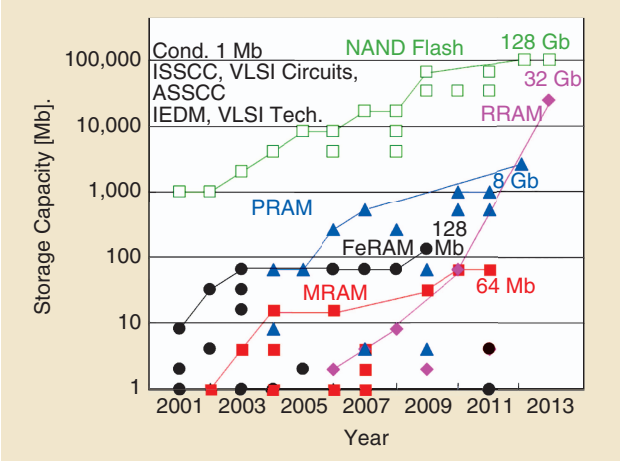

FIGURE 15: Memory capacity of emerging nonvolatile memories.

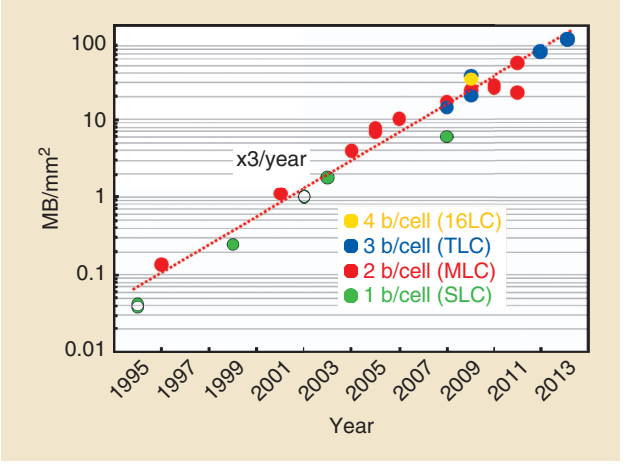

FIGURE 16: NAND flash memory density.

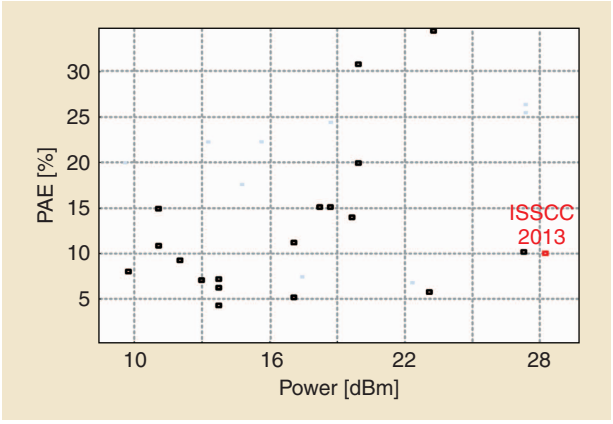

FIGURE 17: PAE versus output power for recent submicron mm-wave CMOS PAs.

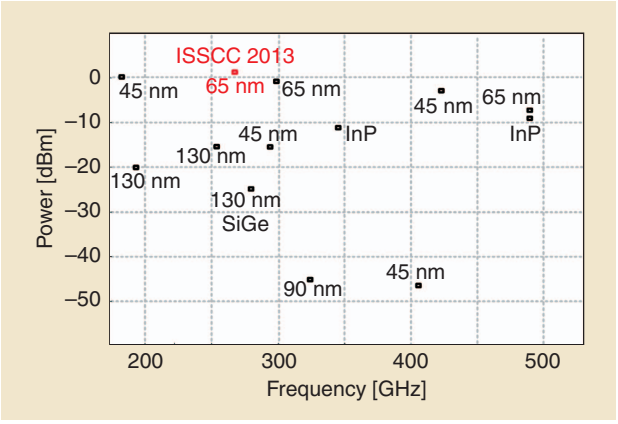

FIGURE 18: Output power versus frequency for mm-wave and sub-mm-wave sources.

devices, including sensors for monitoring environmental conditions. Wireless sensor networks (WSNs) require ultra-low-power radio to increase battery life and minimize the battery size, or, better yet, eliminate the battery altogether by using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. A "wake-up radio" that monitors the channel and alerts the "main" radio when communication is requested becomes the primary building block for WSN designs. Once the radio is awake, power efficiency becomes the main target for both high- and low-data-rate communication. Another approach is to duty cycle the radio operation, such as using the radio only for short communication bursts, which requires fast turn-on techniques. Such WSNs will enable electronics for sustainability.

Similar to the evolution in cellular, ultra-low-power radios are now becoming multistandard, covering, for example, Zigbee, BTLE, and IEEE 802.15.6. Multistandard implementation implies radio-block sharing and standards management, including modulation, frequency, bandwidth, power output, sensitivity, and so on, while maintaining low power consumption, which is one of the keys to the success of such devices. Another main concern is the price. These multistandard radios must have small-silicon-area circuits in low-cost packaging.

Near field communication (NFC) is becoming more and more popular. This new secure-data wireless transmission mode is now embedded in smart phones and will become a de-facto requirement in coming years.

Digital architectures implementing radio functions are very efficient in deep-nm CMOS. In the past years, digital-PLLs have been developed for radio front ends. Now, new digital approaches are being deployed in transmitters, targeting greater flexibility of the RF front end that leverages CMOS scaling for reduced power dissipation and area, simplifying integration in large SoCs and empowering the next generation of wireless communications.

Wireline

Wireline continues to be an important application of semiconductor

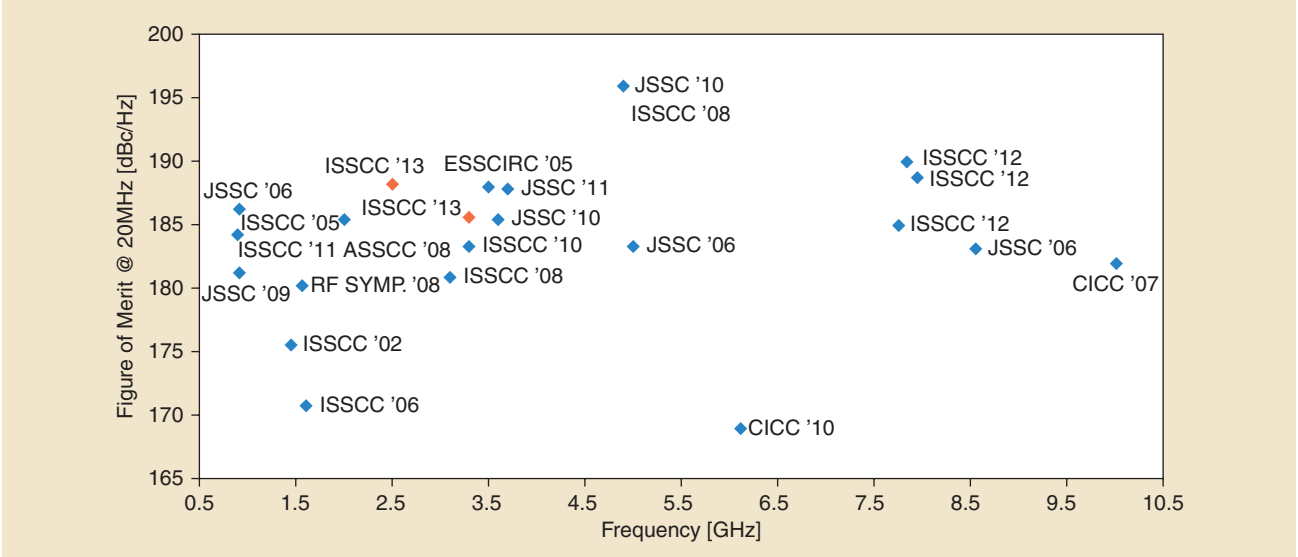

FIGURE 19: Phase-noise FoM at 20-MHz offset frequency versus oscillation frequency.

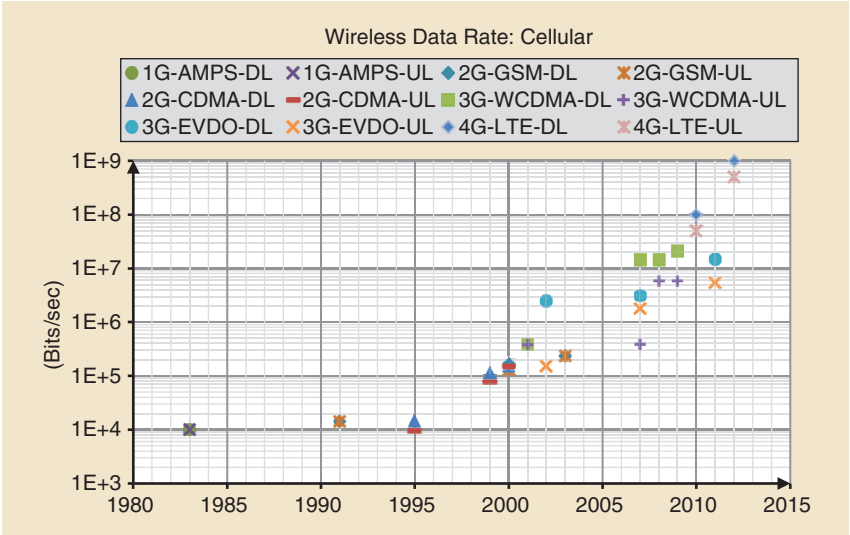

FIGURE 20: Data rates for cellular standards.

technology as the need for wired communication flows out from its long distance origins into smaller and smaller environments, through backplanes to inter- and intrachip connection. A continuing challenge in this evolution is the adaptation of techniques that originated on a large scale to shrinking environments.

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately two-to-three times every two years. Demand for bandwidth has been driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth has been enabled by expanding the number of I/O pins per component. But, as a result, I/O circuitry consumes an increasing amount of area and power on today's chips. However, increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 22 shows that per-pin data rate has approximately doubled every four years across a variety of diverse

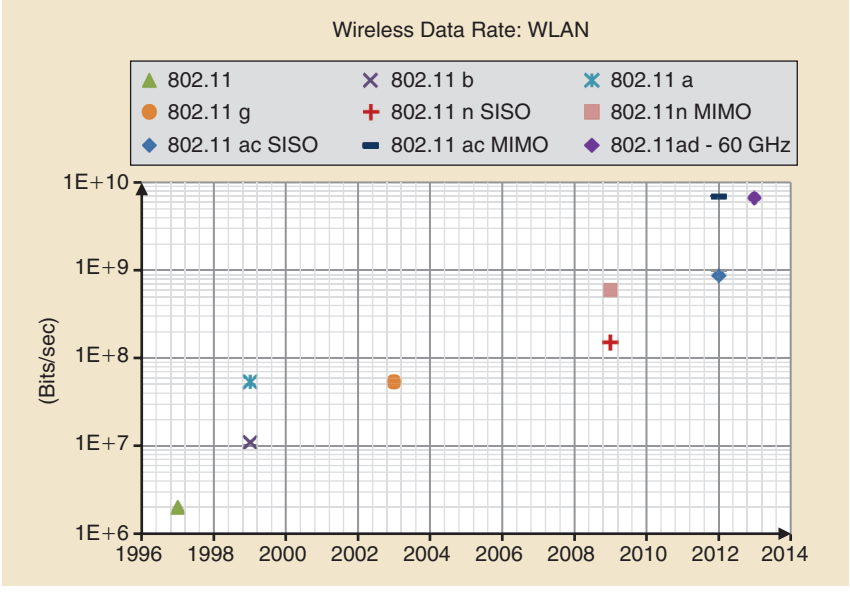

FIGURE 21: Data rate for wireless connectivity standards (802.11x).

I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 23 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process-technology scaling. However, continuing with this rather amazing trend in I/O scaling will require more than just transistor scaling in the future. Significant advances in both energy efficiency and signal integrity must be made to enable the next-generation of low-power and high-performance computing systems.

Power Consumption and Energy Efficiency

Power consumption for I/O circuits is a first-order design constraint for systems ranging from mobile phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of the total power that they consume. Technology scaling enables increased clock and data rates and offers some energy-efficiency improvement, especially for digital components. However, there is a strong correlation between the energy efficiency and the distortion introduced by the channel. Figure 24 plots the energy efficiency (expressed in mW/Gbps, which is equivalent to pJ/b) as a function of Nyquist loss for recently reported transceivers. These transceivers cover a wide variety of standards and process technologies. Based on these data points, the scaling factor between link power and signaling loss is approximately unity, meaning that required link power doubles with every additional 6 dB of channel loss. As a result, simply increasing per-pin data rates with existing circuit architectures and channels while only scaling transistors is not a viable path, given fixed system-power limits. To address this issue, recent link research has focused on reducing power through both circuit and channel innovation. There have been a number of advances that reduce power through circuit innovation, including low-power RX equalization (DFE and CTLE), CMOS resonant clocking, low-swing

voltage-mode transmitters, and links with low-latency power-saving states. Based on the relationship between channel loss and energy efficiency, power can also be reduced by changing the interconnect itself to either reduce the total loss or increase the interconnect density. Examples of these approaches include stacked die TSVs and proximity interconnects, silicon interposers, on-package I/O, and low-loss flexible interconnect. At ISSCC 2013, reported developments move the state of the art well below 1 pJ/b for short-range links. For example, a 20-Gb/s chip-to-chip transceiver consuming only 540fJ/b is reported that employs single-ended ground-referenced signaling across high-density package interconnects. Another development describes a 1 Tb/s aggregate bandwidth across low-loss flexible cabling consuming 2.6pJ/b.

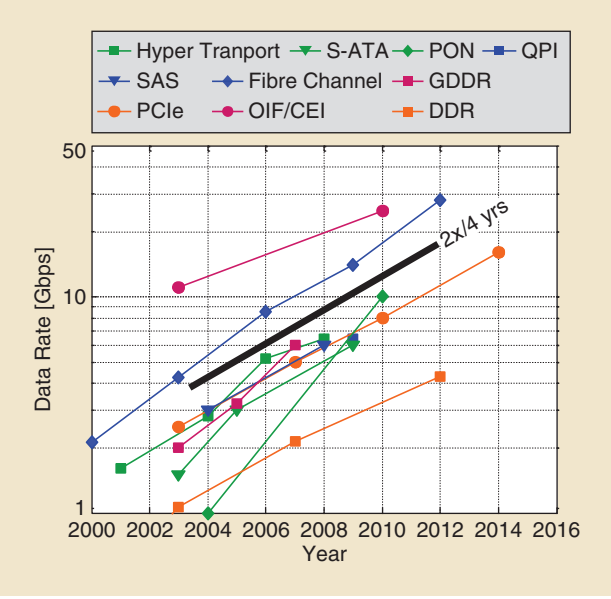

FIGURE 22: Per-pin data rate versus year for a variety of common wireline I/O standards.

Electrical Links

Some types of channels, especially those related to medium-distance electrical I/O (such as server backplanes), must support high data rates along with high loss. Others (such as DDR), must contend with increasing amounts of crosstalk in addition to channel loss. For these links, the key to scaling has been improvements in clock jitter and equalization. There are several recent examples of transceivers able to signal across 30 to 35 dB of loss at the Nyquist frequency at data rates up to 28 Gb/s. These transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. In some cases, equalization is being done in the digital domain after first converting the data signal using 5-to-6-b ADCs. Although the energy efficiency for these systems tends to be lower than in conventional equalization approaches, they enable more complex and flexible equalization techniques, as well as requiring an equalization power that may scale more gracefully. A number of CDR circuit techniques have also been developed for these high-loss transceivers, including digital CDRs that employ baud-rate sampling, over sampling, and even blind sampling techniques. At ISSCC 2013, the fastest link components reported to date, includes a 66-Gb/s three-tap DFE consuming only 46 mW without loop unrolling, and a 48-Gb/s 88-mW TX, both in standard 65-nm CMOS. Also demonstrated are other significant advances in fully-integrated high-speed transceivers: a 39.8-to-44.6-Gb/s chip set in 40-nm CMOS, and several 32-Gb/s TX and RX equalizers compensating up to 40 dB of channel loss.

Optical Links

As the bandwidth demand for traditionally electrical wireline interconnects accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnect. Relative to electrical interconnect, optics provides lower loss and potentially higher density through techniques, such as wavelength-division multiplexing. Optical components [including VCSELs, Mach-Zehnder interferometers (MZI), optical ring

(continued on p. 89)

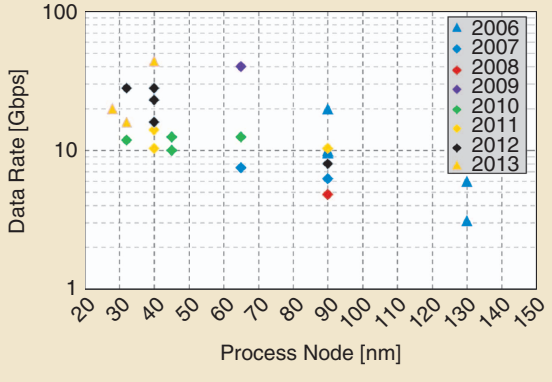

FIGURE 23: Wireline data rate versus process feature size and year.

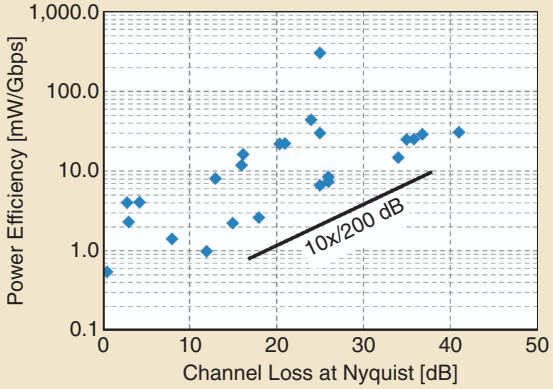

FIGURE 24: Wireline transceiver power efficiency versus channel loss.

the modulator: a power-efficient direct-charge-transfer adder with timing modification is employed, and noise-shaping enhancement is implemented by feeding the differentiated quantization noise to the input of the second integrator. The measured power dissipation is 1.1 mW, the dynamic range is 101.3 dB, the spur-free dynamic range is 112 dB, and the signal-to-noise-plus-distortion ratio is 99.3 dB. The power efficiency of this design is among the best in DSMs with high (over 15) ENOBs.

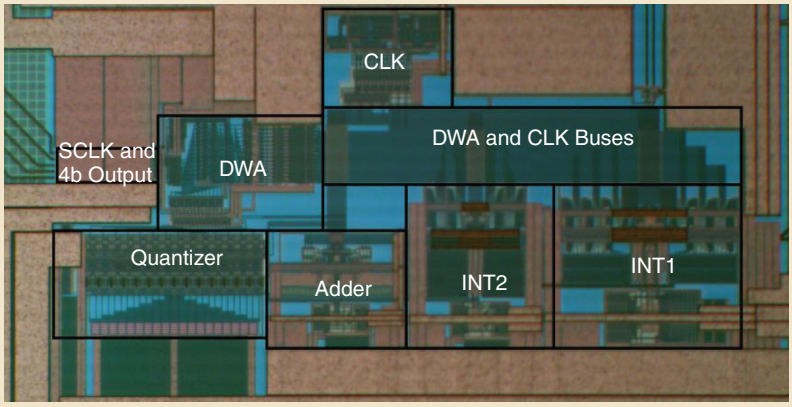

FIGURE 16: A power-efficient direct-charge-transfer adder with timing modification.

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modulators, and photodetectors] are simultaneously being developed for higher performance, lower power, and higher degrees of integration in standard CMOS processes. Circuit-design techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links requiring extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane, and chip-to-chip optical communication. ISSCC 2013 includes several examples of 25-Gb/s optical transceivers, employing an RX that consumes only 4.9pJ/b. As well, ISSCC 2013 highlights significant advances in silicon photonic integration, including a 20-Gb/s driver and associated silicon photonic MZI, and a 2.5-Gb/s driver and ring modulator designed and fabricated in a standard CMOS process.

Overall, the continuing scaling of the I/O bandwidth is essential for the industry, yet extremely challenging. Innovations that provide higher performance and lower power will continue to be made to sustain these goals. Advances in circuit architecture, interconnect topologies, and transistor scaling are, together, changing how I/O will develop over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2013.

Summary

The developments reported at ISSCC 2013 continue to present breakthroughs in the broad domain of solid-state circuits and systems. In this rich environment, presentations at ISSCC characteristically predict the ways in which electronics techniques will fulfill the present and future needs of society. In this role, ISSCC continues to present a road map of things to come, both in the immediate future and in the longer term.

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