Through the Looking Glass Continued (III)

Update to Trends in Solid-State Circuits and Systems from ISSCC 2014

A two-part article, "Through the Looking Glass II" was published last year (in the Winter 2013 and Spring 2013 issues of *IEEE Solid-State Circuits Magazine*) to discuss the trends in solid-state circuits and systems based on papers selected by the program subcommittees of IEEE International Solid-State Circuits Conference (ISSCC) 2013. This article highlights additions to those trends based on technical papers that are selected to be presented at ISSCC 2014.

ISSCC continues to be the premier forum in which industry and academic experts present and discuss the latest innovations in the world of solid-state circuits. The ISSCC International Technical Program Committee is divided into ten subject areas: analog; data converters; energy-efficient digital; high-performance digital; imagers, microelectromechanical systems (MEMS), medical, and displays (IMMD); memory; radio frequency (RF); technology directions (TD); wireless; and wireline. Each year, each subcommittee updates its view of progress in its area of specialty, based on papers to be presented at the upcoming ISSCC. Their complete compilation of trends for ISSCC 2014 are available for download at www.isscc.org. The following summary provides an overview of some of the changes seen this year.

Analog (Power Converters)

Analog circuits serve as bridges between the digital computing world and the analog real world. But digital circuits such as microprocessors drive the market; thus, semiconductor technology has been optimized relentlessly over the past 40 years to reduce the size, cost, and power consumption of digital circuits. These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate the full integration of analog and digital circuits together in our most modern digital semiconductor technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, dc-dc voltage converters are embedded alongside the digital circuitry, driving research into the delivery of locally regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are captured by movement towards the top-right in Figure 1, including two representative publications in ISSCC 2014.

Data Converters

Data converters are specialized analog circuits that link the information present in the analog real world with the processing that occurs in the digital computing world. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be the dominant drivers for innovation, as

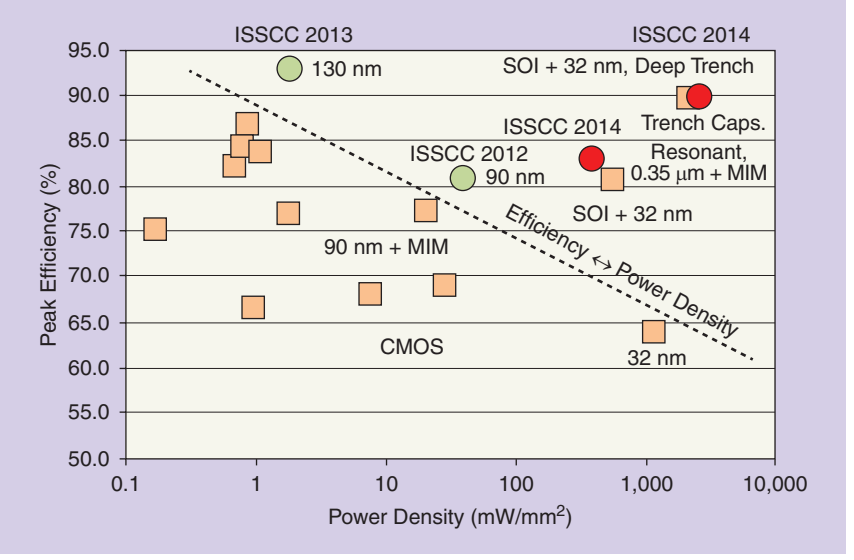

FIGURE 1: A comparison of integrated switched-capacitor power converters showing peak efficiency versus power density. Recent advances achieve much higher power density without sacrificing efficiency (see the top right).

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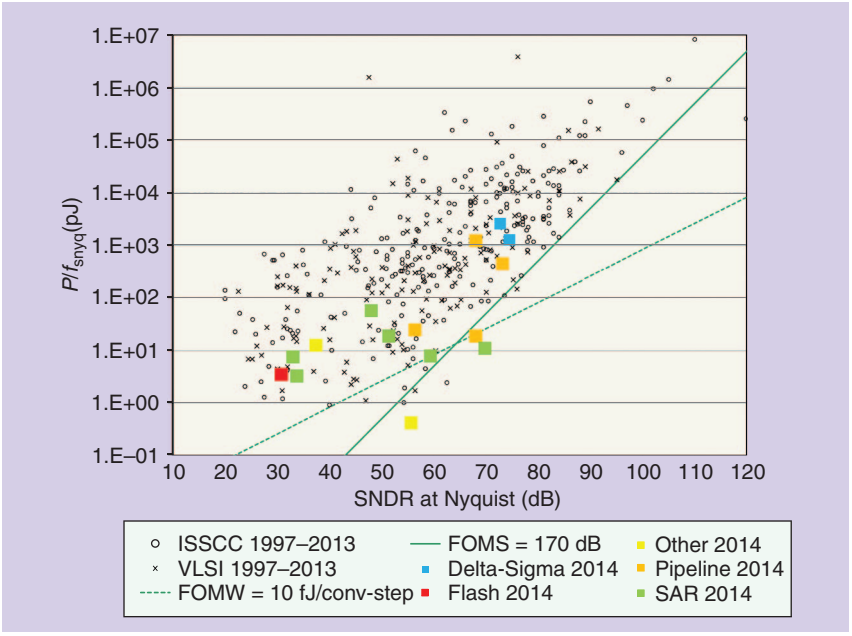

FIGURE 2: A survey of ADC power efficiency expressed as power dissipated relative to the effective Nyquist rate as a function of SNDR. New papers from ISSCC 2014 are highlighted.

evidenced by the data converters to be presented at ISSCC 2014. Figure 2 is a survey of ADC power efficiency expressed as power dissipated relative to the effective Nyquist rate as a function of signal-to-noise and distortion ratio (SNDR). Figure 3 shows energy per conversion step versus the Nyquist sampling rate. Figure 4 plots achieved bandwidth as a function of SNDR. Sampling jitter and aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Just as in past years, in 2014, we see many examples setting a new standard in these metrics, utilizing several different converter architectures.

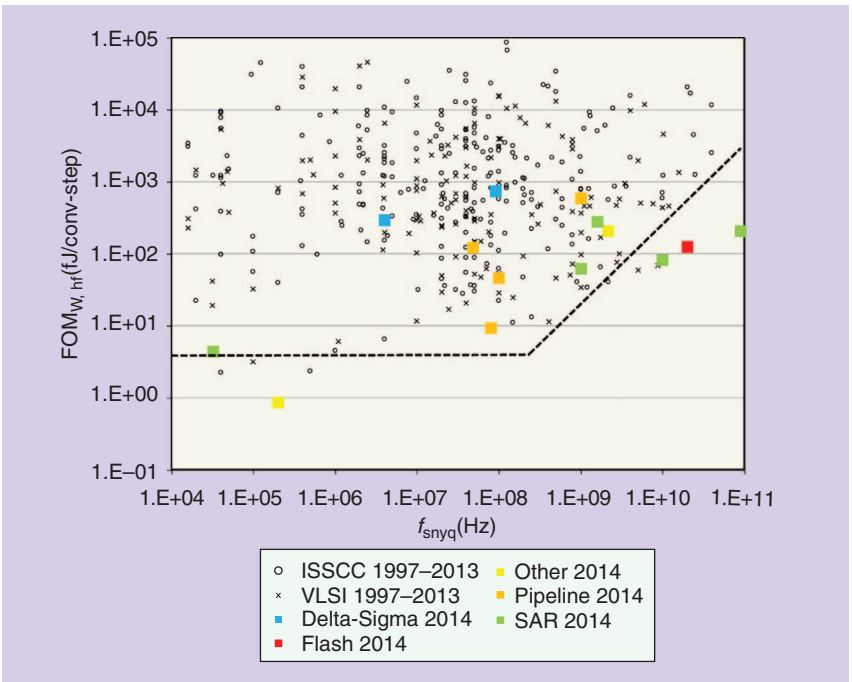

FIGURE 3: The energy per conversion step versus the Nyquist sampling rate. New papers from ISSCC 2014 are highlighted.

Energy-Efficient Digital and Wireless (Smartphone and Wireless Trends)

Figure 5 illustrates the major trends in energy efficiency of digital circuits for smartphones and tablets. A new trend for 2014 is the introduction of smartphone application processors that support wide quad extended graphics array (WQXGA) displays that have a resolution of 3,200 × 1,600 in a 16:9 aspect ratio with as much as 2× increase in computational capacity from last year. Apart from this, the trends in wireless connectivity include the growth of cellular wireless standards such as long-term evolution (LTE), with multiple frequency bands, a wide range of channel bandwidths, and various duplexing and diversity schemes, as well as new features, such as carrier aggregation. In addition, WLAN data rates are increasing exponentially. At ISSCC 2014, a 60-GHz carrier commercial CMOS chip set achieves 4.6 Gb/s over 10-m links, while CMOS front-end solutions reach 28 Gb/s for proximity wireless communication.

High-Performance Digital (Processor Milestones)

The relentless march of process technology brings increasing integration and energy-efficient performance to enterprise and cloud servers.

ISSCC 2014 features include:

- IBM 12-core, 96-thread POWER8 processor in 22-nm SOI, with 96 MB of eDRAM shared L3 cache, all employing 4.2-B transistors, and offers up to 2.5× higher socket performance over its 32 nm POWER7+ predecessor
- Intel 15-core, 30-thread next-generation Xeon server processor in 22-nm trigate technology with 37.5 MB shared SRAM L3 cache integrates 4.31-B transistors
- Intel Haswell processor in a 22-nm trigate process introduces a 128-MB multichip package eDRAM L4 cache to boost integrated graphics performance.

Milestones reached at ISSCC 2014 include the crossing of the 4.3 billion mark in number of transistors and the 100 MB mark in cache size illustrated in Figures 6 and 7, respectively.

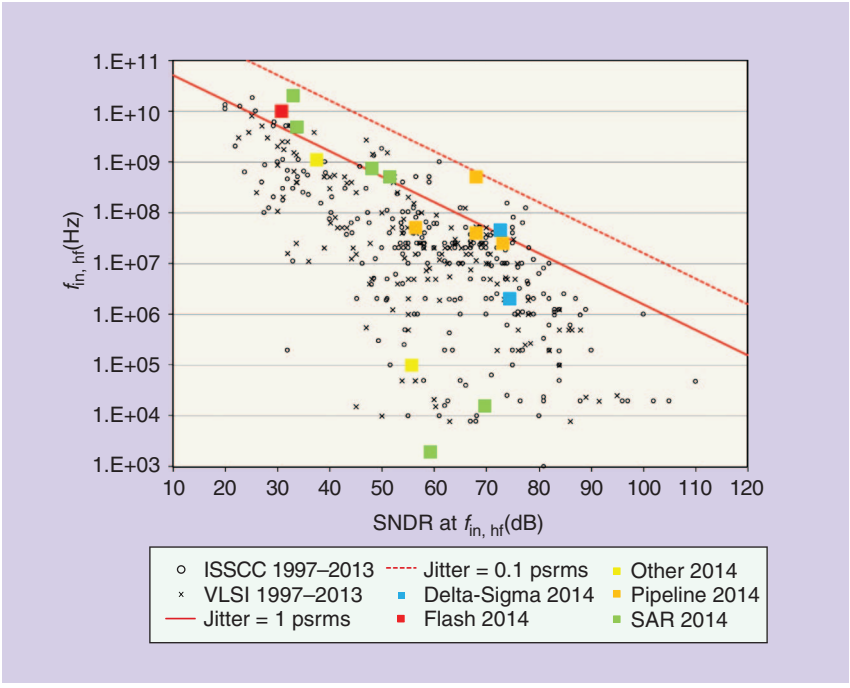

FIGURE 4: Bandwidth as a function of SNDR. New papers from ISSCC 2014 are highlighted, including one high-speed Flash and two high-speed SAR data converters.

Memory

In memory systems, we continue to see progressive scaling in embedded SRAM, DRAM, and floating-gate-based flash for very broad applications. Some state-of-the-art developments from ISSCC 2014 include:

- 1-Gb eDRAM using a 22-nm trigate logic process and capable of being clocked at 2 GHz
- 128-Gb 2-b-per-cell NAND-Flash design using three-dimensional cell technology with 24-WL stacked layers
- 128-Gb 2 b-per-cell NAND-Flash design using 16-nm planar cell technology
- 128-Mb SRAM designed in 14-nm FinFet CMOS using a 6T bitcell with V_{min}-enhancement techniques
- embedded ReRAM in 28-nm capable of working down to 270 mV
- 1-Gb eight-channel 128 GB/s high-bandwidth memory (HBM) DRAM
- 3.2-Gb/s/pin 8-Gb 1.0-V LPDDR4 SDRAM with an integrated ECC engine.

Milestones reached at ISSCC 2014 for SRAM bit-cell size, DRAM bandwidth, and NAND-flash-memory density are shown in Figures 8–10, respectively.

Radio Frequency

At ISSCC 2014, RF techniques are extending both in innovation and integration level, across the RF bands from a few gigahertz to above 500 GHz. For the first time, wireless receivers are being implemented in 28-nm CMOS. At ISSCC 2014, several distinct trends are apparent. Increasing levels of integration are seen in all areas of RF design, from cellular and wireless sensors to mm-wave and imaging systems extending to the terahertz

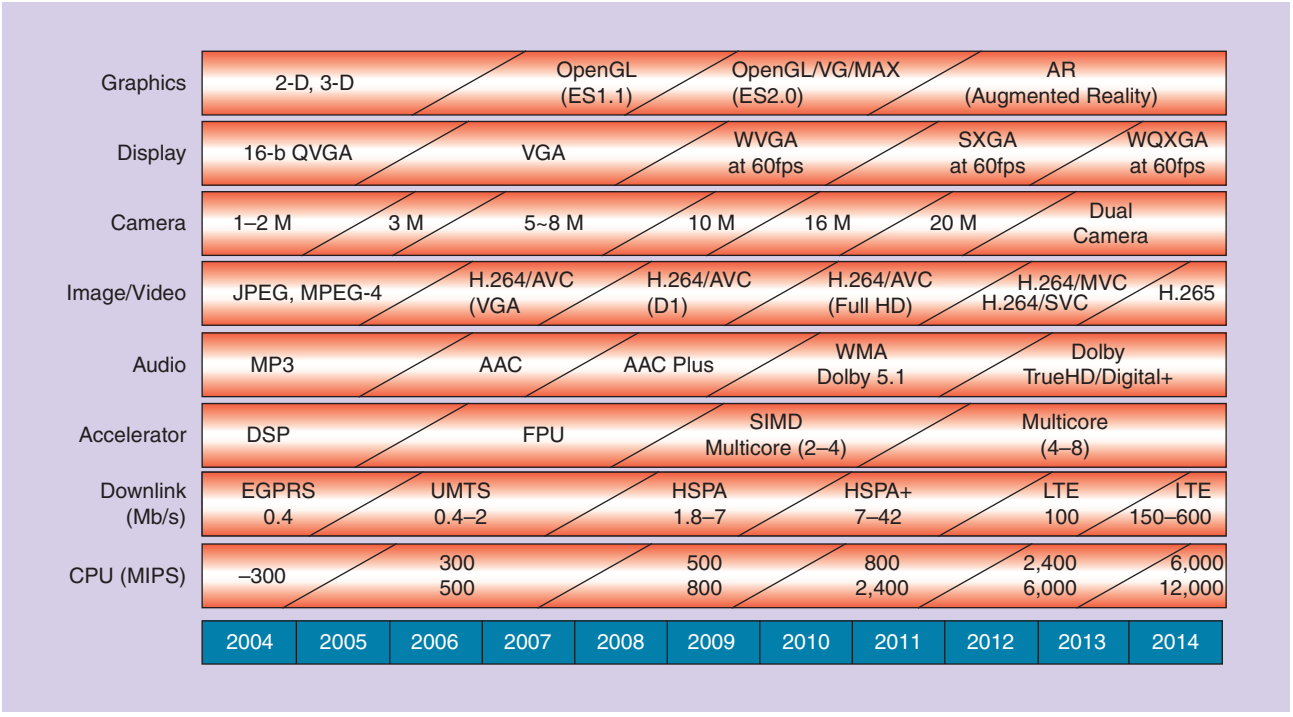

FIGURE 5: Smartphone application processor trends.

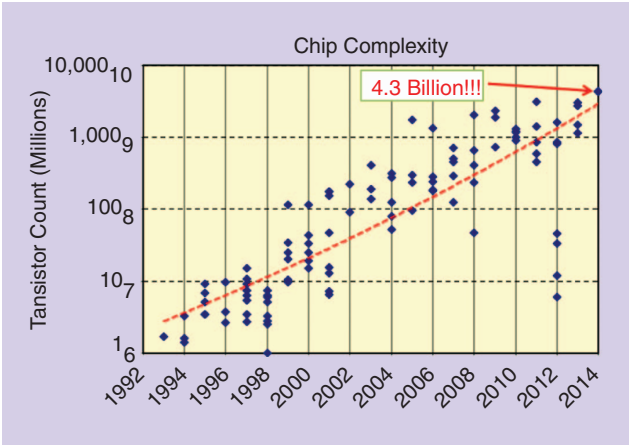

FIGURE 6: The transistor count.

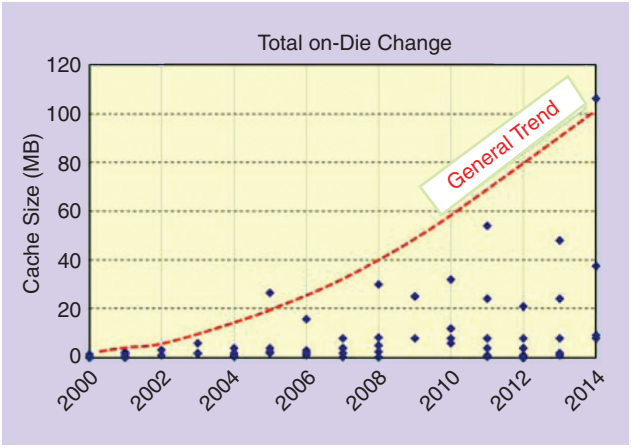

FIGURE 7: The on-die cache size.

region. While there are several other exemplary accomplishments in RF circuits, it is noteworthy that the output power level at sub-mm wave radio frequencies has reached record levels as illustrated by the 130-nm SiGe source shown in Figure 11.

Wireline

Wireline-focused circuits have been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. This year, at ISSCC 2014, notable accomplishments include:

- the lowest-reported power long-range 28-Gb/s transceiver, achieving 20 pJ/b and two DFE receivers operating at 0.25 pJ/b
- a new coded signaling scheme that transmits 8 b over eight wires, enabling 96 Gb/s at 4.3 pJ/b/wire over 15-dB loss channels
- an electrical-interconnected 28-Gb/s transceiver operating over a 30-dB loss channel
- a 60-Gb/s transmitter, the highest transmit data-rate reported to date
- an optical interconnect that uses a two-dimensional (12 × 5) optical array achieving an aggregate data-rate of 600 Gb/s.

IMMD and TD (Novel Circuits and Systems)

A breakthrough concept in biomedical electronics has been the identification of the need for "anytime and anywhere" human-monitoring systems using wearable/implantable devices.

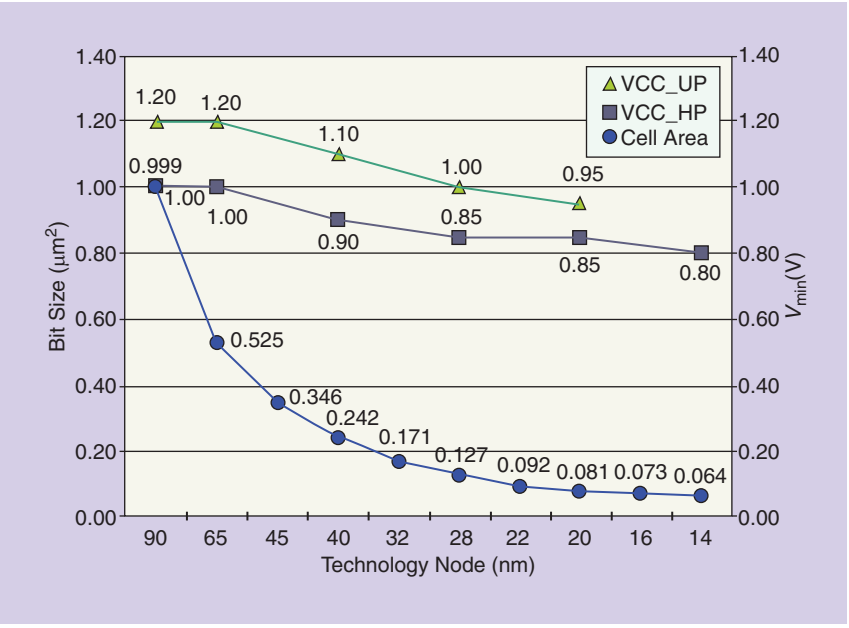

FIGURE 8: SRAM bit-cell and minimum-supply-voltage scaling.

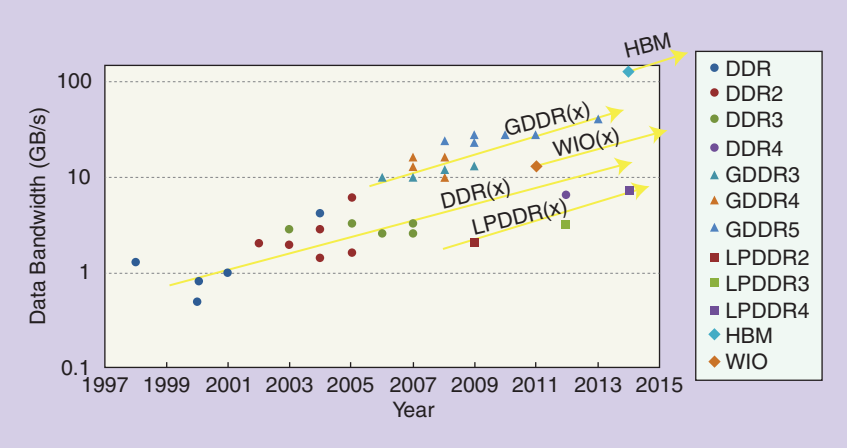

FIGURE 9: DRAM bandwidth.

Such devices will enable improved of quality of life through self-health checks, remote examination by physicians, and continuous monitoring for acute diseases. Key technologies for such system include:

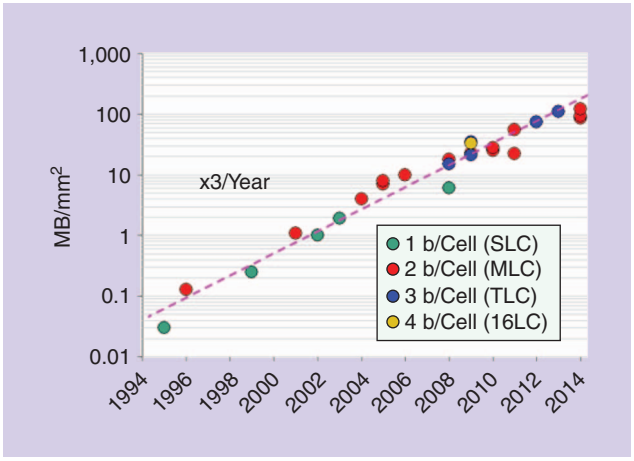

FIGURE 10: NAND flash memory density.

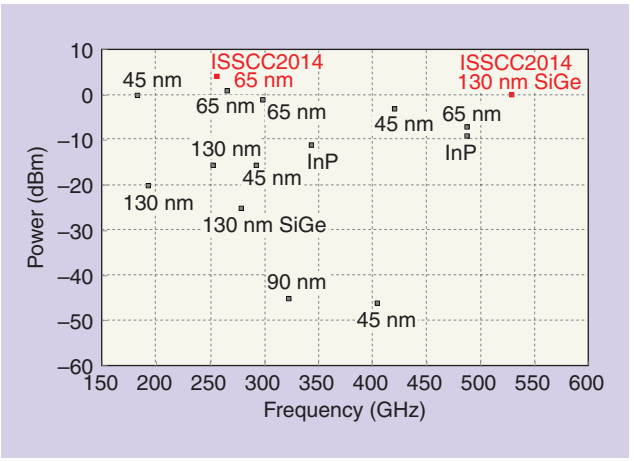

FIGURE 11: Output power versus frequency for mm-wave and sub-mm-wave sources.

- small-footprint devices and flexible electronics to improve the comfort of wearable devices
- high-accuracy monitoring devices
- low-power monitoring and communication systems for long-duration autonomous operation.

In the past few decades, many new applications such as mobile devices and the Internet have driven the growth of high-performance computing systems. The next big application drivers will include cloud computing, big data, and the Internet of Things, which will require increasing performance demands on the backbone of the infrastructure. Important trends and future challenges requiring system innovation include

- satisfying performance demands that increase at an exponential rate
- containing the power dissipated in data centers whose electricity and cooling costs are skyrocketing.

The CMOS-image-sensor business is one of the fastest growing segments of the semiconductor industry. Key applications include cell phone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-cinema cameras, and gaming. The resolution and miniaturization races are ongoing, and while the performance requirements stay constant, pixel size continues to scale down. Images over 40 MP are commercially available. A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Backside illumination is now a mainstream technology for mobile imaging. Wafer stacking of the image array on a CMOS image signal processor will become common.

MEMS has now enabled the world's smallest 32-kHz ultra-low-power timing sources. Low-power timing has normally been supplied by quartz tuning forks, but miniaturization of that technology is proceeding slowly. MEMS oscillators are available a 1.5×0.8 mm^2 die, in a chip-scale package, and consume under 1 µA supply current. Temperature compensation provides three parts per million accuracy over temperature.

Conclusion

In this article, we have highlighted some of the trends in solid-state circuits and systems identified by an international group of over 180 experts that serve as members of the ISSCC Technical Program Committee. Their analysis is based on the review and analysis of papers that were selected for presentation at ISSCC 2014, in the light of the collective expertise represented by each subcommittee's membership. A more complete trend analysis is available for download at www.isscc.org.

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