

ENGINEERING ASPECTS OF MULTI-VALUED LOGIC SYSTEMS

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Introduction

We live in a binary world of computers, accepting the inevitability of dealing with strings of 0's and 1's, simply because this is dictated by the two-valued nature of switching primitives which make up the machines. Yet there is little doubt that most of us would prefer decimal machines if they were available. Present technology is unlikely to result in such machines in the near future, at least not the kind where basic building blocks are inherently 10-valued. However, this does not mean that the binary approach must continue to be the only alternative. Considerable advantages may be gained by considering higher-radix systems, even if decimal schemes are presently out of reach.

Symmetric number representation offers attractive possibilities, as demonstrated by several designs of ternary arithmetic units.^{4,5,11,14,33} For example, if ternary digits are coded as +1, 0, and -1, then sign conversion becomes trivial, since negative numbers are obtained merely by inverting each digit. Addition and subtraction are carried out without regard to the signs, which is equivalent to the binary twos complement techniques. Special "rounding off" schemes are unnecessary, since a number is rounded off to k most significant digits by simple truncation of the remaining digits.

Perhaps the most significant immediate benefits of higher-radix approaches lie in their potential for reduction of the wiring complexity. Integrated circuit technology has placed a premium on the cost of interconnections. Thus, the number of wires needed in a given network often determines the feasibility of its practical implementation. It is apparent that the wiring complexity diminishes with increasing radices, although the actual savings effect is not easy to assess without detailed analysis of large practical circuits. One such investigation showed that ternary parallel multipliers require fewer than two-thirds of the interconnections necessary in equivalent binary configurations.³⁹ There also exists a corresponding reduction in the number of gates (approximately 20%), but this is offset by the higher cost of individual ternary gates.

Practical feasibility of multi-valued digital systems clearly depends upon two critical factors, namely, the availability of reliable electronic implementations of the basic switching primitives and the adequacy of synthesis techniques. The latter have been a frequent subject in recent technical literature.^{1,12,31,35,37,40,41} As a result, it has become apparent that the number of useful (and manageable) basic functions is not large. Some of them are very easy to implement – e.g., the sum and product functions

$$x + y = MAX(x,y)$$

 $x \cdot y = MIN(x,y)$

where $x,y \in Q$ and $Q = \{0,1,2,\ldots, R-1\}$ in an R-valued system. Others require more complex circuits, as is the case with the "literal" gates^{1,12,37}

$$a_x b = R-1$$
 if $a \le x \le b$; $a, b \in Q$
= 0 otherwise,

"complement" gates (also called the diametrical inversion)

$$\overline{\mathbf{x}} = \mathbf{R} \cdot \mathbf{1} \cdot \mathbf{x}$$
,

and the "cycling" gates4,7

$$x^{y} = (x+y) \mod R$$
.

In the typical spirit of most new areas of research, the volume and intensity of the theoretical work in multivalued switching systems has greatly outdistanced the physical implementation efforts. In spite of this, there have been a number of interesting reports on electronic realizations of the basic circuits.^{3,6,8-10,13,14,17-21,23-29,31,36,38} The aim of this paper is to give an overview of these designs, particularly from the performance point of view.

Some of the early attempts concentrated on the development of basic devices which were essentially non-binary in nature. Such was the case of the Rutz transistor,²² the parametron,³² multi-aperture square-loop ferrite devices, etc.^{2,20} Magnetic cores received special attention^{20,30} and even became a key building block in the SETUN' computer.² Eventually these attempts gave way to the approach of utilizing readily available binary components for construction of circuits which exhibit multi-valued behavior.

An essential - and probably the most challenging - implementation task is the design of R-stable circuits (i.e., circuits having R stable states). Their application as a basic storage device for building of registers, shift-registers, counters, etc., is obvious. Moreover, they may be used for signal level restoring, which is often a problem in multi-

valued circuits due to more critical noise tolerances and possible signal degradation in simple gates. Thus, we will concentrate our discussion on R-stable circuits, since they are certainly representative of the general class of R-valued elements and space does not permit consideration of all others.

The next section deals with the voltage-mode designs; the section following it describes more recent current-mode circuits.

Voltage-Mode Circuits

It is logical that the challenge of higher-base storage elements was first met with solutions for radix 3. Large numbers of these abound in a variety of technologies including bipolar junction and field effect transistors. However, the majority of these, with a few important exceptions, make some simple use of the inherent \pm symmetry of radix 3 and are not easily extended to higher bases. Examples of this specialty are the designs by Melnikov (p. 211),²⁰ by Mine et al,²³ and by Braddock et al.³ Here it is arranged that the two transistors of a binary flip-flop pair maintain a third state in which both are either on^{20,23} or off.³ Additional nonlinear components, such as diodes or a transistor, are necessary.

Figure 1 from Mine et al²³ illustrates a variety of points of interest. The basic circuit consists of two transistors (T_1, T_2) cross-coupled by non-linear diode elements $(D_1 - D_4)$. Each transistor can assume three states: ON/OFF driven through diodes by the opposite device on "partially-ON" under control of a negative feedback loop employing the associated 2K and 8K resistors. While both transistors



Figure 1. 3-flop with capacitor storage gating

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Figure 2. 3-stable





Figure 3. 3-flop using COSMOS-resistor technology

are in the latter partially-ON state, corresponding points in each half of the circuit are at the same potential. Thus, the coupling diodes are held below their conducting threshold, and the positive feedback necessary to establish the ON/OFF states is disconnected.

The design, though remarkable for all that it does, is quite sensitive to component variability. The current gain of the transistors, for example, is highly constrained. The problems of this design may be generally relieved by including additional transistors to provide current gain. With additional transistors, however, other approaches are also possible.

Alternative base three designs make inherent use of two binary flip-flops and a circuit connection which automatically suppresses one of the four available states.^{10,19} As in Hurst,¹⁹ an analog adder is often incorporated to provide a three-valued output signal rather than the multiwire binary-coded outputs naturally available.

The design by Smith¹⁰ shown in Figure 2 incorporates a positive and negative flip-flop, and a common signal connection which eliminates the fourth state and provides a single-wire three-valued output. This design, which is also amenable to COSMOS technology, can be extended to base five by incorporating a total of four simple binary flip-flops sharing one output load.

The zero state in the designs patterned after Figure 2 and others^{13,21} is particularly weak, with a high source resistance. For local use within logic, this is often not of consequence. However, in a system application, capacitive loading will adversely affect flip-flop gating time.

Other more general approaches to storage element design exist which are inherently extendable to bases higher than three. An historically important one of these^{27,29} amenable to present digital technology is a one-of-R circuit for which R two-valued outputs exist, only one of which differs from the rest. The basic one-of-R or R-flop may be formed from R (R-1)-input NORs interconnected so that each NOR has an input from all others. The traditional binary flip-flop is, of course, the special case for R=2, for which gating is especially trivial using additional NOR inputs. For R>2 the situation is more complex since oneof-R outputs (not inputs) must be selected. The one-of-R store or R-flop, though conceptually extendable to high bases, offers several practical problems related to the inefficient binary coding of its inputs and outputs. For these reasons the R-flop, though inherently useful in guaranteeing activation of one of many naturally exclusive events, has no real place in multi-valued logic except as an interface element where its inherent one-of-many input/ output property may be a virtue.

Another class of base-R storage elements which appear to hold promise are those formed by feedback cascades of fundamental base-R unary elements. A particular case applicable to base three is described by Hallworth and Heath,¹³ where two diametrical inverters are cascaded. The design by Mine et al²³ illustrated in Figure 1, though not described in these terms by them, is also of the twoinverter cascade type, as is the design by Kaniel.²¹ Kaniel combines a MIN gate with each inverter to form a "NAND" using COSMOS-resistor technology (see Figure 3a). Gating is thus naturally included. A simple cross-coupled arrangement of two "NAND" circuits results in a somewhat awkward three-flop. However, it may be improved with additional gating³⁴ as shown in Figure 3b, with the resultant truth table given in Figure 3c.

A cascade of R cycling gates in a feedback loop forms a storage element in any base R. Porat²⁷ shows an example for base three. An apparent difficulty with this approach is the likely cost of high-performance cycling gates, with guaranteed level-restoring and low-impedance outputs. Within the storage loop cascade, however, conditions are considerably less than general. The existence of only a few highly stabilized signal values, typically the extreme signals 0 and R-1, coupled with controlled transfer properties of the gates, ensures adequate operation. The design by Porat shown in Figure 4 illustrates this fact. The upper and lower levels of his signals are established by power supplies at the output of each cycling gate, while the middle level is a result of diode level shifts from the input. Even though many of the cycling gates in a storage loop may exhibit gains ≤ 1 , it suffices that the gains be somewhat controlled and that at least one level-restoring element exists in the loop.

The last approach we will consider is the nonlinear resistor or stepped-load-resistor (SLR) concept.^{36,30} The idea is an old and fundamental one, first introduced by Henle in 1955.¹⁸ A similar concept has been exploited in the use of tunnel diodes in multi-valued storage, where a series string of tunnel diodes supplied by a common current exhibits a variety of voltage states.¹⁷ Though usually R











Figure 5. A simple step load resistor

states require R-1 tunnel diodes, Salter has shown a scheme in which a single tunnel diode exhibits three terminal voltage states.²⁸

A simple SLR²⁰ for R=5 is shown in Figure 5. The SLR is characterized by the fact that its input terminal current is quantized at multiples of the reference current I_0 . Though the input voltage varies by a large fraction of one diode drop, the current supplied is nearly constant at KI₀. In use the SLR may be supplied by a voltage-to-current converter whose voltage is fed back from the voltage across the step resistor. The effect is such as to establish a sequence of stable output states where the linear source and nonlinear load lines intersect.

This simple scheme suffers from the accumulation of diode resistances at high R. With current IC technology it should be relatively easy to produce related designs for bases up to nine in which the step sizes are more equal than in this simple case.

Current-Mode Circuits

Perhaps the most severe limitation of most of the approaches discussed above is their inherent lack of generality - i.e., extendability to higher bases. This situation has improved with the more recently published current mode circuits.^{6-9,24}

Such circuits employ the fundamental current-switching principle, where the direction of the current flowing through each current switch is determined by the input signal excitation. These concepts are widely applicable and presently form the basis of the best threshold logic implementations.^{15,16}

As a representative example of the possibilities of utilizing current-mode techniques for implementation of multivalued storage elements, we will look at the particular case of multi-threshold multi-valued circuits.^{6,7} Consider an R-valued M-threshold circuit which implements the R-valued function

$$F(x_1, x_2, ..., x_n) = H(e)$$

where $e = \sum_{i=1}^{n} a_i x_i \equiv excitation$

 $a_i \equiv$ weight associated with input x_i

 $H(e) \equiv$ transfer characteristic (i.e. the output value when the excitation is e)

$$F, H, x_i \in \{0, 1, ..., R-1\}$$

The circuit may have at most M thresholds, such that

$$\mathbf{M} \leq \mathbf{e}_{\max} \leq (\mathbf{R} \cdot \mathbf{1}) \sum_{i=1}^{n} |\mathbf{a}_{i}|.$$

Note that H(e) may be arbitrarily specified (within the above constraints), thus allowing a single gate implementation of a great many functions.

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Figure 6. Stair-case transfer characteristic

Since the focal point of this paper is the discussion of approaches to the design of multi-valued storage circuits, we will concentrate on the single-input MT(R) elements. In particular, a simple staircase transfer characteristic – i.e., $H(e) = x_i$, shown in Figure 6 – provides a useful means for realization of R-stable circuits. It can be implemented with circuits such as the one shown in Figure 7, which corresponds to the specific case where R=5. In this circuit the input excitation current is reproduced through a summing resistor R_s by the current-mirror $Q_1 - Q_2$. The resultant voltage at node S is compared with the threshold voltages $VT_{\rm Tm}$ (m=1, . . . , 4) by means of the differential pairs of $Q_3 - Q_4, \ldots, Q_9 - Q_{10}$ (threshold voltages are equally spaced). The bias current of the mth differential pair flows

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Figure 7. 5-valued RT(M) circuit for Figure 6



Figure 8. R-stable circuit

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through Q_{16} if $V_s > V_{Tm}$. Finally, the current in Q_{16} is reproduced as the output through the current-mirror Q_{16} - Q_{17} .

This circuit (let it be denoted by E) becomes R-stable if it is connected in a loop with unity feedback. However, in order to obtain usable storage elements, it is necessary to provide a triggering mechanism, which may readily be done as indicated in Figure 8. Both gating functions (MIN, MAX) can be implemented as simple diode gates, since any signal-level degradation is corrected by the level-restoring characteristic of the E element. Holding the Reset terminal at the "R-1" signal level, the R-stable retains the highest previously-encountered signal at the Set input. The R-stable is reset by the 0 level at the Reset input.



Figure 9. Master-slave R-flop

It should be noted that two R-stables can be combined into a "master-slave" R-flop, using the single-phase clock scheme of Figure 9. The two-valued clock is high when c = R-1 ($\bar{c} = 0$) and low when c = 0 ($\bar{c} = R-1$).

Prototype shift-register circuits consisting of such fivevalued master-slave R-flops have been operated reliably at speeds of 3 MHz.⁶

Conclusion

Despite relatively little effort put into design of electronic circuits for multi-valued logic, there has been an encouraging evolutionary trend towards more practical realizations.

Present implementations suffer greatly from insufficient utilization of integrated circuit techniques. Stray capacitance in complex discrete circuits leads to slow operating characteristics. Additional components and small size available with integrated circuit technology will inevitably lead to much improved speed performance.

Once the speed problems are overcome, the natural advantages of multi-valued techniques in the reduction of wiring complexity will assert themselves. ■



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