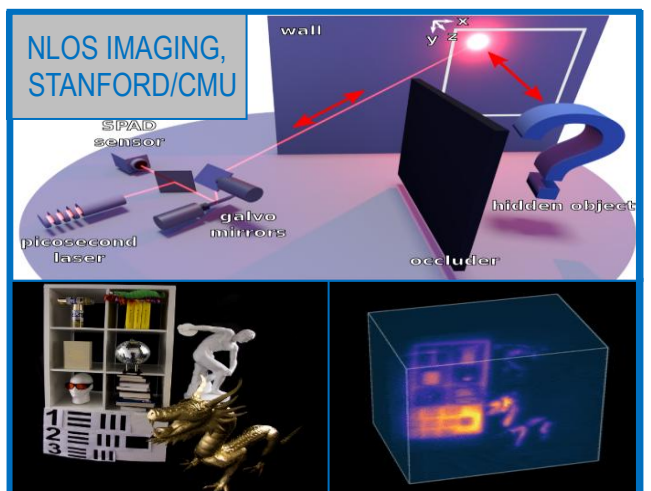
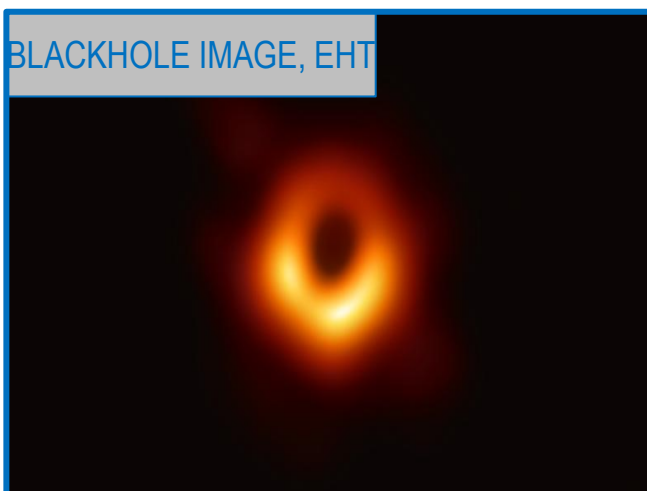
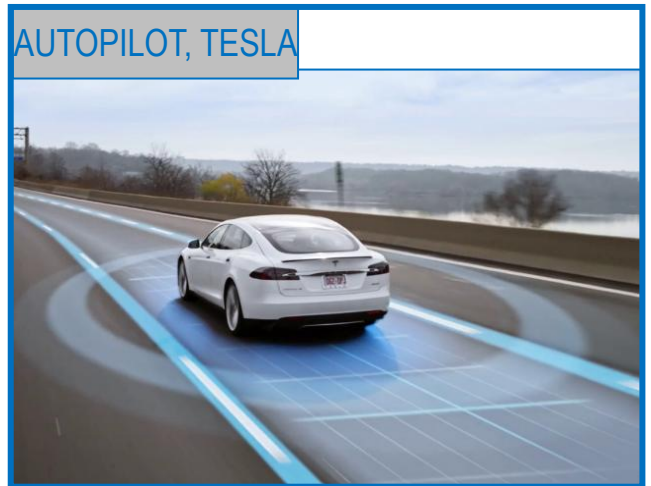
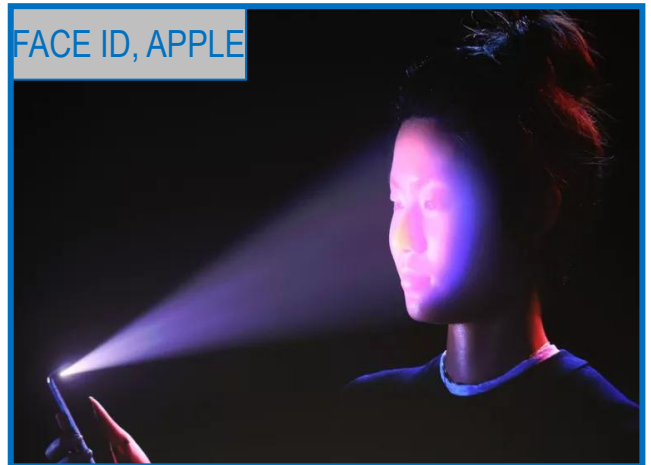


<b>Project proposed by: Supervisor:</b>	Intelligent Sensory Microsystems Laboratory, ECE, U of T Prof. Roman Genov
<b>Project title:</b>	Mixed-Signal IC design for the Next-Generation Computational Cameras (2 Positions)
<b>Project description:</b>	<p>At Intelligent Sensory Microsystems Lab, our team is leading the development of a new family of coded-pixel cameras with never-before-seen capabilities, like the ability to sort incoming photons based on their properties. These cameras target the explosively growing space of new computer vision applications such as 3D imaging for robotic navigation of drones and self-driving cars in harsh environments; and next-generation information-rich user interfaces through face / gesture analysis. Such applications often require programmability, or coding, of the camera exposure at the individual-pixel level.</p> <p>Unlike conventional cameras, which record all light incident onto a pixel, our coded-exposure-pixel (CEP) cameras can be programmed to selectively sort the light based on its path or time of travel. In conjunction with a concurrently coded illumination, this enables a wide range of previously unattainable video capabilities such as seeing against the sun, seeing through the skin, or seeing behind an object/around the corner.</p> <p><b>Related videos:</b></p> <ol style="list-style-type: none"> <li>1. <a href="https://youtu.be/8_WJb06h5E">https://youtu.be/8_WJb06h5E</a></li> <li>2. <a href="https://www.dropbox.com/s/4q60jhp9vfmi4qy/1717-suppl.mp4?dl=0">https://www.dropbox.com/s/4q60jhp9vfmi4qy/1717-suppl.mp4?dl=0</a></li> </ol> <p><b>Undergraduate and Master Students will actively participate in designing key mixed-signal integrated circuit (IC) building blocks</b>—mainly focused on analog-to-digital converters (ADCs) and phase-locked loops (PLLs)—for next-generation computational camera systems. Specifically, the work will focus on developing column-parallel ADCs for high-speed, high SNR sensor readout, PLL (or DLL) circuits for precise clock delay matching, jitter reduction, and high-frequency clock generation to support on-chip ADCs and digital signal processing. We will also aim to search possibilities of other AMS IC blocks, such as PHY, DAC, and so on.</p> <p><b>The ideal candidates are expected to have the following qualifications:</b></p> <ul style="list-style-type: none"> <li>● Concrete understanding in analog/mixed-signal (AMS) IC design (Must have taken ECE412H, ECE430H or equivalent until 2026 Winter)</li> <li>● Experience in design, simulation, and post-extraction of AMS IC blocks using the Cadence Virtuoso environment.</li> <li>● Experience in reading and analyzing AMS IC related publications</li> <li>● cGPA higher than 3.5 out of 4.0, with excellence in AMS IC design related courses</li> <li>● Self-driven attitude, pre-emptive in finding solutions, and high interest in AMS IC design</li> </ul>
<b>Contact persons:</b>	Kindly send your email to Jangwon Suh ( <a href="mailto:j.suh@mail.utoronto.ca">j.suh@mail.utoronto.ca</a> ) and copy to Prof. Roman Genov ( <a href="mailto:roman@eecg.utoronto.ca">roman@eecg.utoronto.ca</a> ). Please include your cGPA, study program, and related accomplished projects in the email along with your attached updated CV and all your official transcripts.

## Computational Imaging Applications



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