Roman Genov

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Research Interests

Analog and digital VLSI circuits, systems and algorithms for parallel signal processing and neural computation with application to pattern recognition, sound classification, autonomous systems design and low-power instrumentation.

Education

Ph.D. Candidate, Electrical and Computer Engineering, **The Johns Hopkins University**, Baltimore, MD, 2002.
Dissertation: Massively-Parallel Mixed-Signal VLSI Kernel Machines.
Advisor: Dr. Gert Cauwenberghs

Visiting Student, Center for Biological and Computational Learning, **Massachusetts Institute of Technology**, Cambridge, MA, 1/99-8/99.

M.S., Electrical and Computer Engineering, **The Johns Hopkins University**, Baltimore, MD, 1998.
GPA 4.00/4.00

B.S. with Highest Honors, Electrical Engineering, **Rochester Institute of Technology**, Rochester, NY, 1996.
GPA 4.00/4.00, Rank in class - 1/316

Experience

Academic and Industrial

Research Assistant, Adaptive Microsystems Laboratory, Department of Electrical and Computer Engineering, **The Johns Hopkins University**, Baltimore, MD, 9/96-present.
Massively parallel mixed-signal VLSI processor implementing a Support Vector Machine (SVM) for high-dimensional data classification. Pattern recognition and acoustic classification systems utilizing SVM parallel processing chips. Low-power charge-mode parallel A/D converters, delta-sigma converters, and high-speed, high-resolution, digitally calibrated pipelined algorithmic A/D converters (with **Northrop Grumman Corporation**, Baltimore, MD). Reinforcement learning algorithms for intelligent robot navigation. Low-power analog and digital VLSI chips for high-performance instrumentation. Xilinx FPGA-based PCI bus interfaces for video and image processing microchips. Linux and Win2000 C++ device drivers, and Matlab interfaces.

Visiting Researcher, Autonomous Systems Laboratory, **Swiss Federal Institute of Technology**, Lausanne, Switzerland, 6/98-7/98.
Developed Q-learning-based algorithms for mobile micro-robot navigation. Investigated their mapping onto VLSI architectures.

Design engineer CO-OP, Advanced Development Team of the Color Digital Imaging Systems Division, **Xerox Corporation**, Webster, NY, 3/96-8/96.
Hardware-software co-design with Verilog, Xilinx tools, PALASM. Design and development of electrical and computer systems for new generation color copiers.

Technical Director Assistant, Chesapeake Design Center, **Atmel Corporation**, Columbia, MD, 6/95-12/95.
Design and simulation of digital cells for ASICs, and design of layouts for different ASIC implementations. Created a Perl extraction tool to automate the process of getting data from HSPICE output files into a con-

densed and useful state used for creating of Verilog ASIC models. Analysis time has been reduced by 10-15 times.

Teaching

Graduate Teaching Assistant, Johns Hopkins University, Baltimore, MD.
"Digital Signal Processing," 9/97-12/97, 9/98-12/98.
"Electronic Design Laboratory," 1/98-5/98.
"Analog and Digital VLSI Systems and Architecture," 9/99-12/99, 9/2001-12/2001.
Teaching Assistant, Rochester Institute of Technology, Rochester, NY.
"Digital Systems Design," 2/95-5/95.
"C Programming," 2/96-5/96.

Awards and Honors

Best Paper Award, 5th World Multi-Conference on Systemics, Cybernetics and Informatics (SCI'2001), Roman Genov, with Gert Cauwenberghs, 2001.
Best Student Paper Award, 3rd place, IEEE Midwest Symposium on Circuits and Systems (MWSCAS'2000), Roman Genov, with Gert Cauwenberghs, 2000.
Best Presentation Award, IEEE International Joint Conference on Neural Networks (IJCNN'99), Roman Genov, with Srinadh Madhavapeddi and Gert Cauwenberghs, 1999.
Best Student Paper Contest Finalist, IEEE International Symposium on Circuits and Systems (ISCAS'99), Roman Genov, with Gert Cauwenberghs, 1999.
Rochester Institute of Technology Presidential Fellowship, 1995-96.
American Council of Teachers of Russian Fellowship, 1994-95.

Invited Presentations

"VLSI Array for Massively Parallel Kernel Computation," R. Genov, invited presentation at Workshop on Neuromorphic Engineering. Telluride, CO, July 2001.
"Q-Learning: Experiments on Microrobots," R. Genov, with S. Madhavapeddi and G. Cauwenberghs, invited presentation at Neural Information Processing Systems (NIPS'1999) workshop, Breckenridge, CO, Dec. 1998.

Activities

Society Memberships: IEEE (Institute of Electrical and Electronic Engineers) Circuits and Systems Society, Computer Society.
High-Technology Entrepreneurship Interactive Program, 1999.
Tau Beta Pi Engineering Future, Leadership and Technical Management Interactive Workshop, 1998.
IEEE JHU Chapter Treasurer, 1997.
Electrical Engineering Class President, 1991-1994.
Volleyball, Ping-Pong, Accordion.

Publications

"Charge-Mode Parallel Architecture for Matrix-Vector Multiplication," R. Genov and G. Cauwenberghs, to appear in *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing* (invited).
"Stochastic Mixed-Signal VLSI Architecture for High-Dimensional Kernel Machines," R. Genov, G. Cauwenberghs, to appear in *Advances in Neural Information Processing Systems (NIPS'2001),* Cambridge, MA: MIT Press, vol. 14, 2002.

“CID/DRAM Mixed-Signal Parallel Distributed Array Processor,” R. Genov, G. Cauwenberghs, to appear in *Proc. of 14th International IEEE ASIC/SOC Conference (ASIC/SOC’2001),* Washington, DC, 2001.

“Embedded Dynamic Memory and Charge-Mode Logic for Parallel Array Processing,” R. Genov, G. Cauwenberghs, *Proc. of the 5th World Multi-Conference on Systemics, Cybernetics and Informatics (SCI’2001),* Orlando, FL, July 22-25, 2001. **Best Paper Award.**

“Massively Parallel Inner-Product Array Processor,” R. Genov, G. Cauwenberghs, *Proc. of International Joint Conference on Neural Networks (IJCNN’2001),* Washington, DC, July 15-19, 2001.

“Analog Array Processor with Digital Resolution Enhancement and Offset Compensation,” R. Genov, G. Cauwenberghs, *Proc. of Conference on Information Sciences and Systems (CISS’2001),* Baltimore, MD, March 21-23, 2001.

“Charge-Mode Parallel Architecture for Matrix-Vector Multiplication,” R. Genov and G. Cauwenberghs, *Proc. of 43rd IEEE Midwest Symposium on Circuits and Systems (MWSCAS’2000),* Lansing, MI, Aug. 8-11, 2000. **Best Student Paper Award, 3rd place.**

“Learning to Navigate from Limited Sensory Input: Experiments with the Khepera Microrobot,” R. Genov, S. Madhavapeddi and G. Cauwenberghs, *Proc. of International Joint Conference on Neural Networks (IJCNN’99),* Washington, DC, vol. 3, pp. 2061-2064, 1999. **Best Presentation Award.**

“16-Channel Single-Chip Current-Mode Track-and-Hold Acquisition System with 100 dB Dynamic Range,” R. Genov and G. Cauwenberghs, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS’99),* Orlando, FL, vol. 6, pp. 350-353, 1999. **Best Student Paper Contest Finalist.**

Publications under Preparation

“Charge-Mode Correlated Double Sampling Comparator and Folding Circuit,” R. Genov and G. Cauwenberghs, to be submitted to *Electronics Letters.*

“Algorithmic Delta-Sigma Analog-to-Digital Converters,” G. Mulliken, F. Adil, R. Genov, and G. Cauwenberghs, to be submitted to *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing.*

“Stochastic Mixed-Signal VLSI Architecture for High-Dimensional Computational Arrays,” R. Genov, G. Cauwenberghs, to be submitted to *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing.*

“16-Channel Single-Chip Current-Mode Track-and-Hold Acquisition System with 100 dB Dynamic Range,” R. Genov and G. Cauwenberghs, to be submitted to *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing.*

“Charge-Mode Gray-Coded Folded A/D Converter,” R. Genov and G. Cauwenberghs, to be submitted to *IEEE International Symposium on Circuits and Systems (ISCAS’2002),* Phoenix, AZ, May 26-29, 2002.

“Algorithmic Delta-Sigma Analog-to-Digital Converters,” G. Mulliken, F. Adil, R. Genov, and G. Cauwenberghs, to be submitted to *IEEE International Symposium on Circuits and Systems (ISCAS’2002),* Phoenix, AZ, May 26-29, 2002.

Patents under Preparation

“Parallel Vector-Matrix Multiplier on an array of embedded Dynamic Random Access Memories (DRAM) and Charge Injection Devices (CID) and method thereof,” R. Genov and G. Cauwenberghs, patent application to be filed.

“Algorithmic Delta-Sigma Analog-to-Digital Converters,” G. Cauwenberghs, F. Adil, G. Mulliken, and R. Genov, patent application to be filed.