An Assessment of the State-of-the-Art 0.5 µm Bulk CMOS Technology for RF Applications

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Abstract

We demonstrate that, given the appropriate layout geometry, state-of-the-art, salicided n-MOSFET's with 0.5 µm drawn gates exhibit similar g_m (160 mS/mm), f_T (20 GHz), f_{MAX} (37 GHz), and F_{MIN} (1.9 dB @ 3.4GHz) as the more costly, metal-reinforced SOI or SOS devices of identical gate length. The record f_{MAX} value for 0.5 µm bulk CMOS is comparable to that of self-aligned, double-polysilicon BJT's.

Introduction

The huge potential market for low-power, hand-held wireless terminals favors a low-cost CMOS solution. A general consensus appears to have emerged that, besides GaAs technologies, advanced Si BJT technologies can meet all the requirements of the RF block. SOI or SOS MOSFET's are also considered [1,2]. It is the purpose of this paper to demonstrate that, with proper characterization and design, the state-of-the-art bulk CMOS is well poised to take on the RF functions up to 2.4 GHz and beyond.

Impact of Gate Geometry on the Maximum Oscillation Frequency

The high frequency performance of MOSFET's is well described by a GaAs-MESFET-like small signal equivalent circuit that includes the usual conductances g_m and g_{ds}, capacitances C_{gd} and C_{gs}, as well as the channel resistance R_i, and the gate and source resistances R_g and R_s, respectively [1,3]. By describing the small signal parameters as functions of the gate length L_g, total gate width W, number of gate fingers n, and gate poly sheet resistance $R_{\square}$, the maximum oscillation frequency f_{MAX} can be expressed as:

$$f_{MAX} = \frac{f_T}{2\sqrt{\frac{R_{\square}W^2}{L_g n^2}(g'_{ds} + 2\pi f_T C'_{gd}) + g_{ds}(R_i + R_s)}} \qquad (1)$$

where, as a result of scalability: $g_{ds}=g'_{ds}W$, $C_{gd}=C'_{gd}W$, $R_g=R_{\square}W/(n^2L_g)$, and $f_T = g_m/2\pi(C_{gs}+C_{gd})$ is the cutoff frequency. In a first order approximation, f_T remains invariant to gate resistance and gate width changes. Eqn. (1) indicates that, for a fixed device width W, f_{MAX} can be improved by reducing $R_{\square}$ or by increasing n. The first approach involves metal-reinforced gates and is expected to provide a factor of ten reduction in R_g [1,2]. The second and more effective solution, requiring only layout optimization, is employed next.

For verification, single and multiple-finger n- and p-channel 0.5 µm MOSFET's with total gate widths of 10, 20 and 40 µm were laid-out in high frequency test pads. S parameter measurements were carried out in the 0.1 to 26.1 GHz range using on-wafer coplanar probes and an HP 8510C Network Analyzer. On-wafer dummy structures were employed to de-embed pad parasitics. f_T and f_{MAX} were determined from the intercept of the current gain vs. frequency (Fig.1) and maxi-

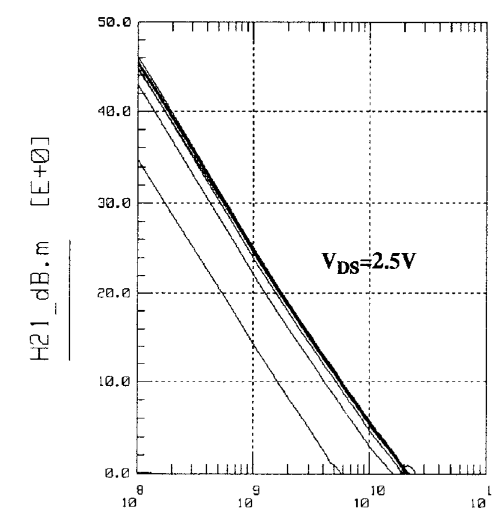

Fig.1: Measured current gain for a 0.5 µm n-channel MOSFET (W=4x10 µm, V_{GS}= 0.5, 0.75,...3V).

mum available gain (MAG) vs. frequency (Fig.2) characteristics, respectively. Figs. 3, for n-channel, and 4, for p-channel devices, show that, by connecting the gate fingers in parallel, a 16-fold gate resistance reduction can be achieved, leading to a 2-fold increase in f_{MAX}, without f_T degradation. As can be inferred from eqn.(1), further reduction of the gate resistance, either by decreasing the sheet resistivity or by increasing the number of gate fingers, does not significantly improve f_{MAX} because the width-independent term $g_{ds}(R_i+R_s)$ becomes dominant. This condition is harder to achieve at smaller gate lengths where gate metal reinforcement may become the

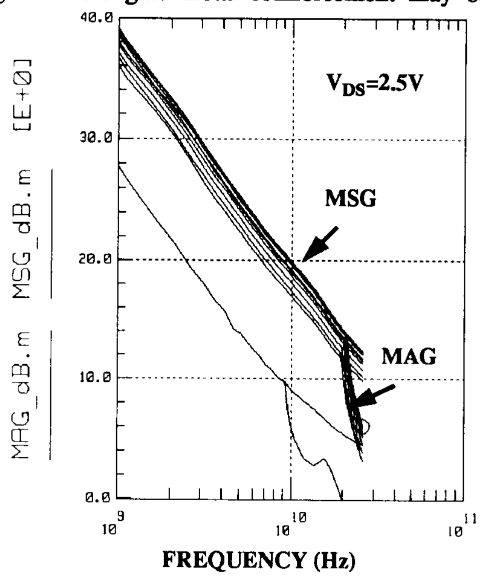

Fig.2: Measured MAG for a 0.5 μm n-channel MOSFET (W=4x10 μm, V_{GS} = 0.5, 0.75,...,3V)

norm. For 0.5 μm technology, layout optimization appears to be sufficient, leading to excellent high speed performance for both n-channel (g_m = 160 mS/mm, f_T = 20 GHz, f_{MAX} = 37 GHz) and p-channel devices (g_m=70 mS/mm, f_T=9 GHz, and f_{MAX} =14 GHz). The f_{MAX} figures are comparable to recent results reported for metal-reinforced SOS MOSFET's [2] and almost a factor of two higher than those reported for 0.5 μm bulk CMOS [4]. The f_T and f_{MAX} characteristics are also compared in Fig. 5 with those of a non-self-aligned polysilicon emitter BJT which can be added to the baseline CMOS process. The f_T's are similar at large current levels but the MOSFET has a clear advantage at low current operation. In terms of f_{MAX}, the MOSFET is faster throughout the bias range and its performance is equal to that of the most advanced ion-implanted Si bipolar technologies [5].

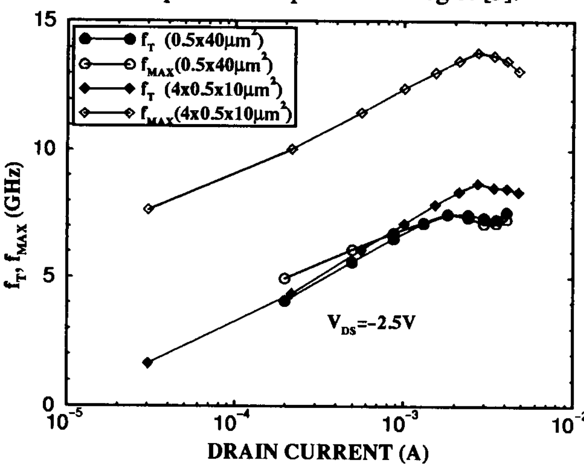

Fig.4: Experimental layout dependence (via R_g) of f_T and f_{MAX} for p-channel MOSFET's.

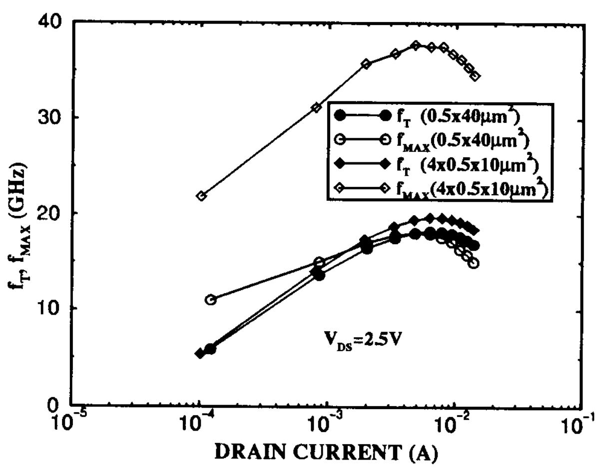

Fig.3: Experimental layout dependence (via R_g) of f_T and f_{MAX} for n-channel MOSFET's.

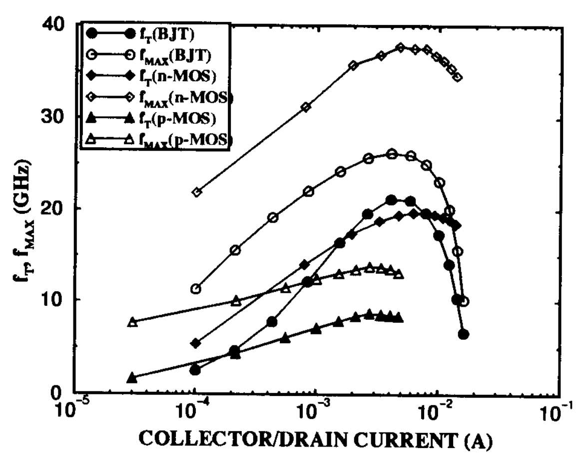

Fig.5: Measured f_T and f_{MAX} characteristics for 0.5 μm MOSFET (W=4x10 μm, $|V_{DS}|$=2.5V) and BJT devices (emitter area: 0.65x25 μm^2, V_{CE}=2V).

Parameter Extraction and Modeling Issues

RF-extracted and MISNAN-modeled [6] small signal parameters and their drain-source voltage dependence are compared in Figs. 6 and 7. The error between measured and modeled conductance and capacitance data is smaller than 10% and it tends to cancel out in f_T. The RF-extracted small signal equivalent circuit parameters, including R_g and R_i, were employed into eqn. (1) to calculate f_{MAX}. Agreement with measured f_{MAX} is excellent, as illustrated in Fig.8. This approach was

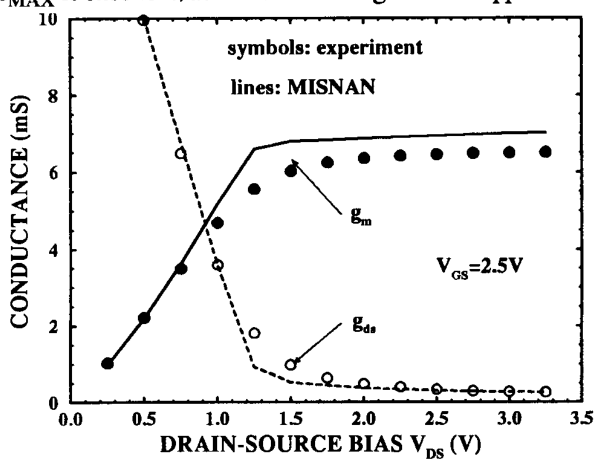

Fig.6: Measured vs. MISNAN-modeled V_{DS} dependence of g_m and g_{ds} for a 0.5 μm n-channel MOSFET. (W=4x10 μm).

necessary since the present version of MISNAN does not model R_i and R_g. Fig.8 also illustrates the variation of f_T and f_{MAX} with drain/collector voltage for MOSFET's and BJT's. The Spice Gummel-Poon model was employed in the BJT

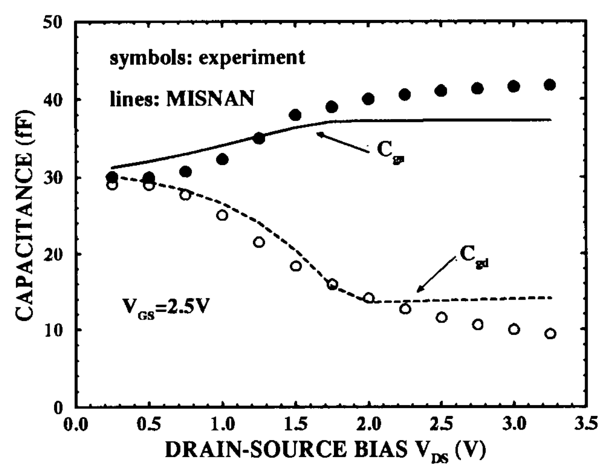

Fig.7: Measured vs. MISNAN-modeled V_{DS} dependence of C_{gs} and C_{gd} for a 0.5 μm n-channel MOSFET. (W=4x10 μm).

calculations. For these technologies, the BJT is faster than the n-channel MOSFET below 1.5 V, making it the low-voltage and high-speed device of choice. Furthermore, f_T and f_{MAX} are almost insensitive to V_{CE}.

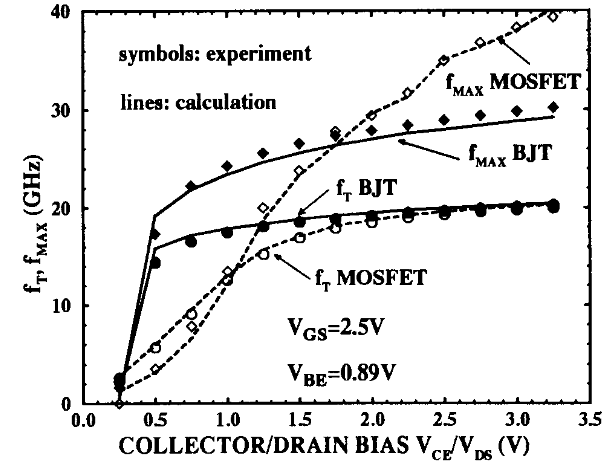

Fig.8: Measured and calculated V_{CE}/V_{DS} dependence of f_T and f_{MAX} for a 0.65*25 μm^2Si BJT and a 0.5 μm n-MOSFET (W=4x10 μm), respectively.

High Frequency Noise Performance

Automated, on-wafer noise figure measurements were carried out in the 2-6 GHz range using an ATN setup. For comparison, the minimum noise figure F_{MIN}, the associated power gain G_{ASS}, and the normalized noise resistance r_n, are plotted in Figs. 9 and 10 for a MOSFET and for a BJT, respectively. The noise contribution of the probing pads was not de-embedded from the noise figure results. The noise

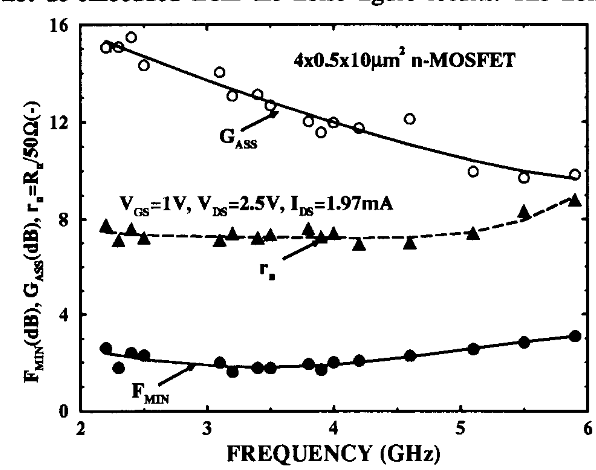

Fig.9: Measured minimum noise figure F_{MIN}, associated gain G_{ASS}, and normalized noise resistance r_n for an n-channel MOSFET.

figure of the n-channel MOSFET was 1.9 dB at 3.4 GHz with an associated power gain of 13 dB. F_{MIN} values were typically 0.1-0.3 dB lower than those of the BJT, throughout

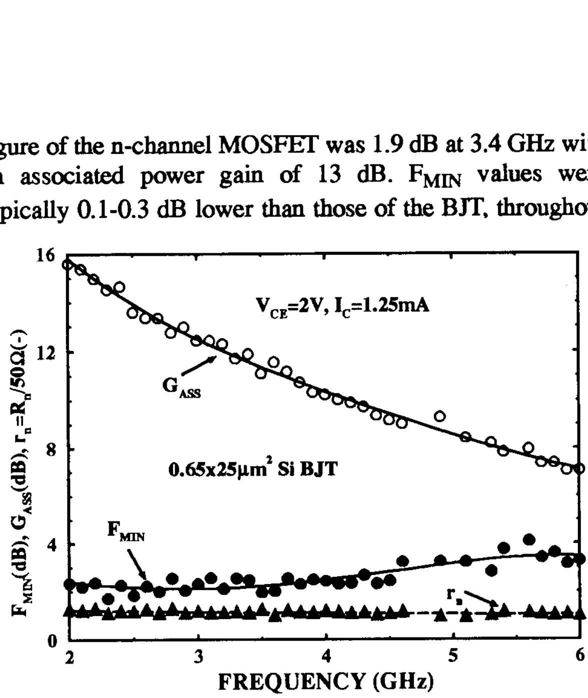

Fig.10: Measured minimum noise figure F_{MIN}, associated gain G_{ASS}, and normalized noise resistance r_n for a silicon BJT.

the measurement band. The associated gain was also higher for the MOSFET, in agreement with the larger f_{MAX}. Despite the excellent noise figure, similar to that reported for SOS devices [2], the much higher optimum source reflection coefficient (Fig. 11) of the MOSFET complicates low-noise matching. The problem is compounded by the large noise resistance which makes the noise figure of a MOSFET circuit very sensitive to source impedance mismatch. A solution is to increase the device size at the expense of larger drain current and power dissipation. In such a case, a circuit with bipolar transistors requires lower bias current and dissipates less power for comparable noise figures.

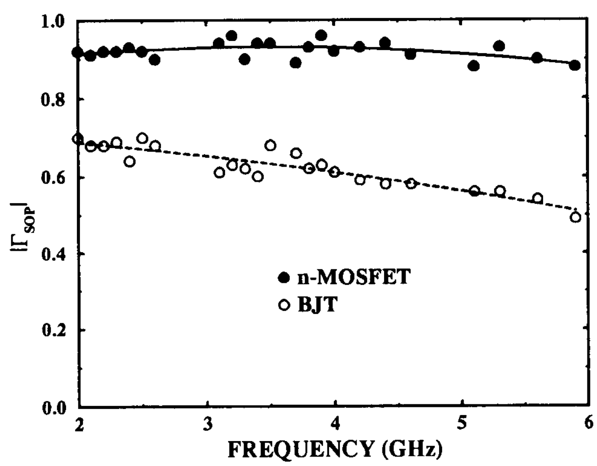

Fig.11: Measured optimum noise reflection coefficient for a 0.65x25 μm² Si BJT and a 4x0.5x10 μm² n-MOSFET.

Finally, on-wafer load-pull measurements, performed using mechanical slide screw tuners, revealed a large signal gain of 10 dB, at 2 GHz. Because of the small size, output and input matching was not optimal. With proper width scaling, these MOSFET's can be used for low-voltage (push-pull) power amplifiers in wireless handsets, obviating the requirement for high voltage LDD structures [7].

Conclusion

Record high frequency and noise performance was demonstrated for 0.5 μm bulk CMOS technology, making it a viable candidate for integrating most RF functions up to 2.4 GHz. In comparison with a BiCMOS-class silicon bipolar device, n-channel MOSFET's show higher f_{MAX} and slightly better F_{MIN} values. The speed advantage prevails at low current operation but is lost under low-voltage regime. The minimum noise figure of MOSFET's was found to be lower than 2 dB up to 3.5 GHz, sufficient for most LNA requirements. Although not critical for low-noise amplifier functions, the availability of a BJT is beneficial. For identical bias conditions, the high transconductance of the BJT leads to smaller optimum source reflection coefficient and noise resistance, simplifying low-power noise matching.

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