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NEW TECHNIQUE FOR THE CHARACTERIZATION OF Si/SiGe LAYERS USING HETEROSTRUCTURE MOS CAPACITORS

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Abstract—This paper presents a comprehensive on-line electrical characterization technique addressing the emerging Si/SiGe MOS technology. It demonstrates that the experimental high frequency and low frequency C–V characteristics of Si/SiGe heterostructure MOS capacitors can provide accurate material-, process-, and device-related information such as: the valence band offset, Si cap layer thickness, substrate doping, and MOSFET threshold voltages.

NOTATION

C_{ox}	gate oxide capacitance per unit area
C_{HF}	high frequency gate capacitance per unit area
C_{LF}	low frequency gate capacitance per unit area
D_{it}	interface trapped charge density at the Si–SiO_2 interface
E	energy
E_A	energy level of shallow acceptors
E_{AT}	energy level of deep acceptor traps
E_D	energy level of shallow donors
E_{DT}	energy level of deep donor traps
E_C	conduction band energy
E_F	Fermi level energy
E_i	hole eigenenergies in the quantum well
$\hbar$	Planck's constant
$H(\phi_H)$	contribution of holes to the electric field in the SiGe film
k	Boltzmann constant
m_h	effective mass of holes
n	electron concentration
N_{appHF}	apparent doping obtained from high frequency measurements or calculations
N_{appLF}	apparent doping obtained from low frequency measurements or calculations
N_A	shallow acceptor concentration
N_A^-	ionized shallow acceptor concentration
N_{AT}	deep acceptor trap concentration
N_B	effective doping concentration in the bulk of the semiconductor
N_C	conduction band density of states
N_D	shallow donor concentration
N_D^+	ionized shallow donor concentration
N_{DT}	deep donor trap concentration
N_{VSi}	valence band density of states in silicon
N_{VSiGe}	valence band density of states in SiGe
p	hole concentration
p_H	hole concentration at the heterointerface
p_S	hole concentration at the surface
q	electron charge
Q_f	fixed oxide charge at the Si–SiO_2 interface
Q_T	total charge in the semiconductor
T	temperature
V_{FB}	flat-band voltage
V_G	gate voltage
V_{TH}	threshold voltage at the top SiGe/Si heterointerface
V_{TS}	threshold voltage at the silicon cap surface
x	Ge content in the SiGe film
x_{av}	hole charge centroid location
x_{ca}	silicon cap thickness
x_{dHF}	depletion layer width obtained from high frequency measurements or calculations
x_{dLF}	depletion layer width obtained from low frequency measurements or calculations
x_{dm}	maximum depletion layer width in strong inversion
x_{ox}	gate oxide thickness
ΔE_V	valence band offset between SiGe and Si
ΔE_{Vapp}	apparent valence band offset between SiGe and Si
ΔV_T	gate voltage window
ϵ	permittivity
ϵ_{ox}	SiO_2 permittivity
ϵ_{Si}	silicon permittivity
ϵ_{SiGe}	SiGe permittivity
ϕ	potential
ϕ_F	Fermi potential
ϕ_H	potential at the top heterointerface
ϕ_{TH}	potential at threshold at the top heterointerface
ϕ_S	potential at the surface
ϕ_{TS}	potential at threshold at the surface
ϕ_{MS}	work function difference between the gate and the silicon substrate
ψ_i	hole wavefunctions
∇	gradient

1. INTRODUCTION

A salient feature of the $Si/Si_{1-x}Ge_x$ heterostructure system is the possibility of realizing high quality oxides, comparable to those obtained on Si[1,2]. It is the purpose of this paper to show that the Si/SiGe

heterostructure MOS capacitor can become an excellent and thorough characterization vehicle for Si-based heterostructure technology. The structure used in this investigation is shown in Fig. 1 and is similar to that of a conventional MOS capacitor, except for the presence of the SiGe channel, separated from the Si/SiO_2 interface by a thin Si cap layer.

Since the type I Si/SiGe heterojunction has a negligible conduction band offset, the accumulation and depletion regions of the low frequency C_{LF}–V_G capacitance–voltage characteristics are similar to those of a MOS capacitor fabricated on Si, as illustrated in Fig. 2. The high frequency C_{HF}–V_G characteristics of Si/SiGe capacitors also resemble those of their Si counterparts. As a consequence, the oxide thickness x_{ox}, substrate doping N_B, maximum depletion depth x_{dm}, and the flat-band voltage V_{FB} can be extracted directly from the experimental C–V curves according to established techniques[3].

The differences between heterostructure and homostructure MOS capacitors become apparent only in the inversion regime of the C_{LF}–V_G characteristics. The heterostructure capacitor exhibits two thresholds, V_{TH} corresponding to charge inversion at the top Si/SiGe heterojunction, and V_{TS} related to charge inversion at the Si/SiO_2 interface[4]. The C_{LF}–V_G characteristics also show a plateau of slow-varying capacitance. The value of the plateau capacitance depends on the thickness of the Si cap layer x_{ca}. Its width is determined by the valence band offset ΔE_V at the top Si/SiGe interface and by x_{ca}. These features can be used to extract accurate material-related data for the heterostructure, most importantly, the valence band offset.

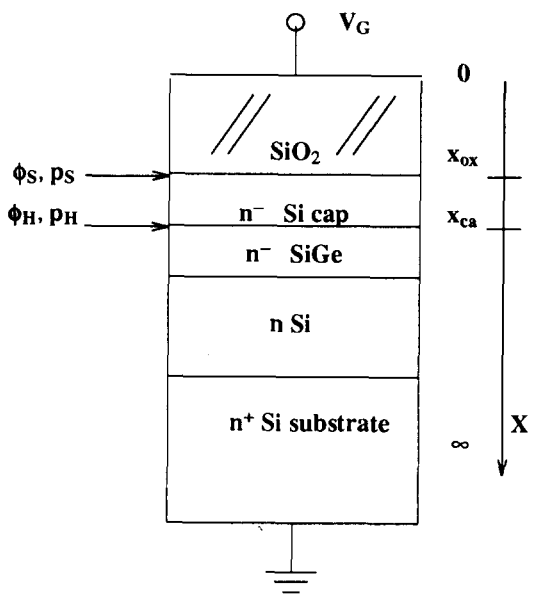

Fig. 1. $Si/Si_{1-x}Ge_x$ MOS capacitor used as test structure. Notations used for hole concentration and electric potential at the top heterojunction and at the Si/SiO_2 interface are also shown.

To achieve this goal, one needs to (a) determine the cap layer thickness x_{ca} and the threshold voltages, and (b) to quantify the relation between ΔE_V on one side, and V_{TH}, V_{TS} and x_{ca} on the other. It is in the extraction of the cap layer thickness and of the valence band offset that this paper offers original solutions.

The rest of the paper is organized as follows. Section 2 describes the C_{LF}–V_G characteristics and the resulting apparent doping profiles of heterostructure MOS capacitors as obtained from self-consistent numerical solutions of Poisson's and Schrödinger's equations. An analytic model is employed to calculate the valence band offset as a function of the measured threshold voltages and of the structural parameters. The sources of errors that may affect the value of the extracted valence band offset are also addressed. Section 3 presents the new characterization technique. Section 4 describes the test structures and the experimental validation of the characterization technique. Conclusions are provided in Section 5.

2. THEORETICAL BACKGROUND

2.1. C–V characteristics of heterostructure MOS capacitors

Numerical simulations have been carried out to investigate the quantitative link between the internal layer structure and the C_{LF}–V_G characteristics of Si/SiGe MOS capacitors. As will be explained, the position of the inversion charge at the top Si/SiGe heterojunction must be accurately known in order to determine the cap layer thickness. A classical approach using Fermi–Dirac statistics does not explain the size-quantization induced offset between the heterojunction and the position of the centroid of the accumulated charge. Because this quantum effect has to be accounted for, a numerical simulator was developed that selfconsistently solves Poisson's equation:

$$\nabla(\epsilon\nabla\phi) = -q[N_D^+ - N_A^- - n + p], \tag{1}$$

and Schrödinger's equation:

$$-\frac{\hbar^2}{2}\nabla\left(\frac{1}{m_h}\nabla\psi_i\right) + (\phi - E_i)\psi_i = 0, \tag{2}$$

in one dimension to obtain the potential ϕ, hole wavefunctions ψ_i, corresponding to each eigenenergy E_i, and the concentration of holes p throughout the structure[5]:

$$p = \frac{m_h kT}{\pi\hbar^2}\sum_{i=1}^{\infty}|\psi_i|^2 \ln\left[1 + \exp\left(\frac{E_i - E_F}{kT}\right)\right]. \tag{3}$$

Since only the inversion region of the C_{LF}–V_G characteristics is of interest, the electron concentration is

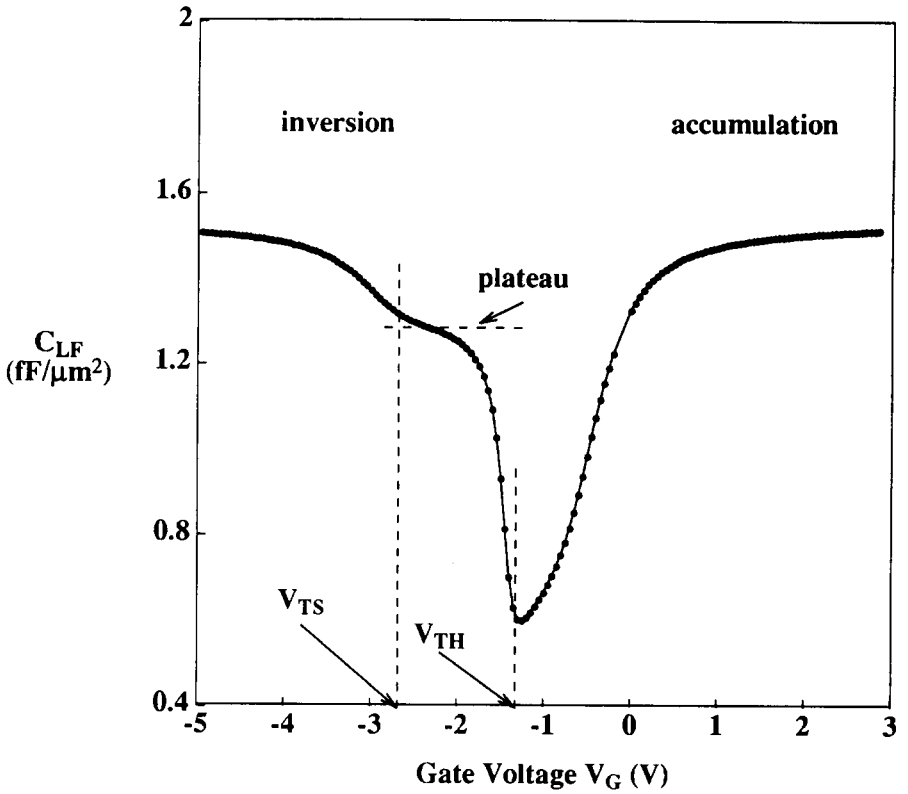

Fig. 2. Typical C_{LF}–V_G characteristics of $Si/Si_{1-x}Ge_x$ MOS capacitors showing threshold voltages and capacitance plateau.

assumed to obey Boltzmann statistics and is included as such in Poisson's equation:

$$n = N_C \exp\left(\frac{E_F - E_C}{kT}\right). \tag{4}$$

The analysis also accounts for interface trapped charge D_{it}, fixed interface charge Q_f and for the contribution of deep level N_{DT}, N_{AT}, and shallow level traps N_D, N_A, located either in the Si or in the SiGe film. The ionized fixed charge densities N_D^+ and N_A^- are calculated as functions of the trap energies: E_{DT}, E_D, E_{AT}, E_A, according to the formulae[6]:

$$N_D^+ = \frac{N_D}{1 + 2\exp\left(\frac{E_F - E_D}{kT}\right)} + \frac{N_{DT}}{1 + 2\exp\left(\frac{E_F - E_{DT}}{kT}\right)} \tag{5}$$

$$N_A^- = \frac{N_A}{1 + 4\exp\left(\frac{E_A - E_F}{kT}\right)} + \frac{N_{AT}}{1 + 4\exp\left(\frac{E_{AT} - E_F}{kT}\right)}. \tag{6}$$

The simulator calculates the potential ϕ_H and the peak hole concentration p_H at the top Si/SiGe heterojunction, and at the Si/SiO_2 interface ϕ_S, p_S, respectively, the overall charge:

$$Q_T(V_G) = \int_{\infty}^{0} q[N_D^+(x, V_G) - N_A^-(x, V_G) - n(x, V_G) + p(x, V_G)]\,dx \tag{7}$$

and the hole charge centroid location:

$$x_{av}(V_G) = \frac{\int_{\infty}^{0} xp(x, V_G)\,dx}{\int_{\infty}^{0} p(x, V_G)\,dx}, \tag{8}$$

all as functions of the gate voltage V_G. Next, the low frequency capacitance, which is a measurable terminal function, is calculated:

$$C_{LF}(V_G) = \frac{\partial Q_T(V_G)}{\partial V_G}. \tag{9}$$

Such characteristics are compared in Fig. 3 for Si and Si/SiGe MOS capacitors. There is no capacitance plateau in the case of the Si structure, but the accumulation regions are identical, allowing for the simple extraction of the flat-band voltage.

2.2. *Apparent doping profiles and their interpretation*

From the calculated C_{LF}–V_G characteristics, the depletion depth x_{dLF}:

$$x_{dLF}(V_G) = \epsilon_{Si}\left(\frac{1}{C_{LF}(V_G)} - \frac{1}{C_{ox}}\right), \tag{10}$$

and apparent doping N_{appLF}:

$$\frac{1}{N_{appLF}(V_G)} = \frac{q\epsilon_{Si}}{2}\frac{\partial\left(\frac{1}{C_{LF}^2(V_G)}\right)}{\partial V_G}, \tag{11}$$

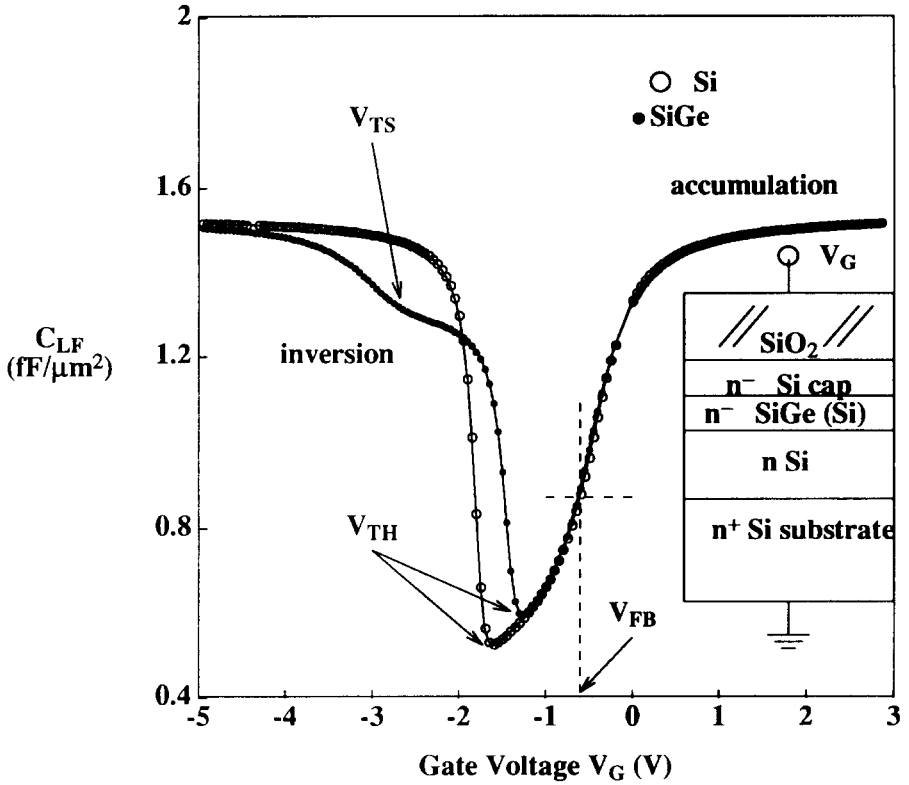

Fig. 3. Comparison of simulated C_{LF}–V_G characteristics of Si and $Si/Si_{1-x}Ge_x$ MOS capacitors with layer structure shown in the inset.

are obtained as functions of the applied gate voltage. The term "apparent doping" refers to the contributions of both fixed and mobile charge.

Further, the computed C_{LF}–V_G and N_{appLF}–V_G profiles are correlated with the voltage dependence of the peak hole concentrations at the top heterojunction and at the Si/SiO_2 interface. The thresholds V_{TH} and V_{TS} are defined as the gate voltages at which the peak hole concentration at the respective interface equals the background doping:

$$p_H(V_G = V_{TH}) = N_B, \quad p_S(V_G = V_{TS}) = N_B.$$

If the high frequency capacitance voltage characteristics are employed in eqns (10) and (11) then the corresponding high frequency depletion depth and apparent doping, x_{dHF} and N_{appHF}, respectively, are obtained.

The C_{LF}–V_G characteristics cannot directly provide very accurate values for V_{TH}, V_{TS} and x_{ca} because the transitions between the various regions of the inversion regime tend to be smoothed out at room temperature. To precisely identify V_{TH} and V_{TS}, one has to plot the N_{appLF}–V_G characteristics.

The absolute value of the apparent doping characteristics for the structure in Fig. 3 is plotted in Fig. 4. It exhibits two regions in which the apparent doping is high and dominated by the mobile charge: one for large positive bias corresponding to accumulation of electrons, and another, for large negative bias, associated with strong inversion. Between them lie the regions of interest to the characterization method: namely a plateau corresponding to the depletion regime whose value gives the substrate doping ($N_B = N_D - N_A$), and sharp transitions with local maxima related to the thresholds. The onset of inversion at the top heterojunction is marked by a change of sign and an abrupt transition on the N_{appLF}–V_G characteristics while inversion at the Si/SiO_2 interface is signalled by a local maximum of the apparent doping. This local maximum is particular to SiGe structures and gives the value of V_{TS}.

The thickness of the cap layer can be extracted from the apparent doping vs depth profile N_{appLF}–x_{dLF}, as shown in Fig. 5. This curve is obtained by combining the x_{dLF}–V_G and N_{appLF}–V_G characteristics, from eqns (10) and (11), respectively. There are two appparent doping values, of opposite sign, for each position x_{dLF}, one corresponding to the inversion- and one to the accumulation/depletion regime of the C_{LF}–V_G characteristics. Only the absolute value of the apparent doping profile is shown. The apparent doping obtained from the inversion region exhibits three peaks, corresponding (from the left to right) to: (a) the accumulation of mobile holes at the Si/SiO_2, (b) accumulation of holes at the top Si/SiGe heterojunction and (c) to the maximum depletion depth, where the change of sign in the apparent doping occurs. The thickness of the Si cap layer can be

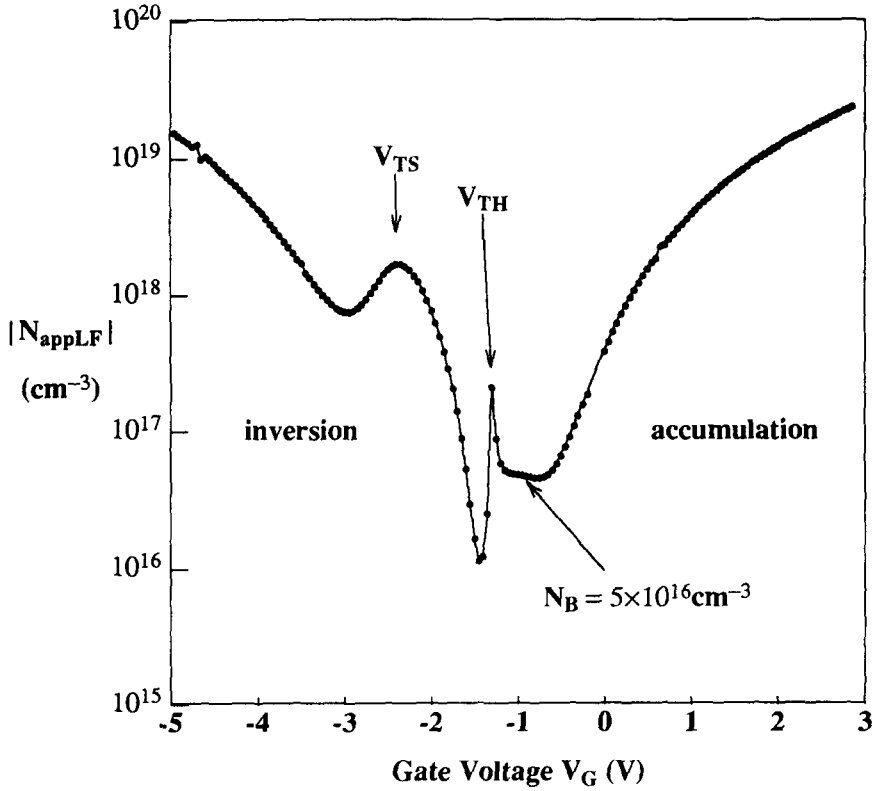

Fig. 4. Low frequency apparent doping vs gate voltage characteristics for a $Si/Si_{1-x}Ge_x$ MOS determined from the simulated C_{LF}–V_G characteristics of Fig. 3.

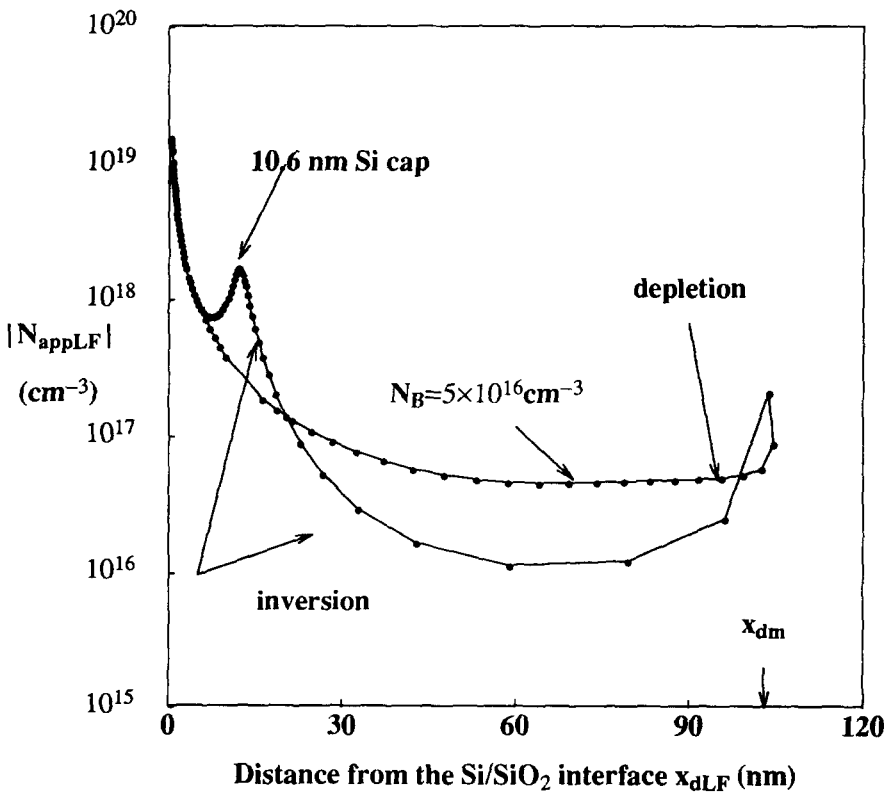

Fig. 5. Low frequency apparent doping vs depth profiles in $Si/Si_{1-x}Ge_x$ MOS capacitors obtained from the simulated C_{LF}–V_G characteristics of Fig. 3.

directly extracted from the position of the second peak.

2.3. Calculation of the valence band offset

To provide the quantitative relation between the measured threshold voltages and the valence band offset, a recently developed analytical model that predicts the threshold voltages in a Si/SiGe MOSFET is employed[4]. The inversion potential at the top Si/SiGe heterojunction ϕ_{TH} and at the Si/SiO_2 interface ϕ_{TS}, respectively, is defined as:

$$\phi_{TH} = \phi_H(V_G = V_{TH}), \quad \phi_{TS} = \phi_S(V_G = V_{TS}).$$

We start from the expressions that relate V_{TH} and V_{TS} to the structural parameters of the capacitor:

$$V_{TH} = V_{FB} + \phi_{TH} - qN_B x_{dm}\left(\frac{x_{ca}}{\epsilon_{Si}} + \frac{x_{ox}}{\epsilon_{ox}}\right) \quad (12)$$

$$V_{TS} = V_{FB} + \phi_{TS} - \frac{qN_B x_{dm}}{C_{ox}}\sqrt{1 + H(\phi_H)}, \quad (13)$$

where:

$$\phi_{TH} = 2\phi_F + \frac{\Delta E_V}{q}$$

$$H(\phi_H) = hfo \exp\left(\frac{\phi_{TH} - \phi_H}{kT/q}\right)$$

$$hfo = \frac{2\epsilon_{SiGe} N_B kT}{(qN_B x_{dm})^2}$$

and

$$\Delta V_T = V_{TH} - V_{TS} \text{ (the gate voltage window).}$$

By subtracting eqn (13) from eqn (12) and rearranging, a system of two nonlinear equations (14) and (15), with ΔE_V and ϕ_H as unknowns is obtained:

$$\Delta E_V = \phi_H - 2\phi_F + \frac{kT}{q} \times \ln\left[\frac{\left[1 + C_{ox}\frac{x_{ca}}{\epsilon_{Si}} + \frac{C_{ox}(\Delta V_T + \Delta E_V)}{qN_B x_{dm}}\right]^2 - 1}{hfo}\right] \quad (14)$$

$$\phi_H = \phi_{TH} - \frac{kT}{q}\ln\left[\frac{\left[\frac{\epsilon_{Si}(\phi_H - 2\phi_F)}{qN_B x_{dm} x_{ca}}\right]^2 - 1}{hfo}\right]. \quad (15)$$

One can calculate the valence band offset by iterating eqns (14) and (15) until a solution is found. The valence band offset determined in this manner refers to the properties of the SiGe region in the vicinity of the top Si/SiGe interface. If the SiGe layer is graded, the measured band offset reflects the Ge content at the interface, and not the average Ge content in the channel[4].

2.4. Sources of error affecting ΔE_V

Errors in the determination of the valence band offset may be attributed to: (a) equipment limitations, (b) interface and/or bulk traps and (c) model limitations.

2.4.1. Equipment limitations. The sensitivity of the measured valence band offset to inaccuracies in the values of the structural parameters was simulated. It was found that errors in C_{ox}, x_{ca}, x_{dm} and N_B affect ΔE_V linearly. Of these x_{ca} requires corrections to account for quantum effects. Simulations using two-dimensional (2D) hole gas statistics indicate that the hole charge centroid is located about 2 nm away from the top Si/SiGe heterointerface. This offset has to be subtracted from the experimentally extracted value of x_{ca}.

2.4.2. Interface and bulk traps. According to the eqns (12) and (13), both V_{TH} and V_{TS} depend on the flat-band voltage V_{FB}. However, because the latter's effect cancels out in ΔV_T, fixed surface charge Q_f and ϕ_{MS} do not affect the value of the measured valence band offset. The major source of uncertainty associated with the value of ϕ_{MS} is thus eliminated.

Even a small interface trapped charge concentration (of the order of $10^{11}\,cm^{-2}\,eV^{-1}$) changes the shape of the low frequency apparent doping profile N_{appLF}–x_{dLF} in the depletion regime, raising its value and reducing the maximum depletion depth. In order to eliminate any inaccuracies on ΔE_V due to incorrect maximum depletion depth and substrate doping values, both x_{dm} and N_B must be determined from the high frequency apparent doping profile N_{appHF}–x_{dHF} since traps do not respond to high frequency signals.

In strong inversion, the impact of the interface traps on the N_{appLF}–x_{dLF} profile is eliminated by the large concentration of holes piling up at the Si/SiO_2 and Si/SiGe interfaces. The cap layer thickness, given by the position of the hole charge centroid should therefore be insensitive even to moderately high trap density.

The interface trapped charge distribution $D_{it}(E)$, located between the positions of the Fermi level at the Si/SiO_2 interface corresponding to V_{TH} and V_{TS}, respectively, also alters the measured gate voltage window ΔV_T. Simulation results indicate that a uniformly distributed interface trap density of $2 \times 10^{11}\,cm^{-2}\,eV^{-1}$ causes errors of 25 mV in the gate voltage window ΔV_T and 0.5 nm in the cap layer thickness. It may be safely concluded that by simultaneously using experimental low frequency and high frequency apparent doping profiles the error caused by the interface trapped charge density on the extracted valence band offset can be minimized.

Errors in ΔE_V can also be caused by bulk traps in SiGe[7], if their concentration is larger than one fifth of the active doping. Their presence is signaled by a kink in the depletion region of the C_{LF}–V_G characteristics which in turn causes an easily identifiable local peak on the N_{appLF}–x_{dLF} profile.

2.4.3. Model limitations. Due to the lack of reliable experimental data for the valence band density of

states in SiGe, the densities of states in Si and SiGe were tacitly assumed to be identical in the derivation presented in the preceding section. Therefore, the analytical model actually gives an "apparent" valence band offset:

$$\Delta E_{V_{app}} = \Delta E_V - kT \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right]. \quad (16)$$

By neglecting the contribution of the second term in eqn (16) the error will not be larger than ± 25 meV at room temperature.

For Ge mole fractions smaller than 30%, the hole charge at the top Si/SiGe heterojunction is screened by the charge at the Si/SiO_2 interface and neither the cap layer thickness nor the surface conduction threshold V_{TS} can be precisely identified at room temperature. To overcome this problem the sample must be cooled. At 77 K, even samples with 15% Ge clearly exhibit the hole charge accumulation at the top Si/SiGe interface.

Finally, eqns (12) and (13) are based on Boltzmann statistics. Comparison of simulated and analytically derived threshold voltages indicate that the analytical model underestimates both thresholds by 15–25 mV. This error cancels in ΔV_T and does not affect the extracted value of ΔE_V.

3. PROPOSED CHARACTERIZATION TECHNIQUE

Based on the discussion above, the following steps can be used to characterize the Si/SiGe layers:

(a) The oxide capacitance, flatband voltage, maximum depletion depth and the effective substrate doping are extracted from experimental C_{HF}–V_G characteristics and N_{appHF}–x_{dHF} profile, respectively, as for a Si MOS capacitor. Interface trapped charge density and bulk traps, which do not respond to the high frequency signal, will thus not influence the extracted values of the substrate doping and maximum depletion depth.

(b) Equations (10) and (11) are then applied to the experimental C_{LF}–V_G characteristics to determine the N_{appLF}–V_G characteristics and the N_{appLF}–x_{dLF} profile. From the inspection of the latter, accurate values of the threshold voltages V_{TH}, V_{TS} and of the cap layer thickness x_{ca} are obtained in the manner outlined in the preceding section.

(c) The data obtained in the previous two steps are fed into eqns (14) and (15) to determine the valence band offset.

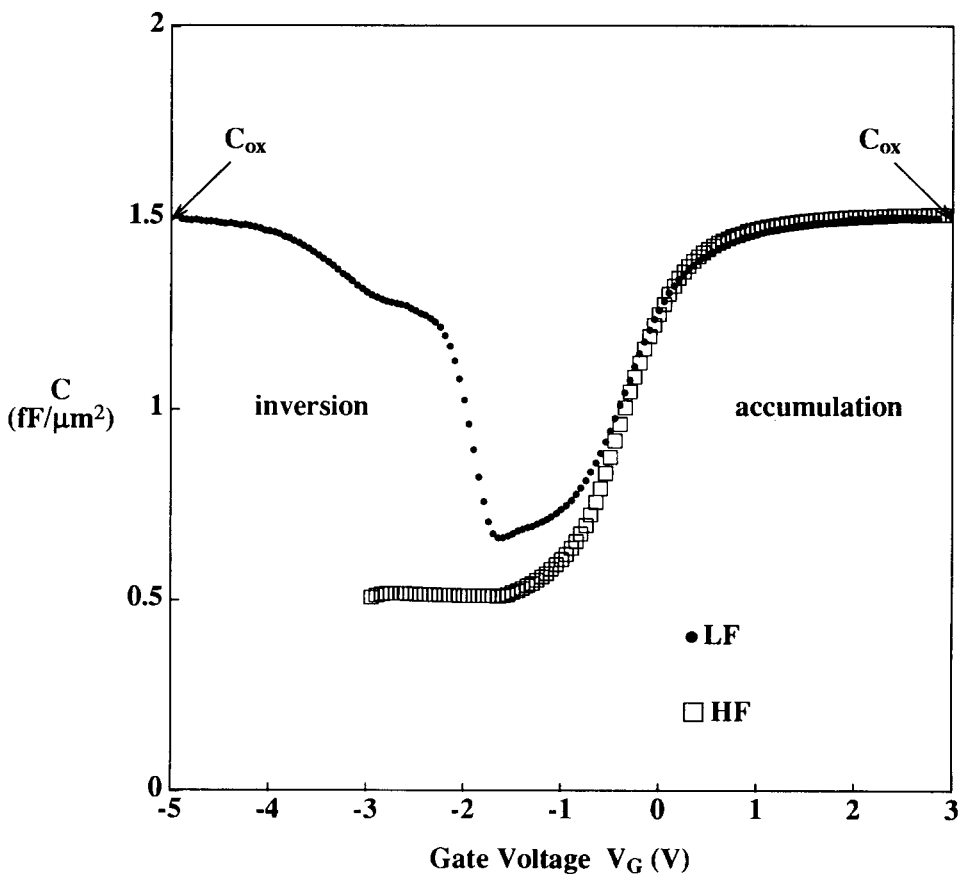

Fig. 6. Typical experimental C_{HF}–V_G and C_{LF}–V_G characteristics of graded (0–47% Ge) $Si/Si_{1-x}Ge_x$ MOS capacitors. The structure is similar to that presented in Fig. 3.

(d) D_{it} is estimated from the difference between the experimental C_{LF}–V_G and C_{HF}–V_G characteristics[8] and by matching the simulated and measured low frequency apparent doping profiles.

(e) Q_f is extracted from the difference between the measured and calculated flatband voltage, after the contribution of the interface trapped charge on the flatband voltage has been removed.

As in the case of Si MOS capacitors, the accuracy of the interface trapped charge density determined in step (d) is limited to the midgap region.

4. EXPERIMENTAL RESULTS

For experimental confirmation, Si/SiGe wafers were grown by MBE with the following layer structure: n^+ substrate doped $2 \times 10^{19}\,cm^{-3}$, n-type Si epitaxial layer doped $2 \times 10^{17}\,cm^{-3}$ and 0.3 μm thick, n-type Si spacer doped $5 \times 10^{16}\,cm^{-3}$ and 200 nm thick, undoped SiGe layer 15 nm thick, and undoped Si cap layer 10 nm thick. The Ge mole fraction was graded from 0% (bottom) to 50% (top). A low thermal-budget process was employed to create the gate oxide: 1 min RTO at 850°C, followed by a 3 min LPCVD (139 mtorr, 12% O_2, 6.7% SiH_4) at 410°C and followed by a 1 min RTO at 850°C. Capacitors with areas varying from 6.25×10^{-6} to $1.52 \times 10^{-2}\,cm^2$ were defined by Al deposition and wet-etch patterning. Al was also sputtered on the back side to provide a large-area ohmic contact. A postmetallization anneal was performed in forming gas at 420°C for a duration of 20 min.

The doping profile was independently confirmed by spreading resistance measurements. Auger spectroscopy was used to verify the Ge profile. The depth resolution was 5 nm, sufficient to confirm the thickness of the SiGe film and its graded profile (approximately 20 nm) but not accurate enough to determine the thickness of the cap layer, and the precise Ge concentration at the top Si/SiGe interface. The Ge profile linearly increases from 0% Ge for about 12 nm, saturates at just above 40% Ge and then drops steeply back to 0%. If one extrapolates the slope of Ge grading in the linear region, a value close to 50% Ge is found at the top Si/SiGe interface.

The C_{LF}–V_G and C_{HF}–V_G characteristics were measured using Hewlett Packard's 4280A 1 MHz C Meter and are plotted in Fig. 6. Corrections were made for parasitic capacitances and leakage currents but no attempt was made to smooth out the experimental data by interpolation. First, the oxide thickness $x_{ox} = 22.3$ nm was determined from the C_{LF}–V_G characteristics presented in Fig. 6, and the substrate doping $N_B = 5 \times 10^{16}\,cm^{-3}$ was obtained from the associated N_{appHF}–x_{dHF} profile, shown in Fig. 7. Then, from the inversion region of the experimental C_{LF}–V_G

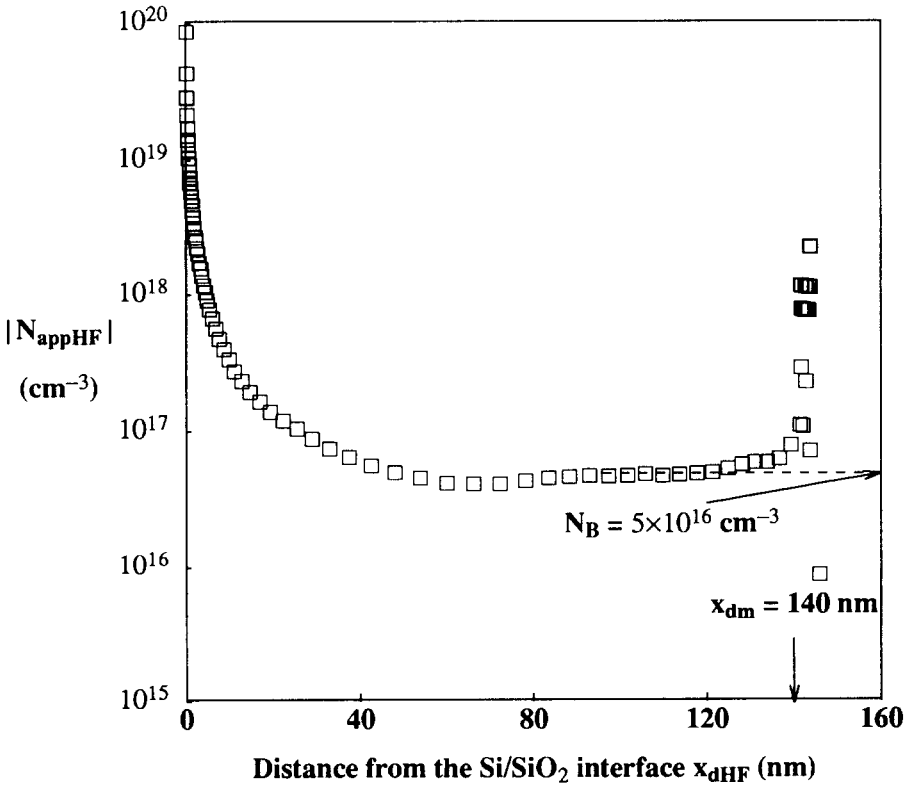

Fig. 7. Experimental high frequency apparent doping vs depth profiles in $Si/Si_{1-x}Ge_x$ MOS capacitors obtained from the measured C_{HF}–V_G characteristics of Fig. 6.

characteristics, plotted in Fig. 8, the N_{appLF}–V_G and N_{appLF}–x_{dLF} profiles were calculated and are presented in Figs 9 and 10, respectively. The two thresholds $V_{TH} = -1.65$ V and $V_{TS} = -2.8$ V were identified from the experimental trace in Fig. 9 and the cap layer thickness $t_{ca} = 10.6$ nm was deduced from the apparent doping vs depth profile, as shown in Fig. 10. Even though it is not evident from the experimental characteristics in Fig. 9, V_{TH} can be easily identified because it corresponds to a change of sign in the apparent doping.

Using these data, the valence band offset $\Delta E_V = 347$ meV was extracted by solving eqns (14) and (15). If one assumes that the valence band offset depends on the Ge mole fraction x_{Ge} according to the formula[9]:

$$\Delta E_V = 0.74 * x_{Ge}$$

then the measured valence band offset corresponds to a Ge mole fraction of 0.47.

An average interface trap density $D_{it} = 7 \times 10^{10}\,cm^{-2}\,eV^{-1}$ was estimated from the difference between the experimental low frequency and high frequency C–V curves. As explained in Section 2.4, this value is low enough not to significantly affect the accuracy of the measured valence band offset.

To validate the characterization technique, the extracted structural and material parameters were used as input data into the heterostructure MOS capacitor simulator. A uniformly distributed interface trap density of $7 \times 10^{10}\,cm^{-2}\,eV^{-1}$ was included in the simulation and a fixed charge density $Q_f = 2.8 \times 10^{11}\,cm^{-2}$ was determined by superimposing the calculated and experimental $C_{LF}(V_G)$ characteristics, as shown in Fig. 8. The simulated and experimentally derived N_{appLF}–V_G and N_{appLF}–x_{dLF} characteristics are plotted in Figs 9 and 10, respectively. They all show good agreement between theory and experiment.

5. CONCLUSION

A novel technique for the characterization of Si/SiGe layers was developed and verified experimentally using heterostructure MOS capacitors as test structures. Quantum-mechanics numerical modeling

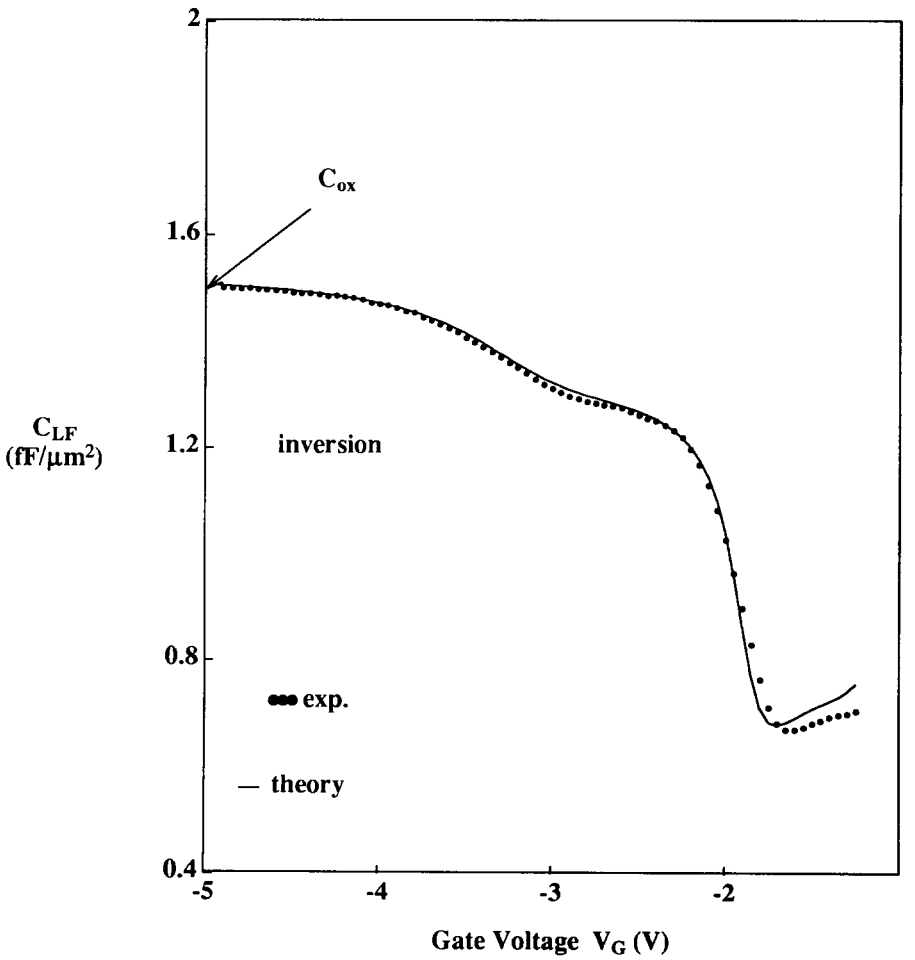

Fig. 8. Comparison of measured and simulated C_{LF}–V_G characteristics of $Si/Si_{1-x}Ge_x$ MOS capacitors based on extracted structural and material data.

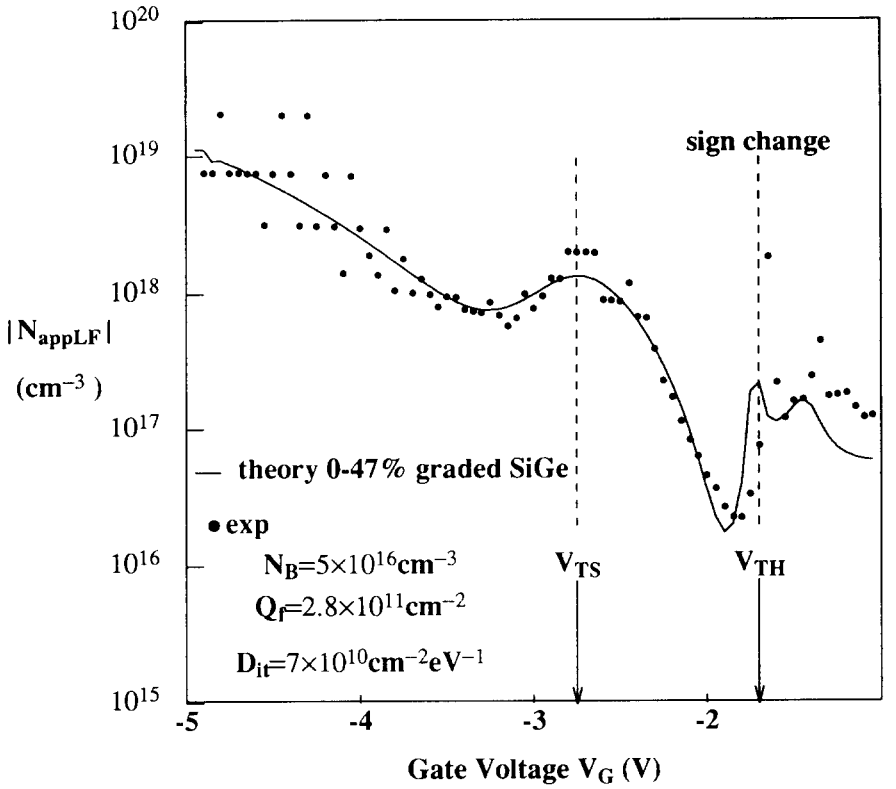

Fig. 9. Simulated and experimental apparent doping vs gate voltage characteristics for a graded 0–47% Ge $Si/Si_{1-x}Ge_x$ MOS capacitor as determined from the measured C_{LF}–V_G characteristics shown in Fig. 6.

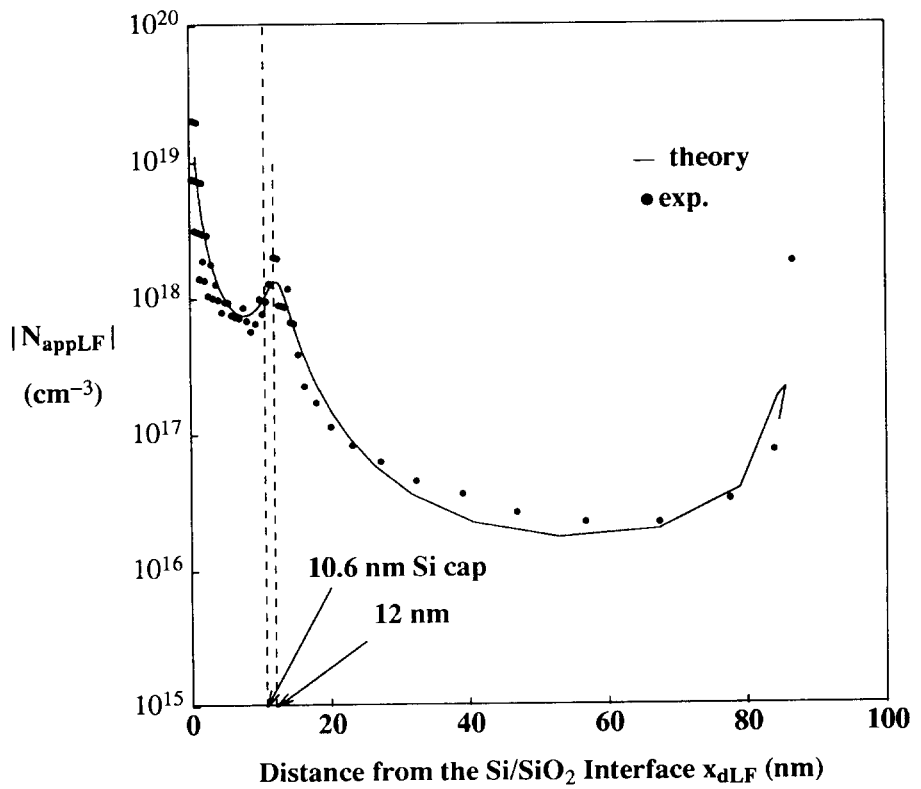

Fig. 10. Simulated and experimental apparent doping vs depth profiles. The experimental data are obtained from the inversion region of the measured C_{LF}–V_G characteristics of Fig. 6. The size-quantization-induced offset between the cap layer and the position of the hole charge centroid is also illustrated.

was employed to explain the features of the $C-V$ characteristics and of the apparent doping profiles and to assess the theoretical limits of the characterization method. The method itself relies on direct low frequency and high frequency $C-V$ measurements and on simple analytical calculations. It allows for the accurate extraction of the threshold voltages of the corresponding MOSFET, of the valence band offset and Si cap layer thickness. Possible sources of error in the extracted value of the valence band offset were identified and discussed. It is instrumental for the ultimate success of the characterization technique that high frequency and low frequency measurements be carried out in conjunction, so that errors due to interface traps be removed.

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