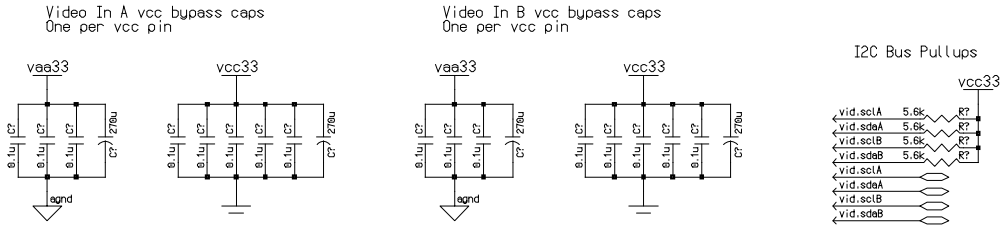
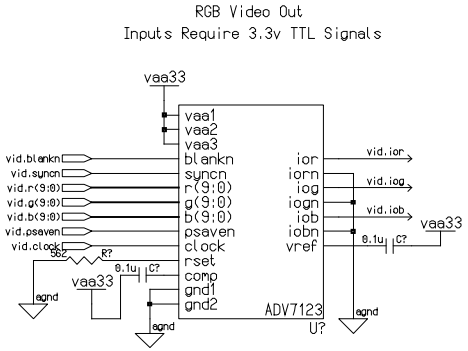
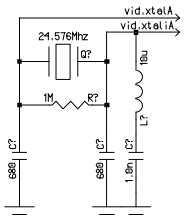
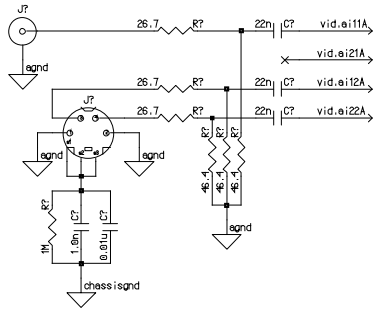
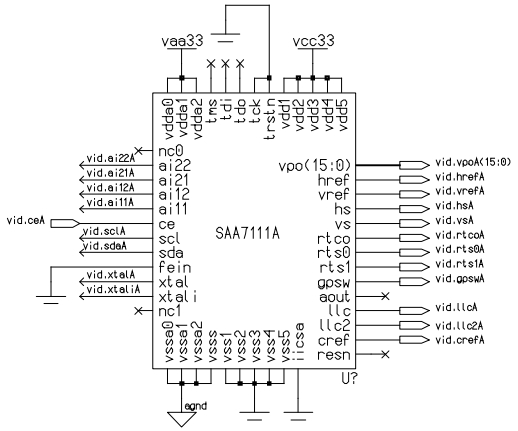
NTSC Video In/RGB Video Out

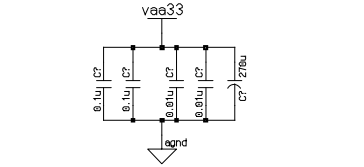


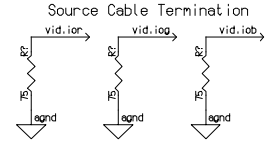


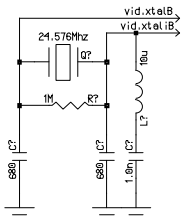


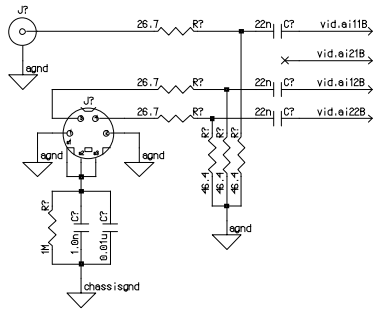


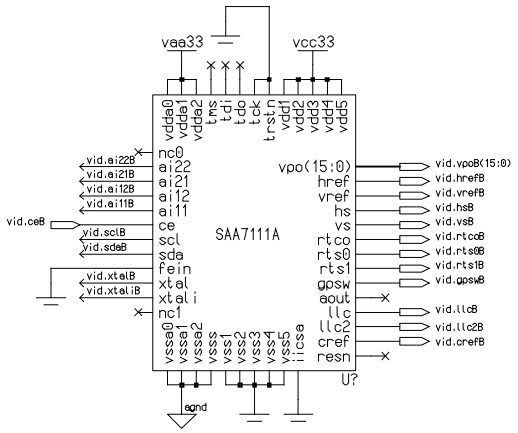


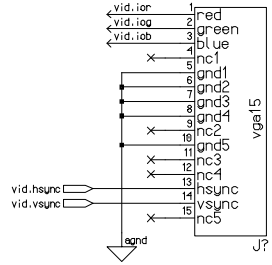










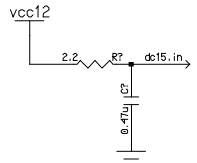


TM-4

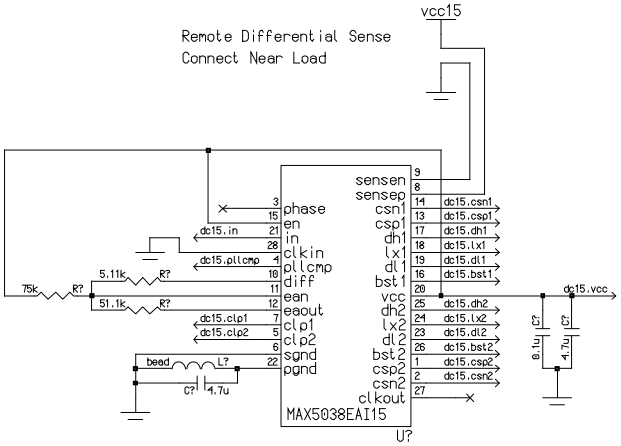
Joshua Fender
University of Toronto

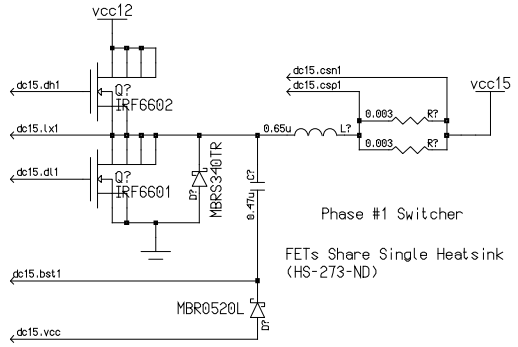
DC-DC Converter (1.5v 50A)

MAX5038 Power Supply Filter

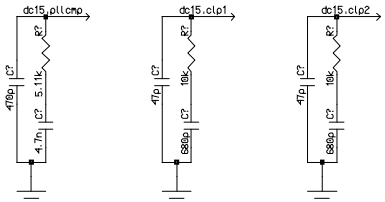


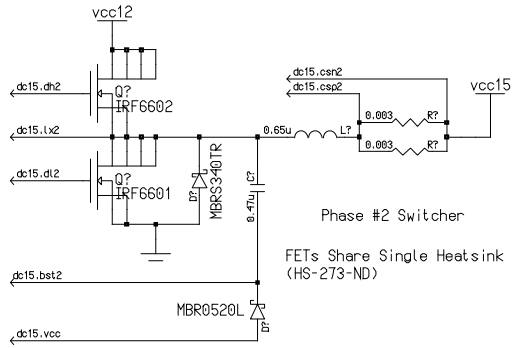
Remote Differential Sense
Connect Near Load



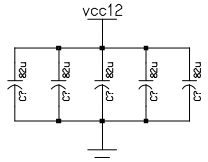


Compensation Networks

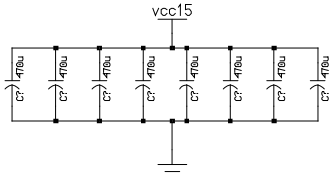




Decoupling Capacitors
Distribute Around Highside FETs



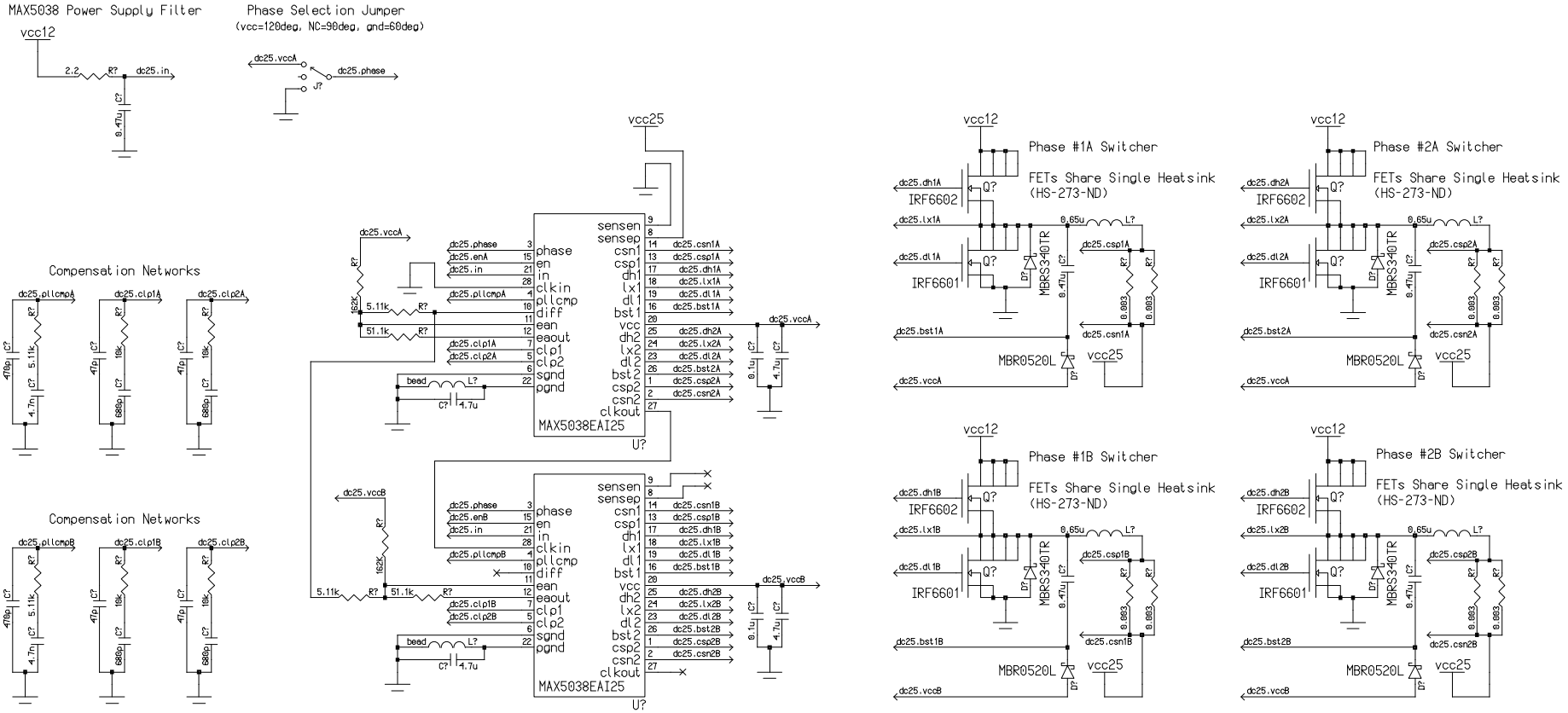
Bulk Holdup Capacitors
Distribute Around 1.5v Loads



TM-4

Joshua Hester
University of Toledo

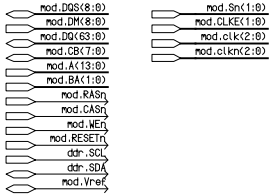
DC-DC Converter (2.5v 100A Peak)



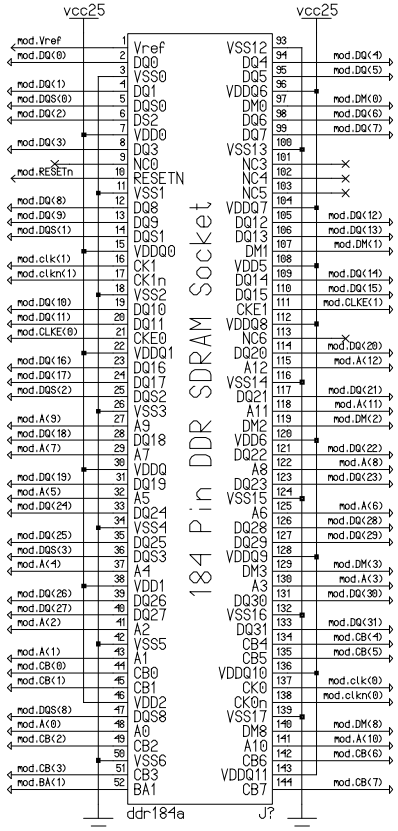
TM-4

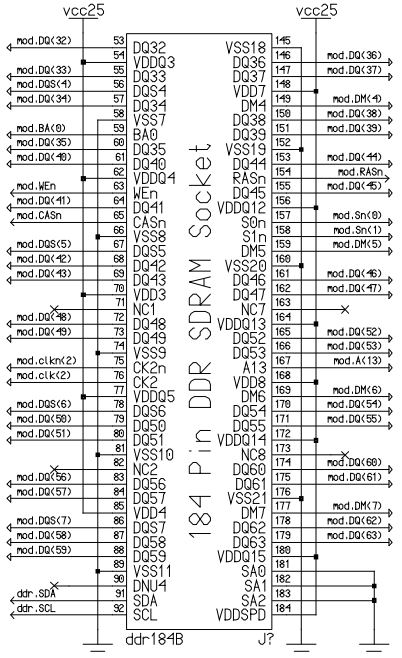
Jason Fredett
University of Toronto

DDR Module Sockets



DDR SDRAM 184 Pin Socket A



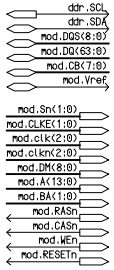


SPD Address (000)

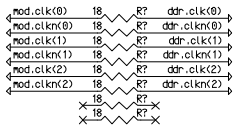
TM-4

Joshua Fender
University of Toronto

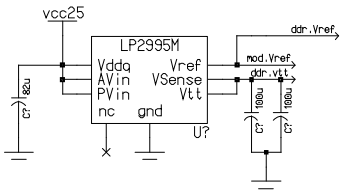
DDR Termination Regulator / Clock Buffer / Termination



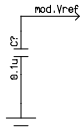
Differential Clock Series Termination



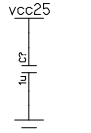
Termination Regulator



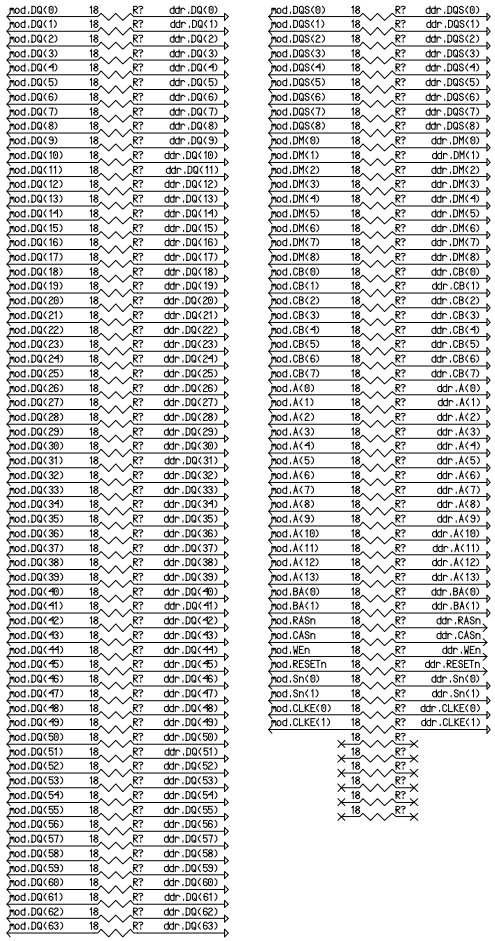
Vref Bypass Caps



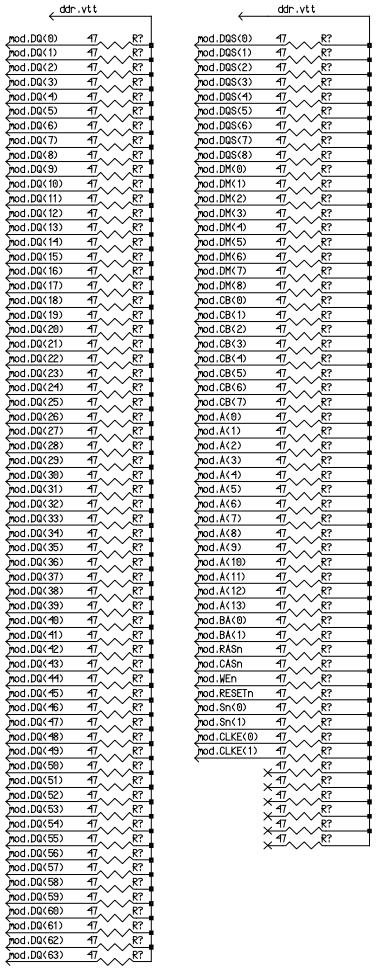
SPD Bypass Caps



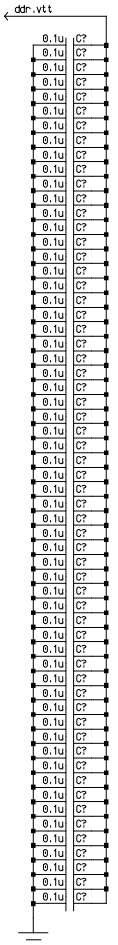
SSTL-2 Series Termination



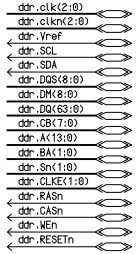
SSTL-2 Parallel Termination
Place After Last Socket



SSTL-2 Termination Bypass
1 Per 2 Termination Res



Top Level Ports



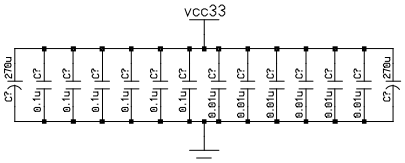
Termination Resistor's Values Are Placeholders
Pending Board Level Simulation

TM-4

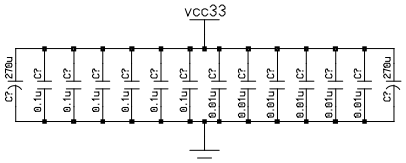
Joshua Fender
University of Toronto

Development FPGA Bypass Capacitors

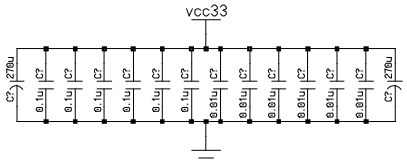
FPGA0 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



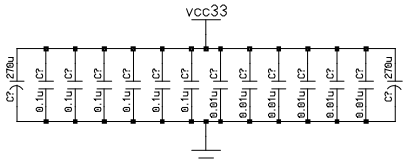
FPGA1 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



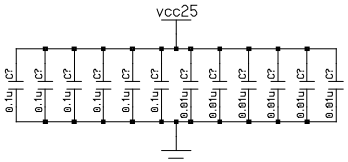
FPGA2 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



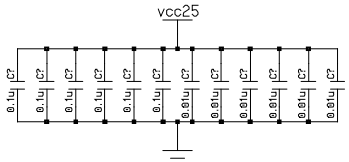
FPGA3 Banks 1,2,5,6 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



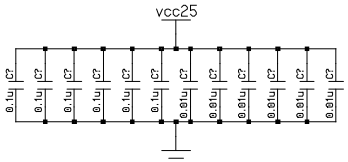
FPGA0 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



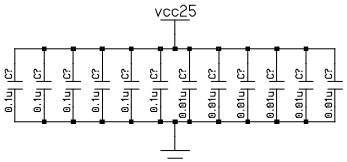
FPGA1 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



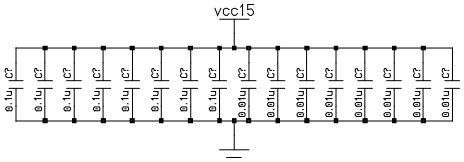
FPGA2 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



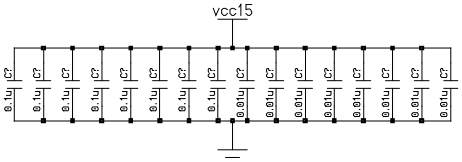
FPGA3 Banks 3,4,7,8 vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side



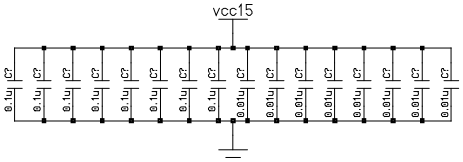
FPGA0 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



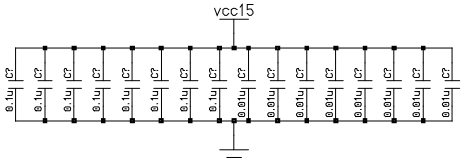
FPGA1 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



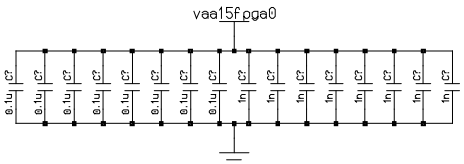
FPGA2 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



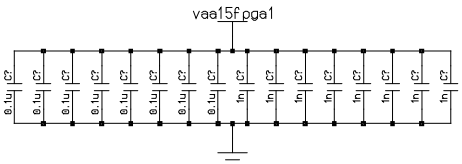
FPGA3 Vccint Bypass Caps 0603
Place near center of FPGA bottom side



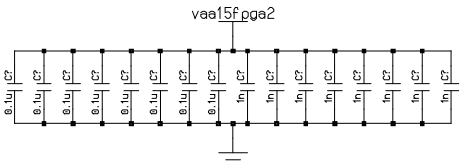
FPGA0 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



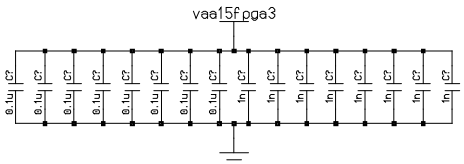
FPGA1 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



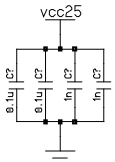
FPGA2 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



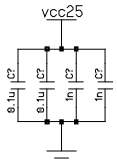
FPGA3 Vcca_pll Bypass Caps 0603
Place pair by each of 8 power pin groups



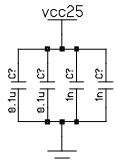
FPGA0 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



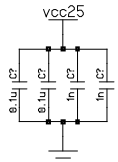
FPGA1 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



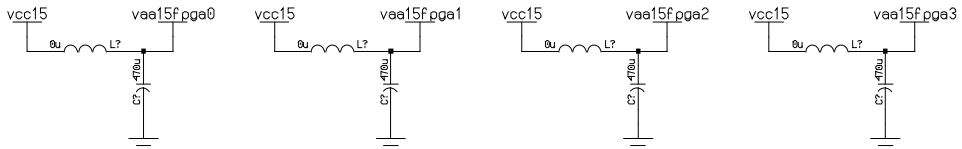
FPGA2 vcc_pll_out Bypass Caps 0805
Place pair by each of 2 power pin groups



FPGA3 vcc_pll_out Bypass Caps 0603
Place pair by each of 2 power pin groups



PLL Analog Supply Ferrite Beads and Bulk Caps



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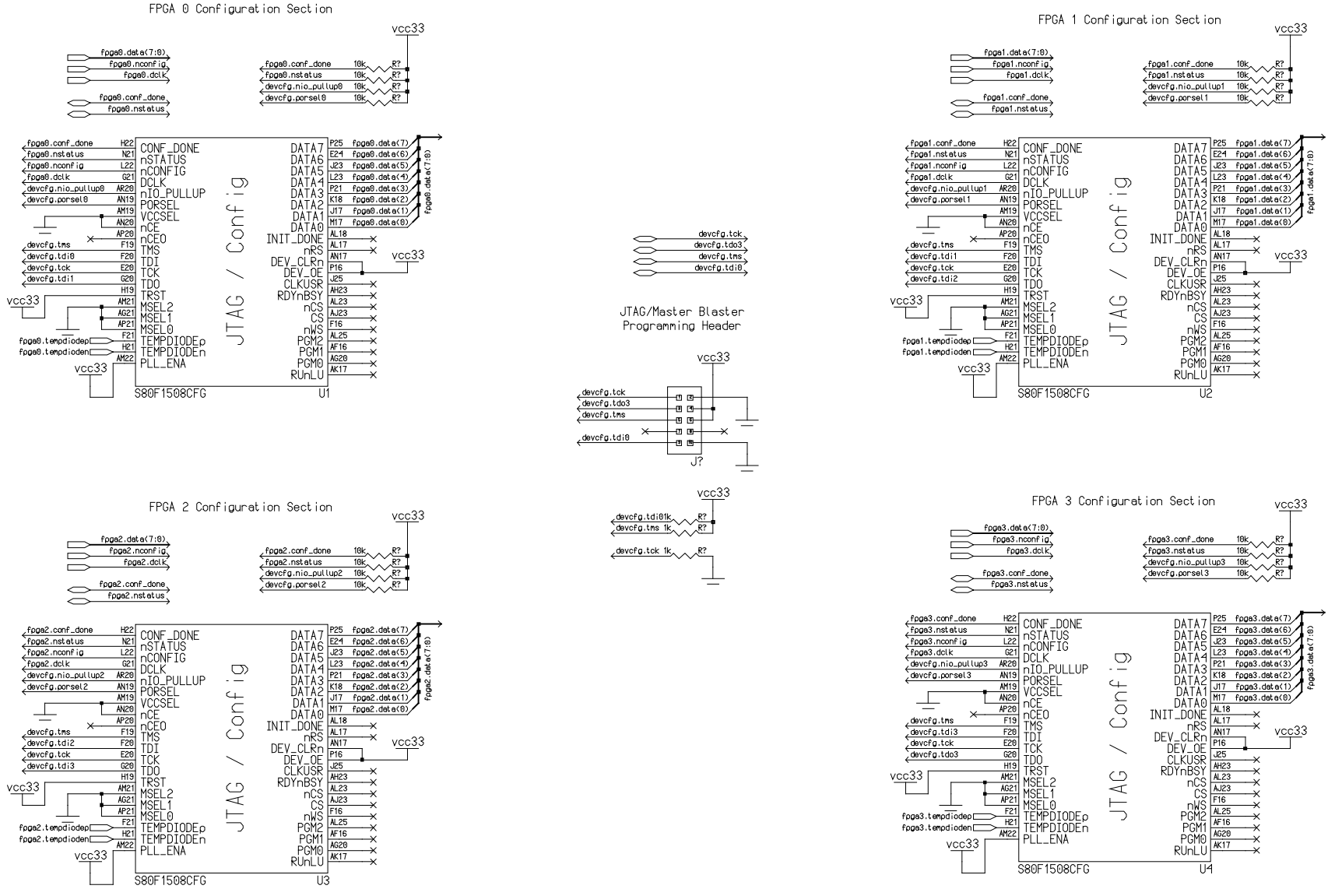
Josh Fender
University of Toronto

Development FPGA Configuration



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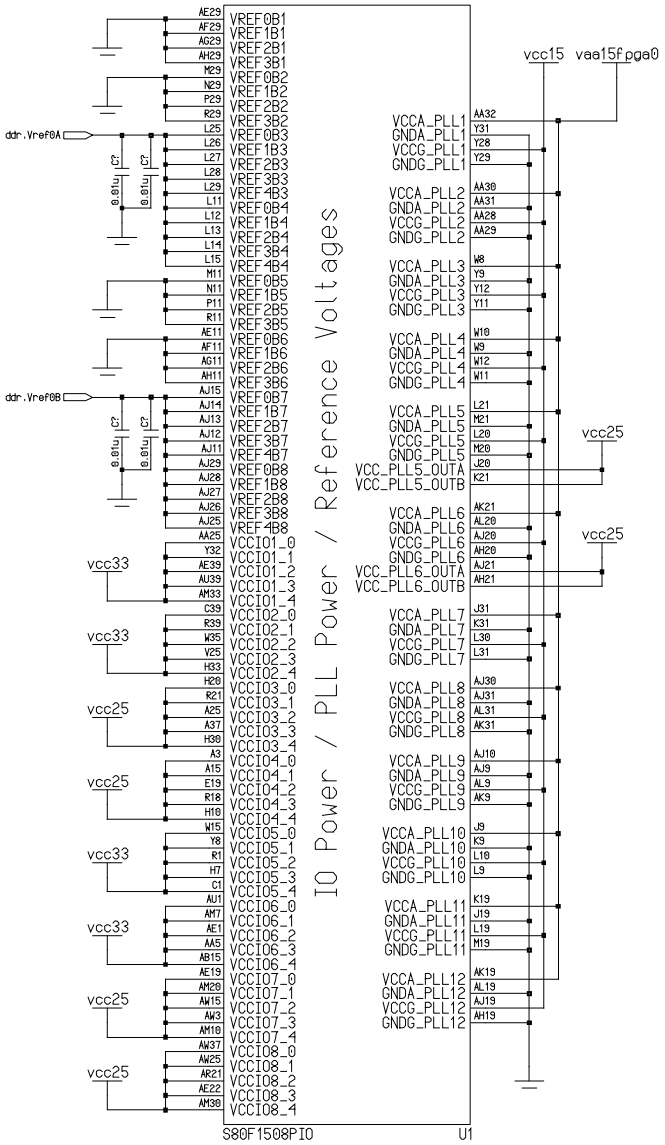
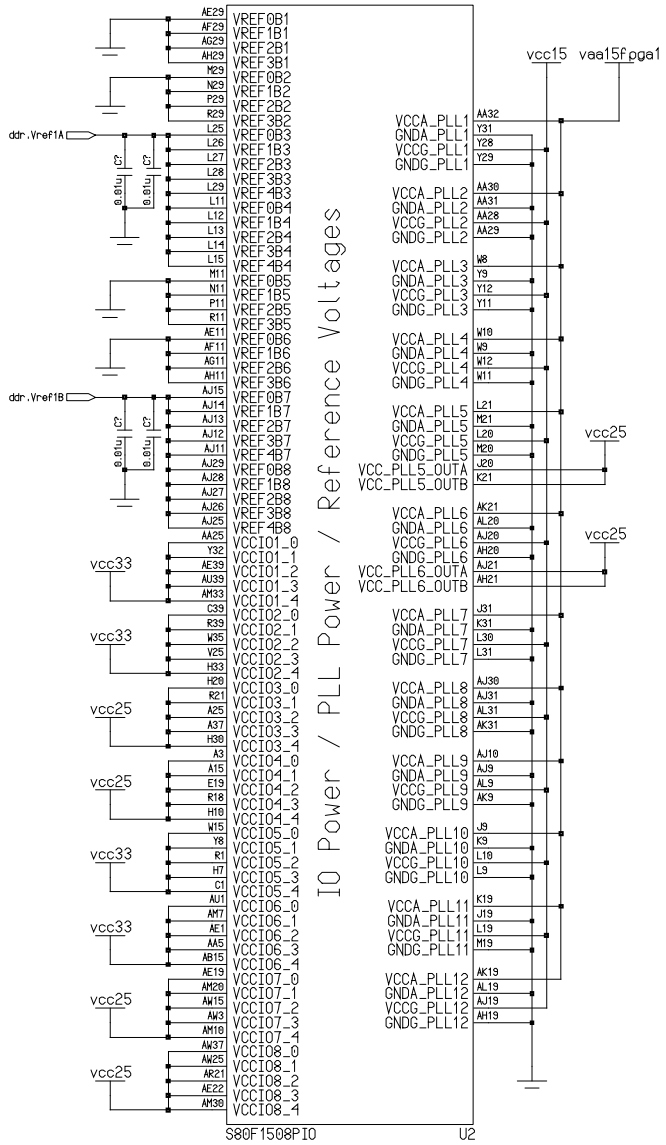
Development FPGAs 0, 1 IO/PLL Power & References





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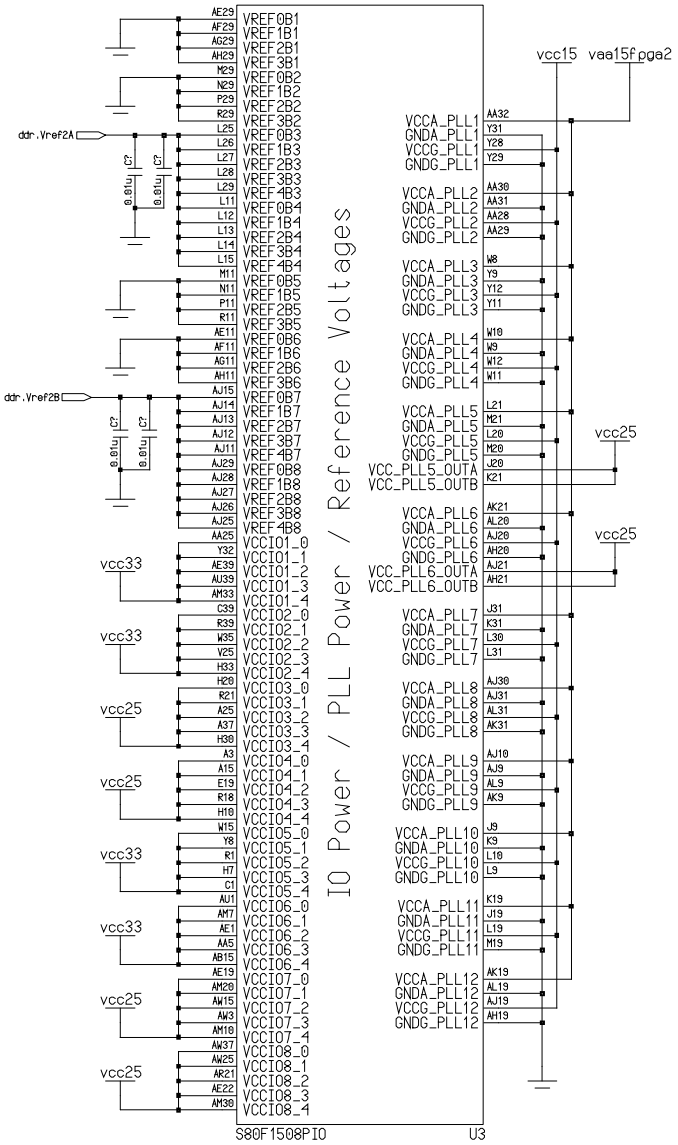
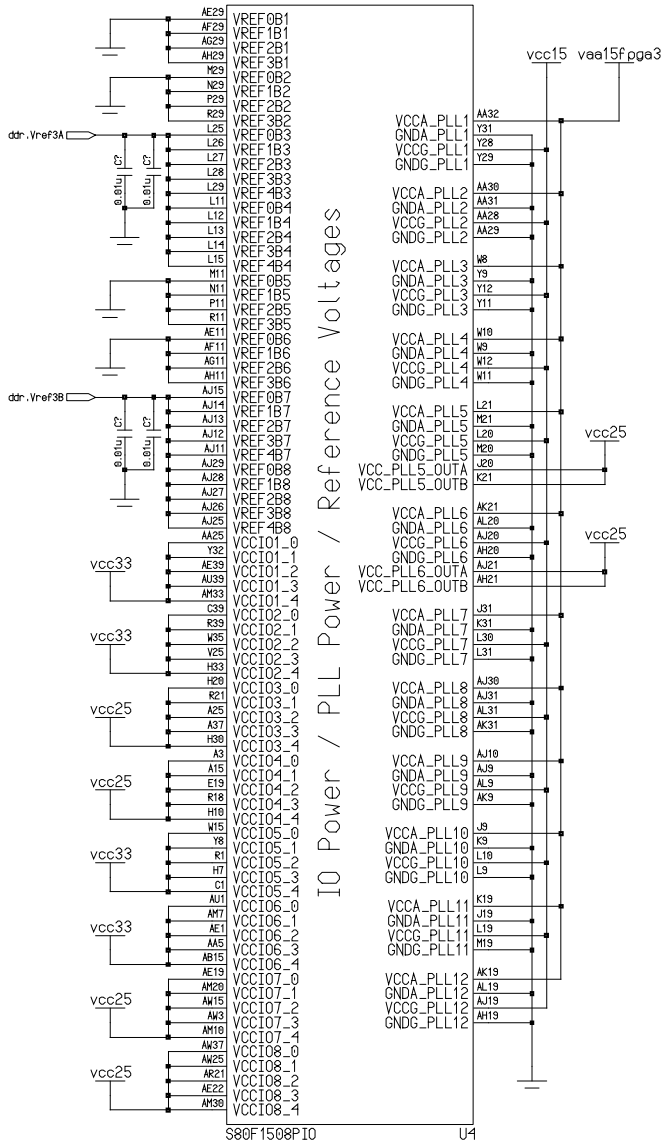
University of Toronto

Development FPGAs 2, 3 IO/PLL Power & References

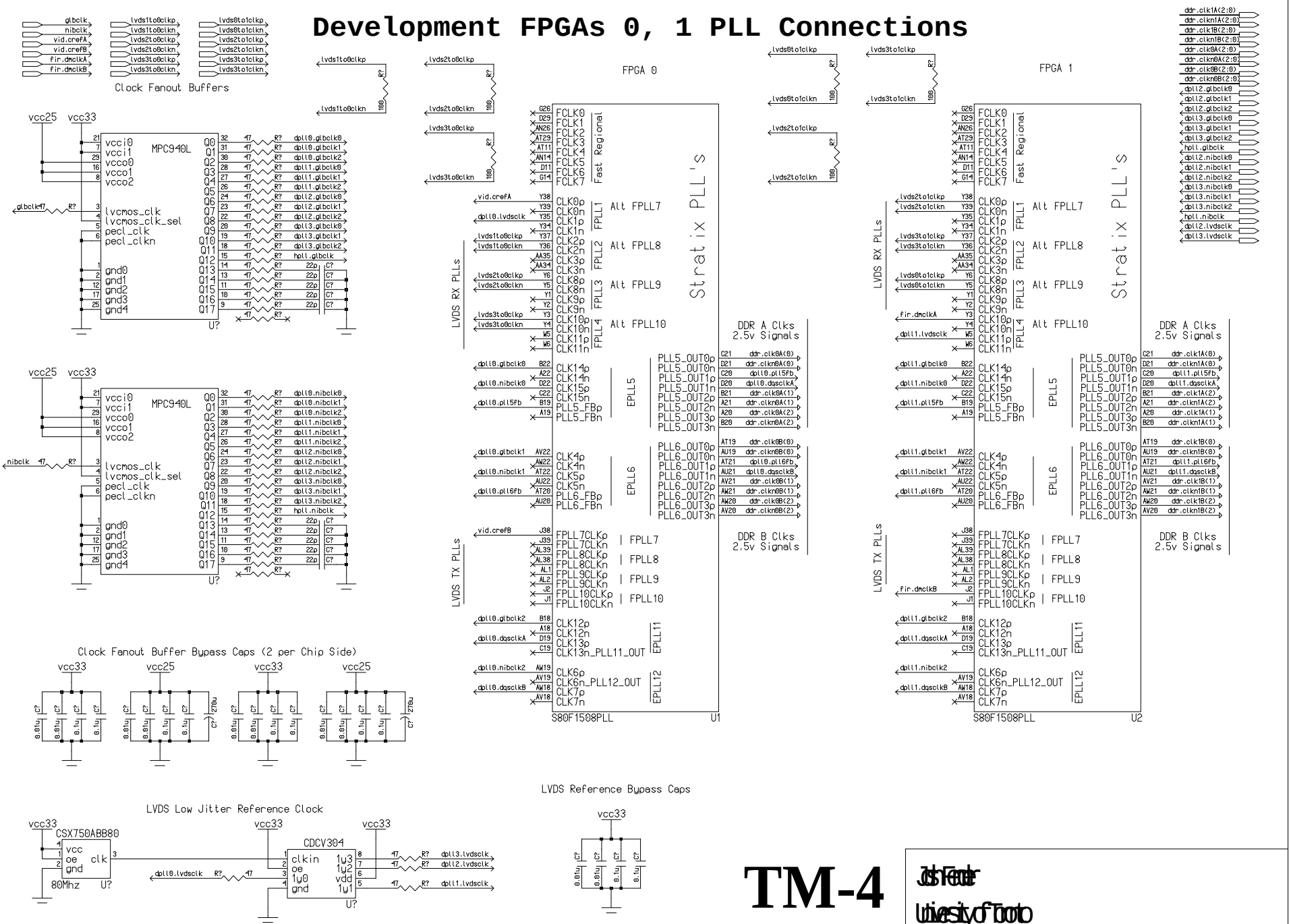




TM-4

Josh Fender
University of Toronto

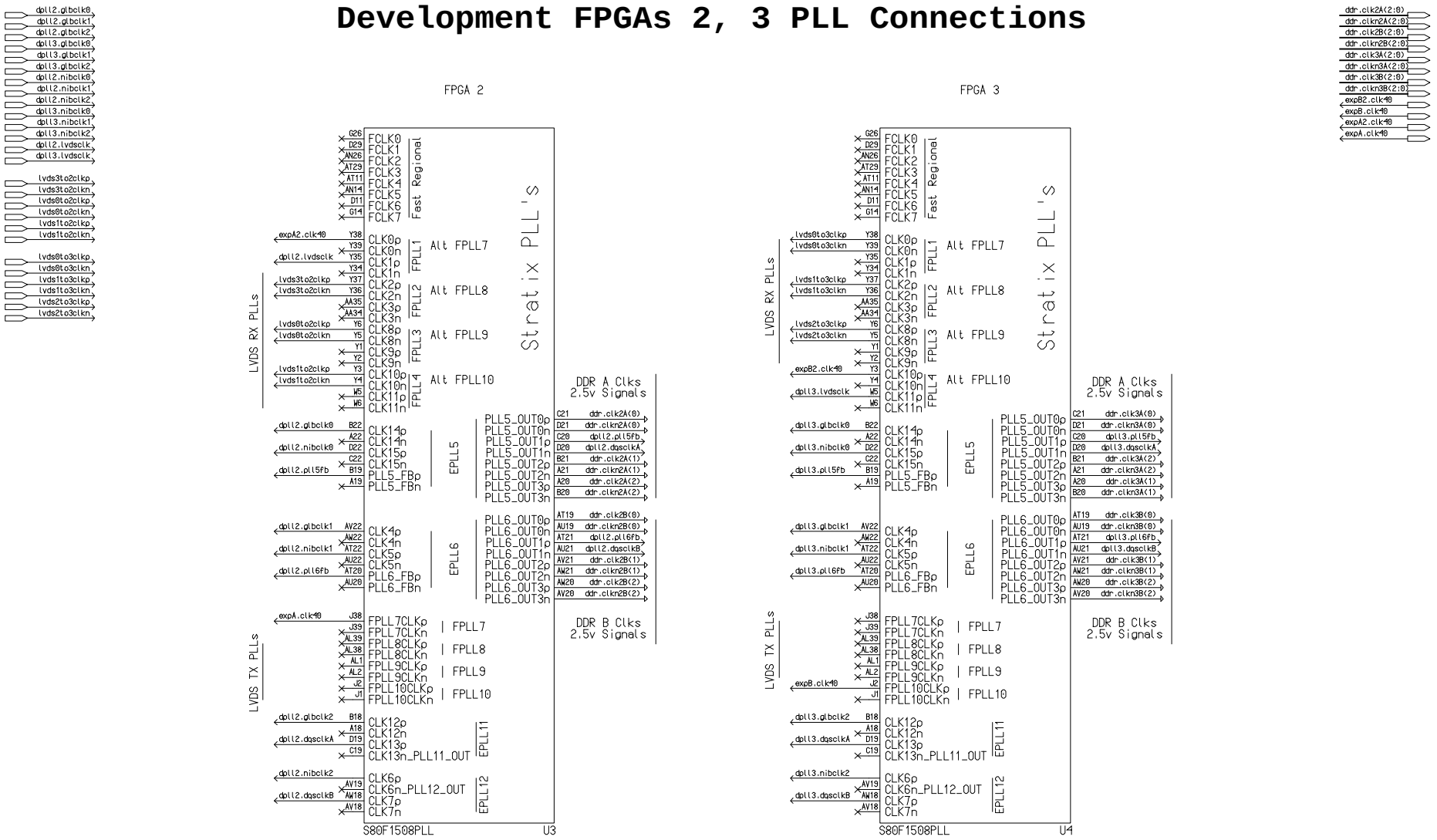
Development FPGAs 0, 1 PLL Connections



TM-4

Joshua Fender
University of Toronto

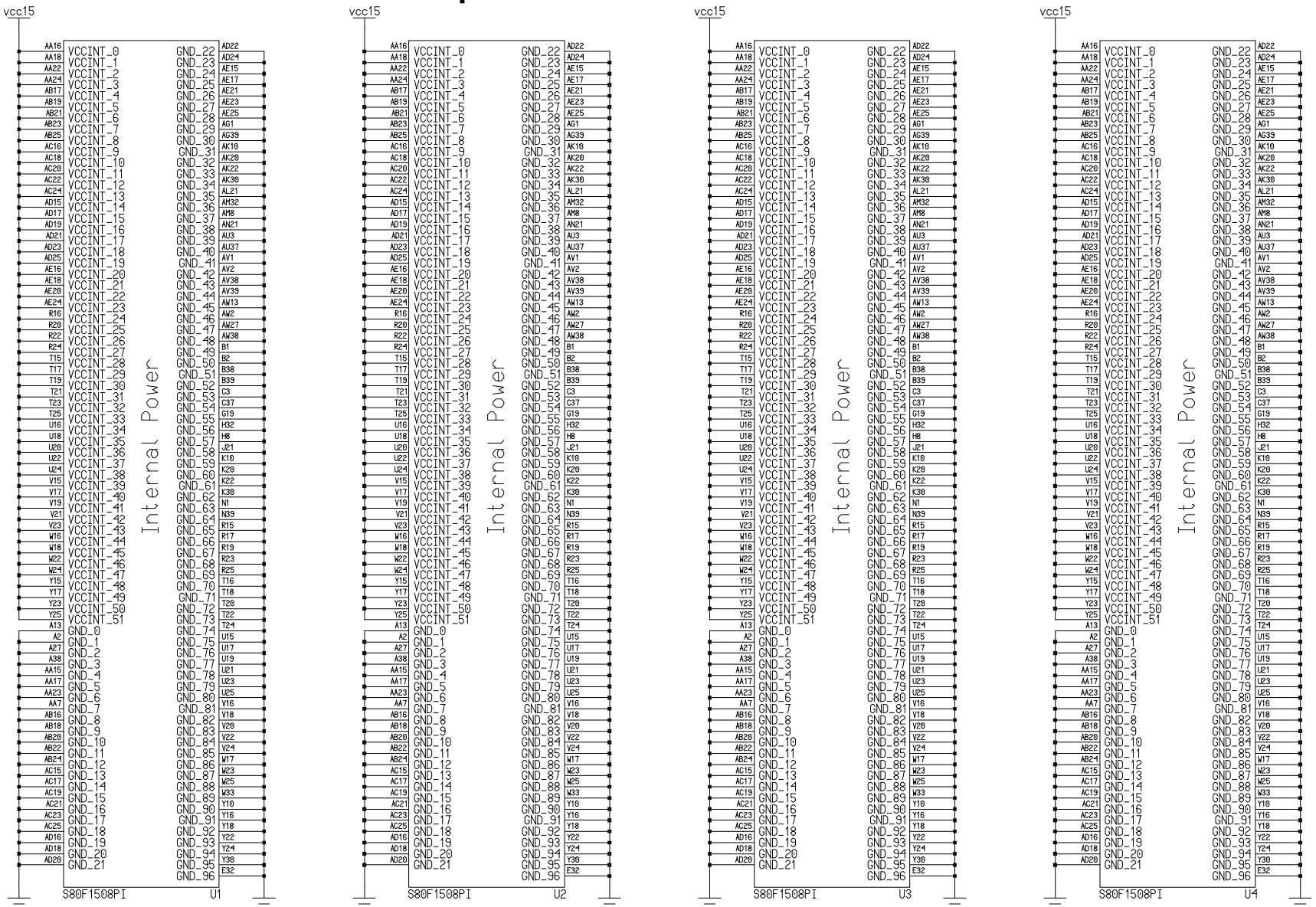
Development FPGAs 2, 3 PLL Connections



TM-4

Jason Fender
University of Toledo

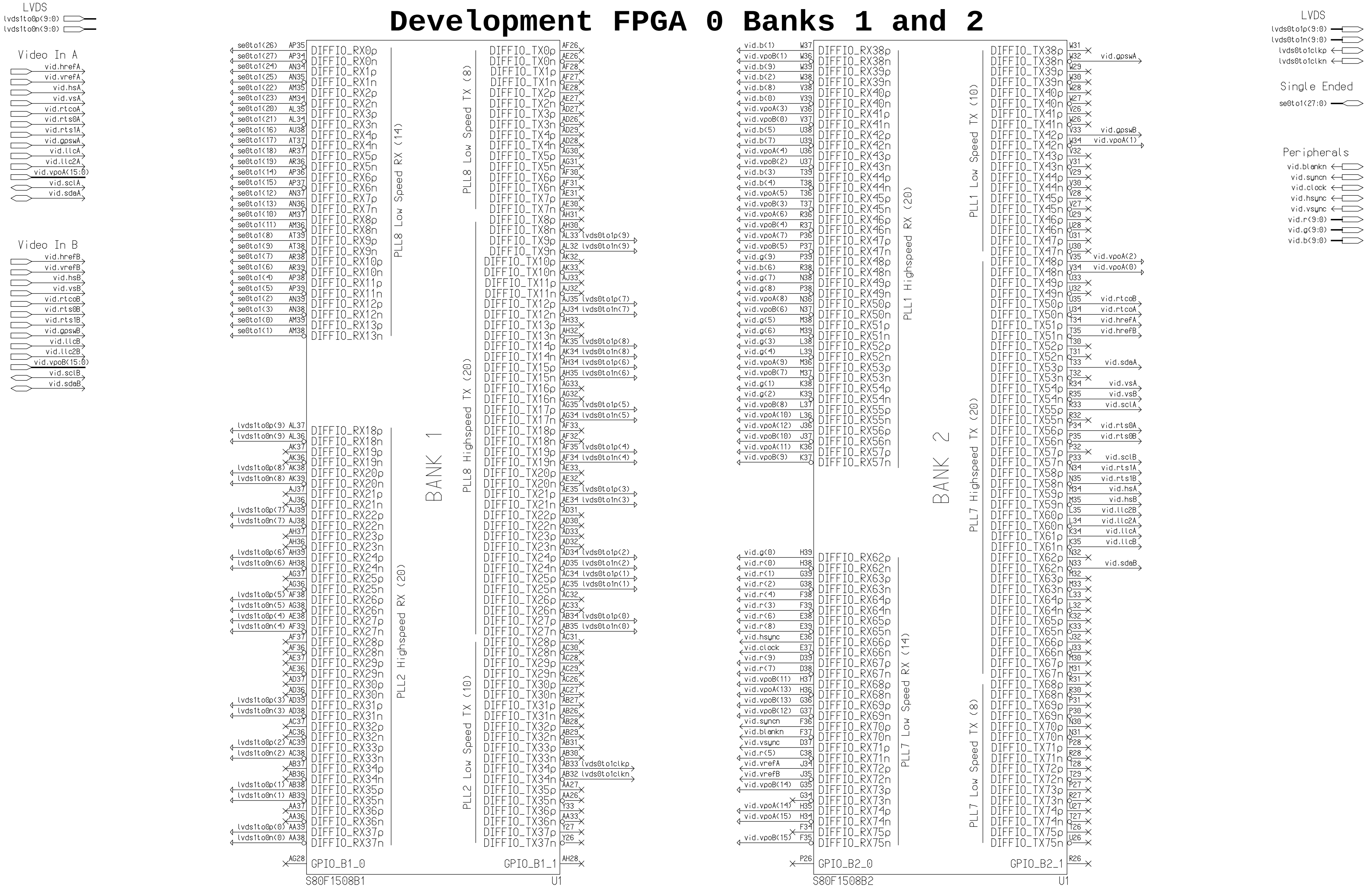
Development FPGAs Internal Power



TM-4

Joshua Fender
University of Toronto

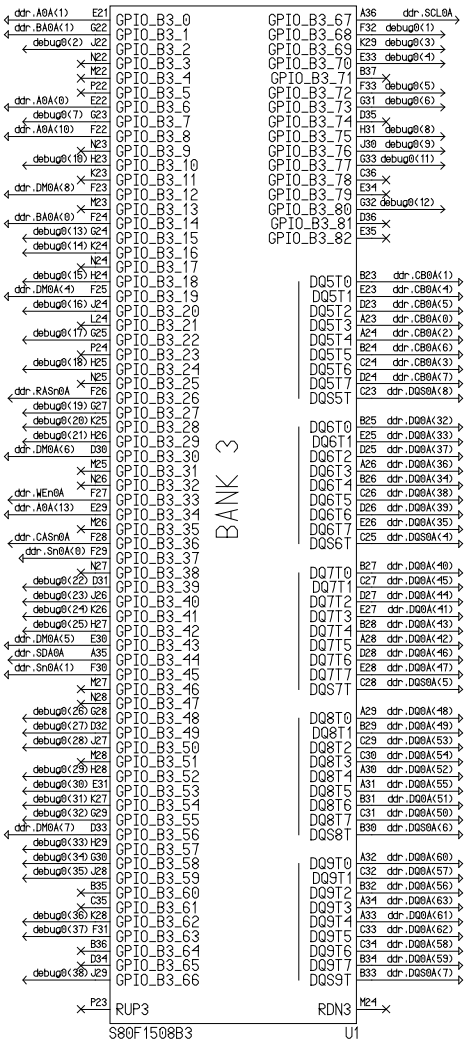
Development FPGA 0 Banks 1 and 2

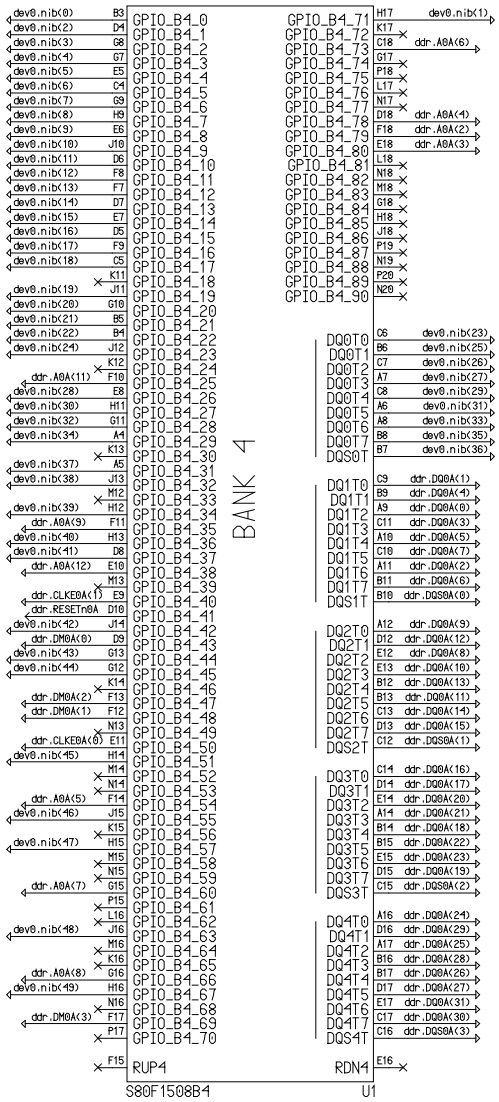


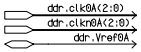
TM-4

Josh Fender
University of Toronto

Development FPGA 0 Banks 3 and 4

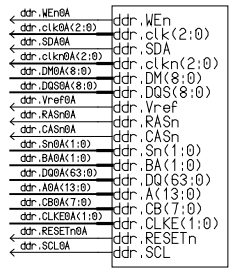




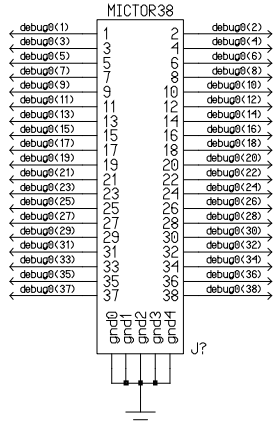


Nibble Bus

DDR SDRAM Bank A



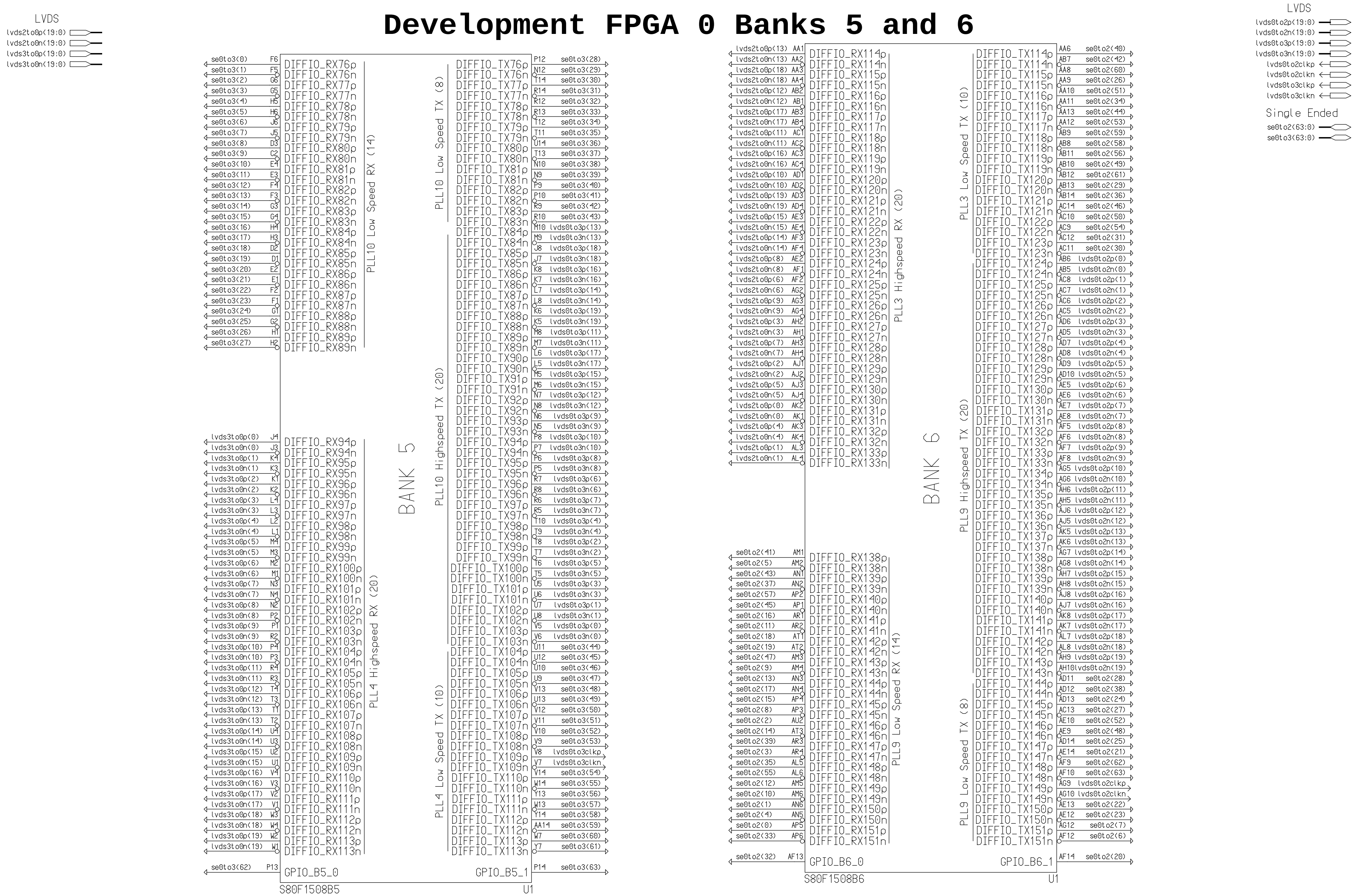
Logic Analyzer Connector



TM-4

Joshua Fender
University of Toronto

Development FPGA 0 Banks 5 and 6

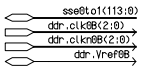


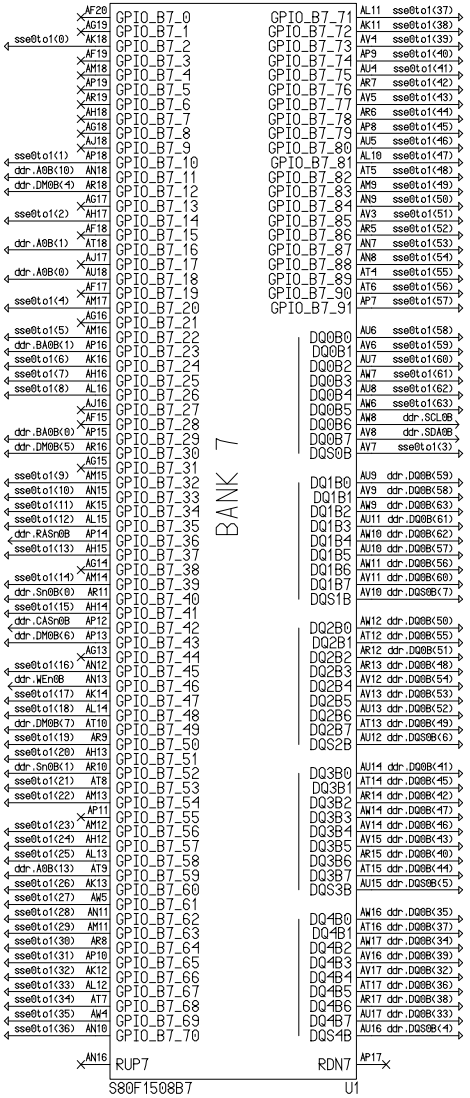
TM-4

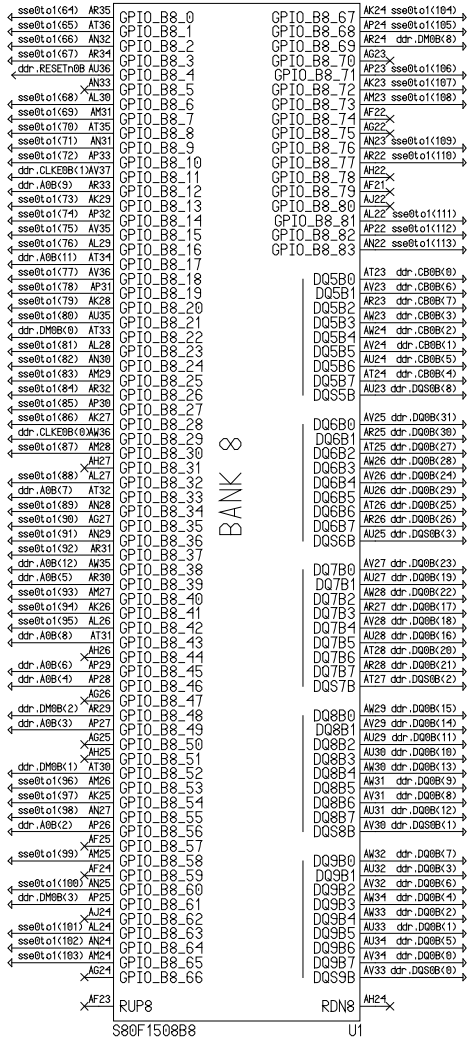
Josh Fender

University of Toronto

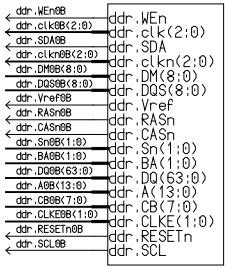
Development FPGA 0 Banks 7 and 8







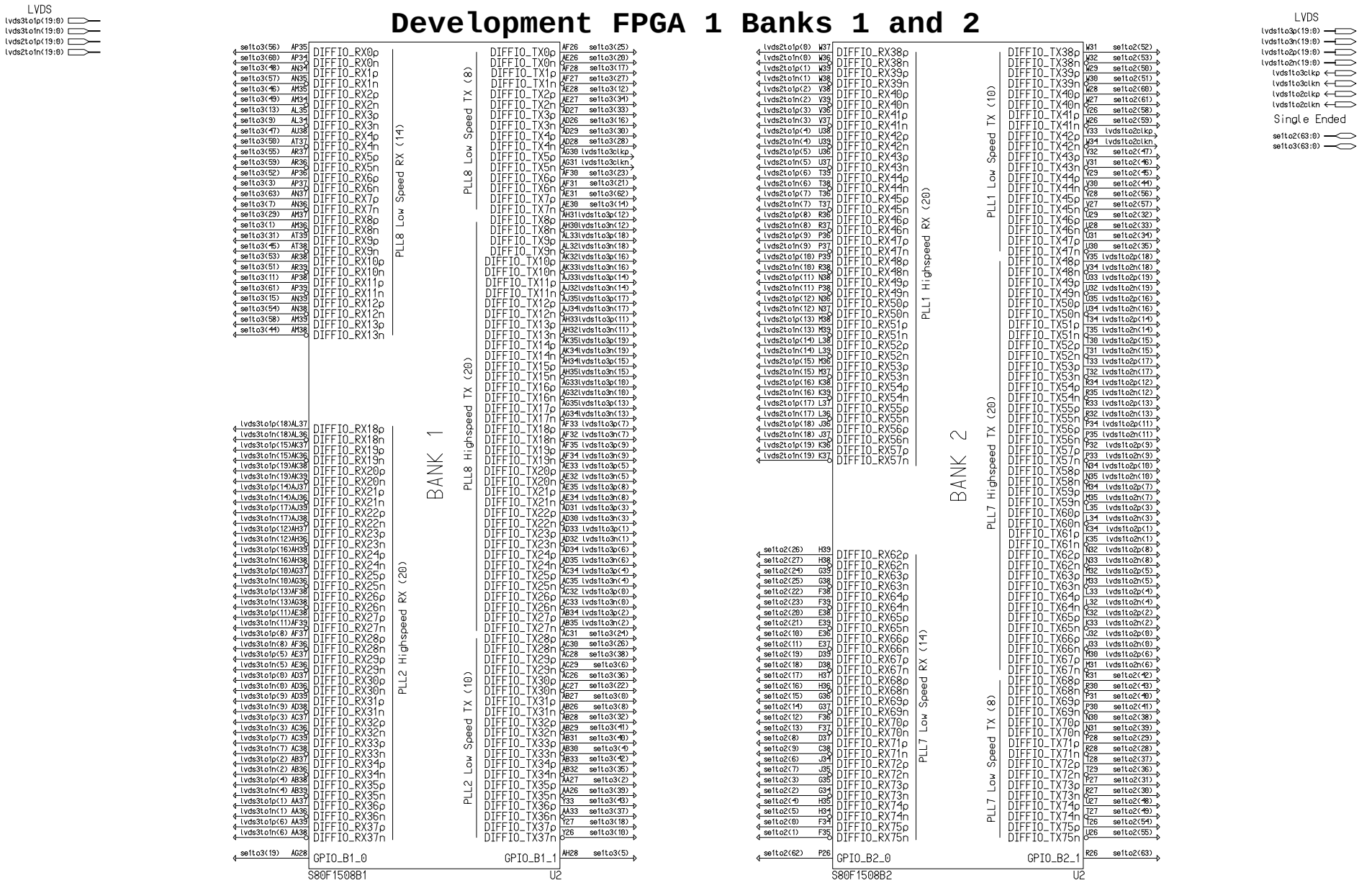
DDR SDRAM Bank B



TM-4

Jos Fortes
University of Florida

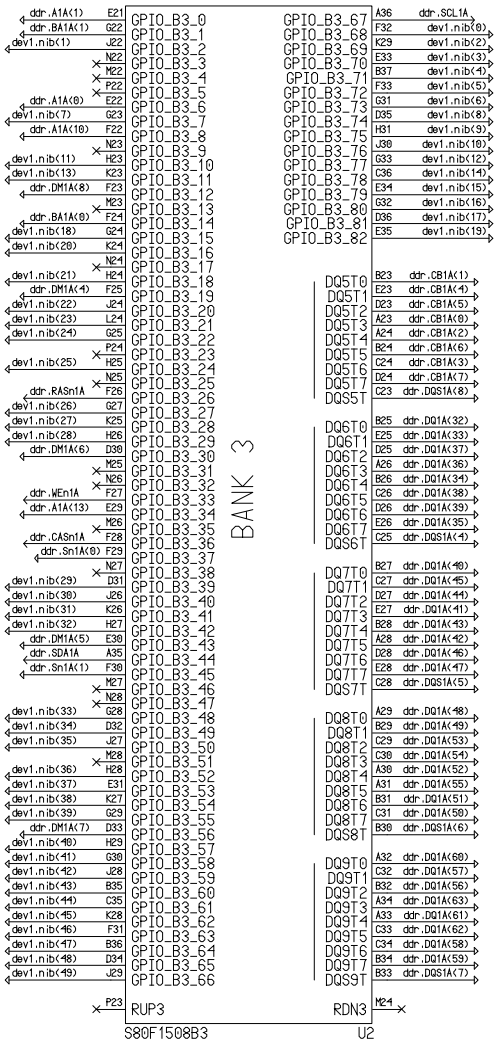
Development FPGA 1 Banks 1 and 2

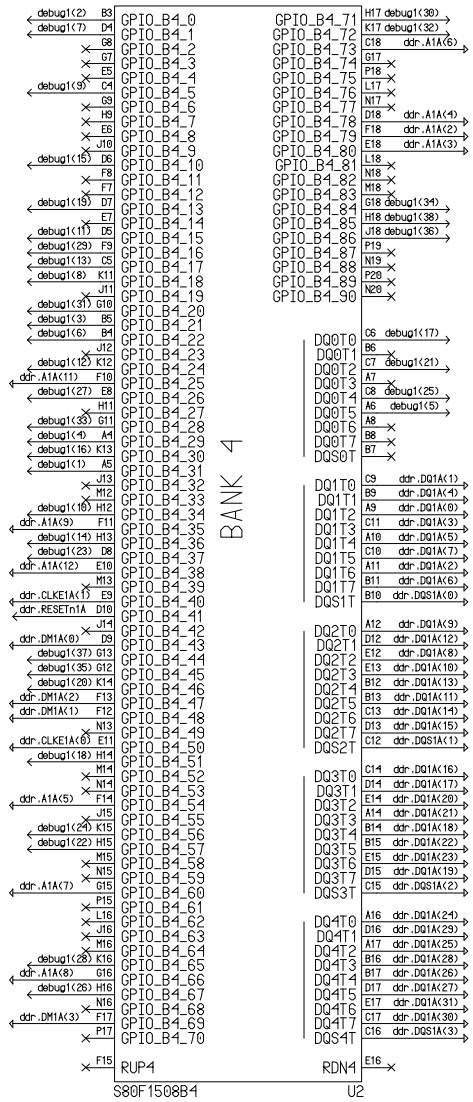


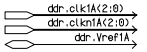
TM-4

Joshua Fender
University of Toronto

Development FPGA 1 Banks 3 and 4

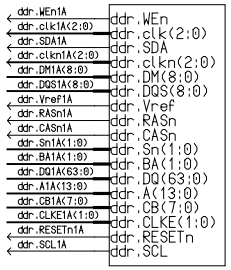






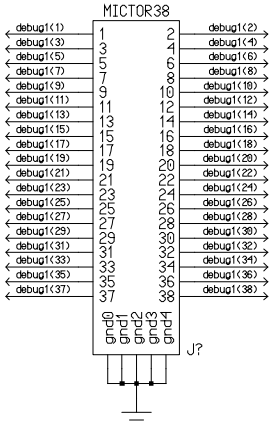
Nibble Bus

DDR SDRAM Bank A



debug1(38:1)

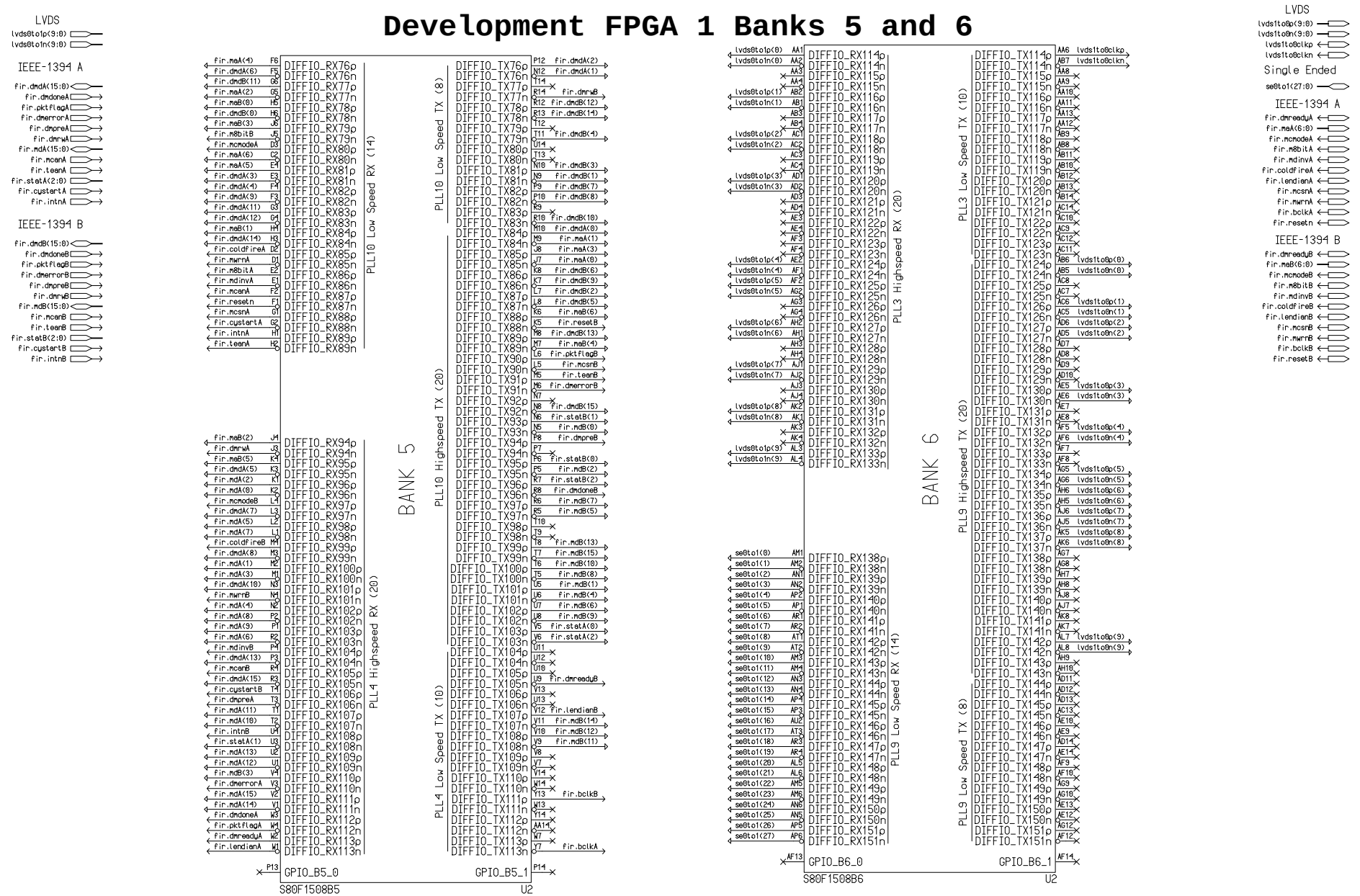
Logic Analyzer Connector



TM-4

Joshua Fender
University of Toledo

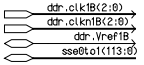
Development FPGA 1 Banks 5 and 6

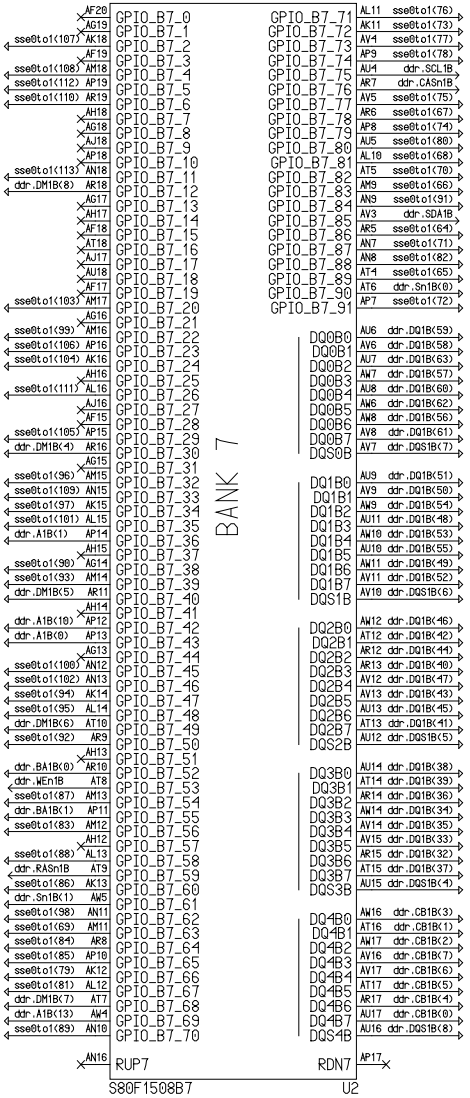


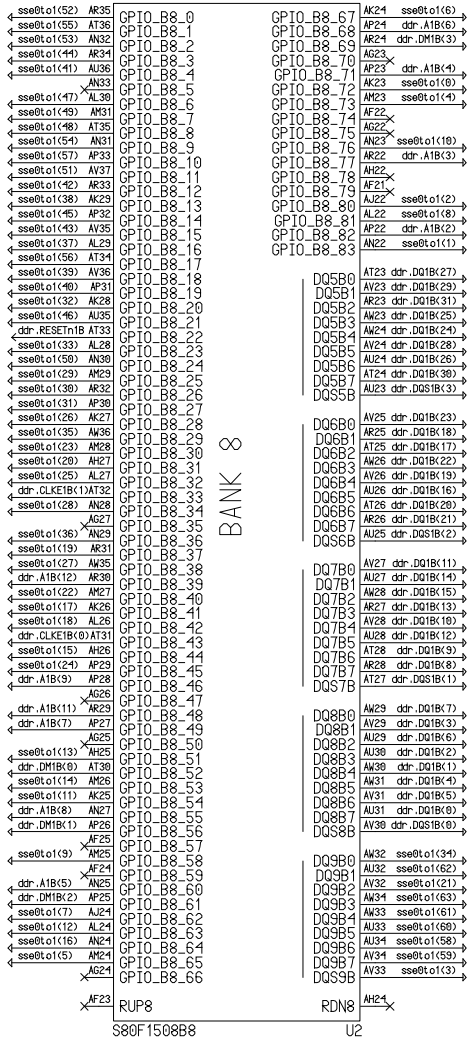
TM-4

Jonathan Hays
University of Toronto

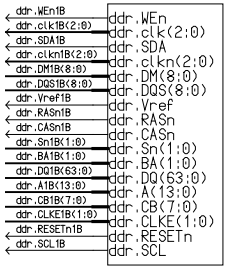
Development FPGA 1 Banks 7 and 8







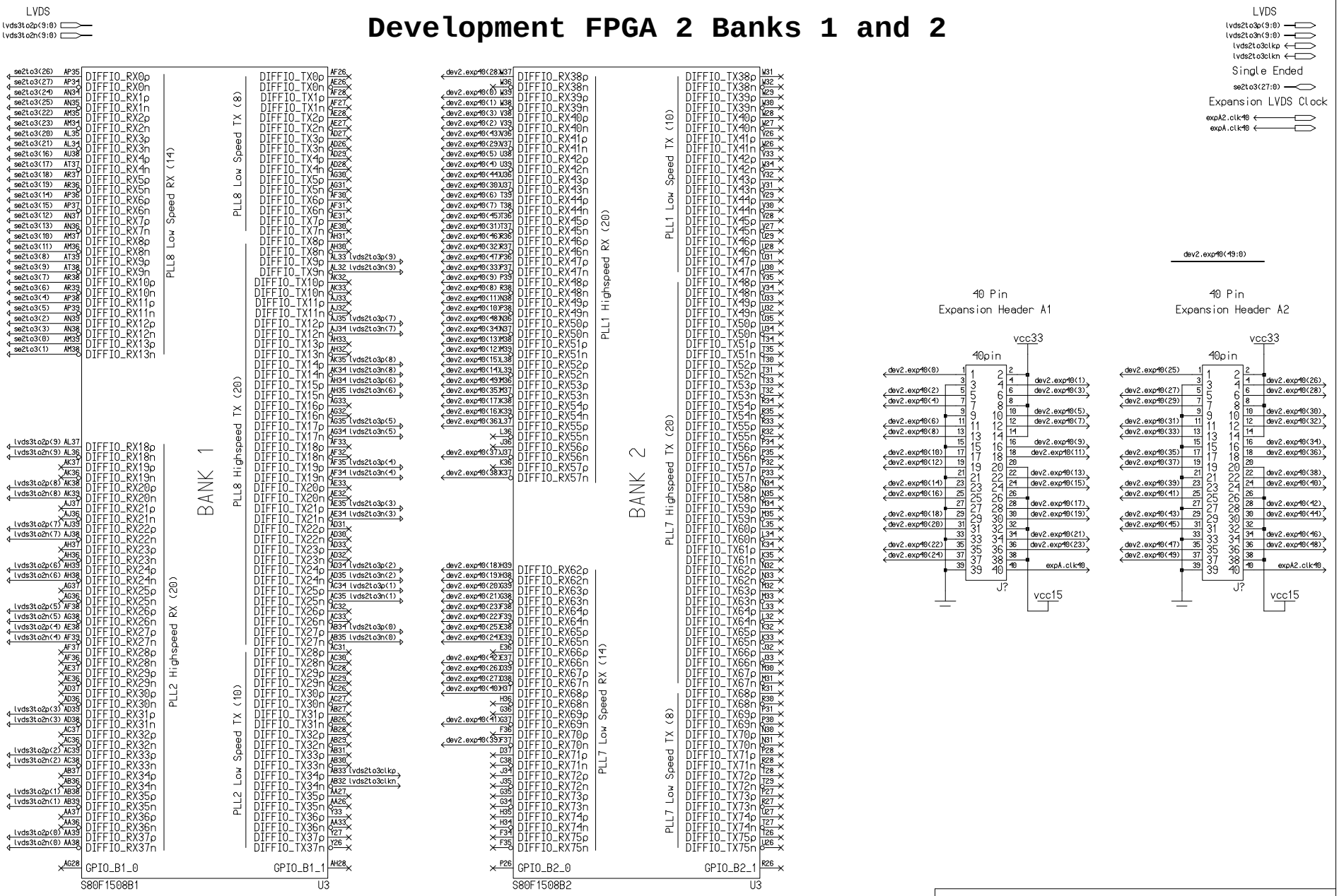
DDR SDRAM Bank B



TM-4

Jos Fortes
University of Florida

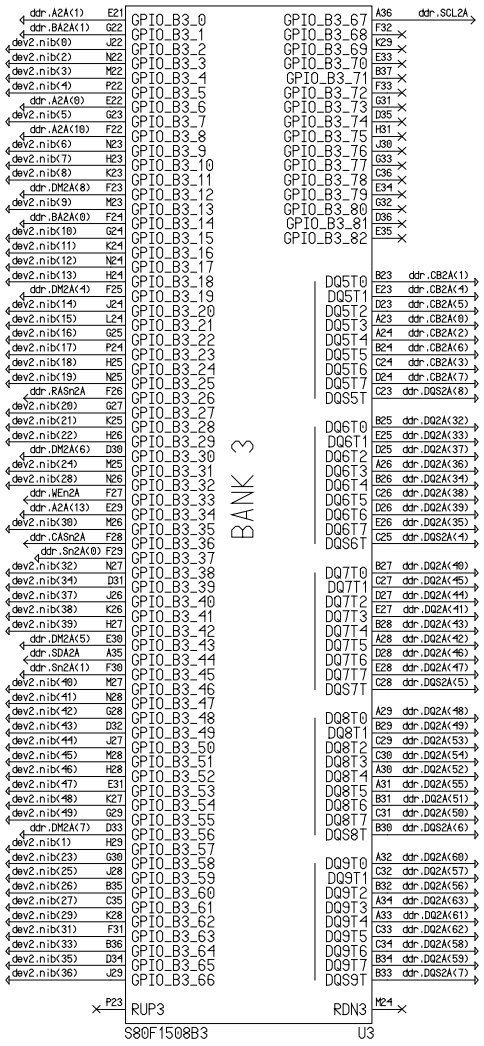
Development FPGA 2 Banks 1 and 2

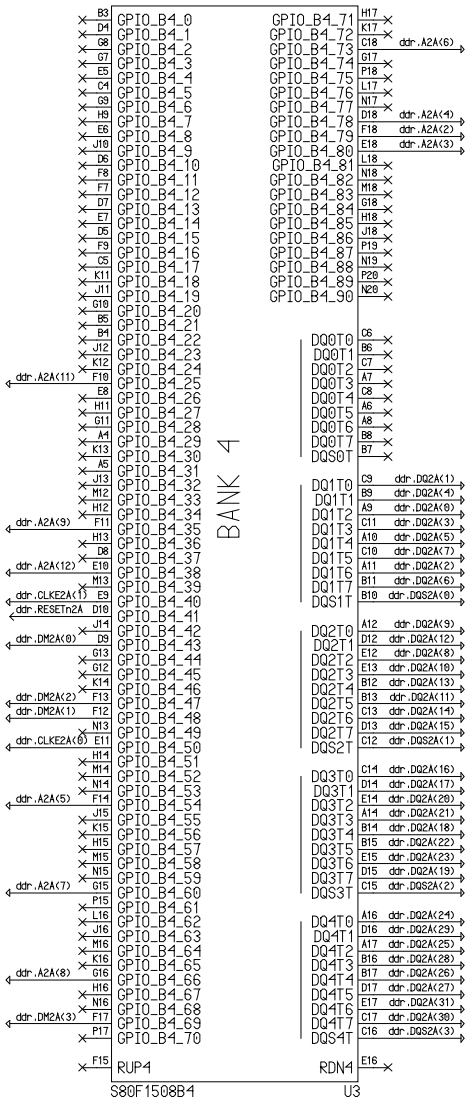


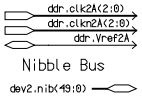
TM-4

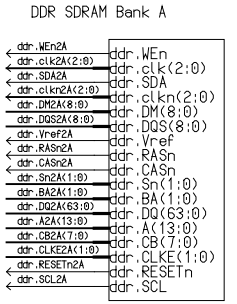
Jason Fredett
University of Toledo

Development FPGA 2 Banks 3 and 4





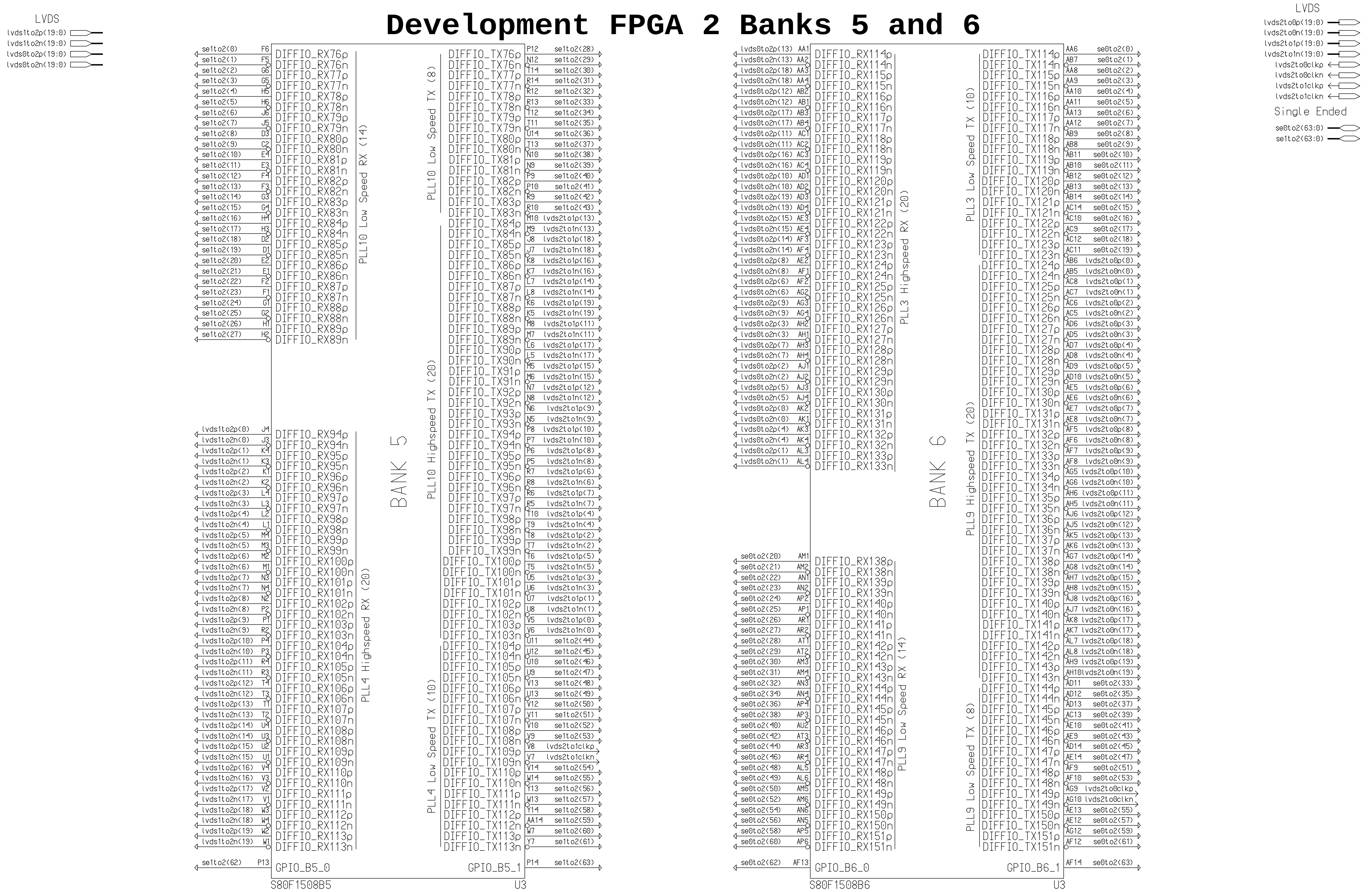




TM-4

Joshua Fender
University of Toronto

Development FPGA 2 Banks 5 and 6

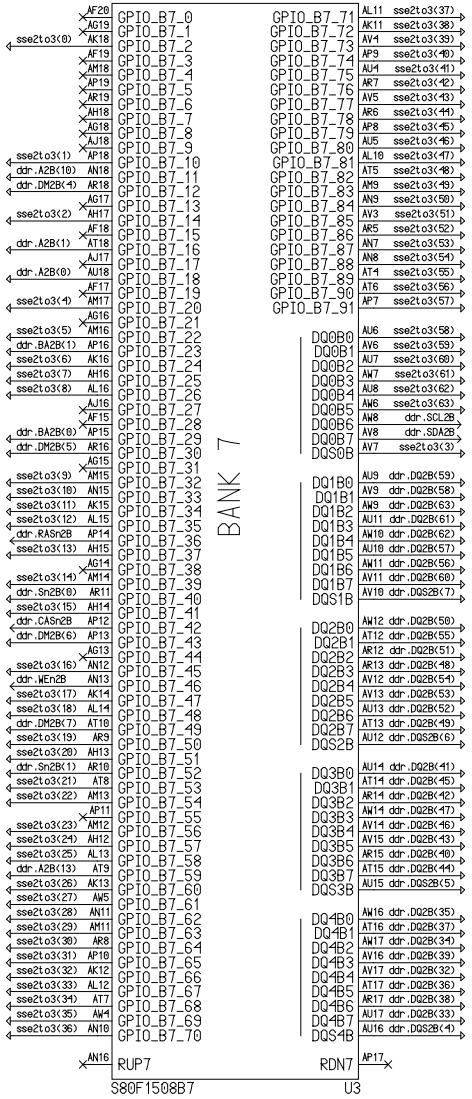


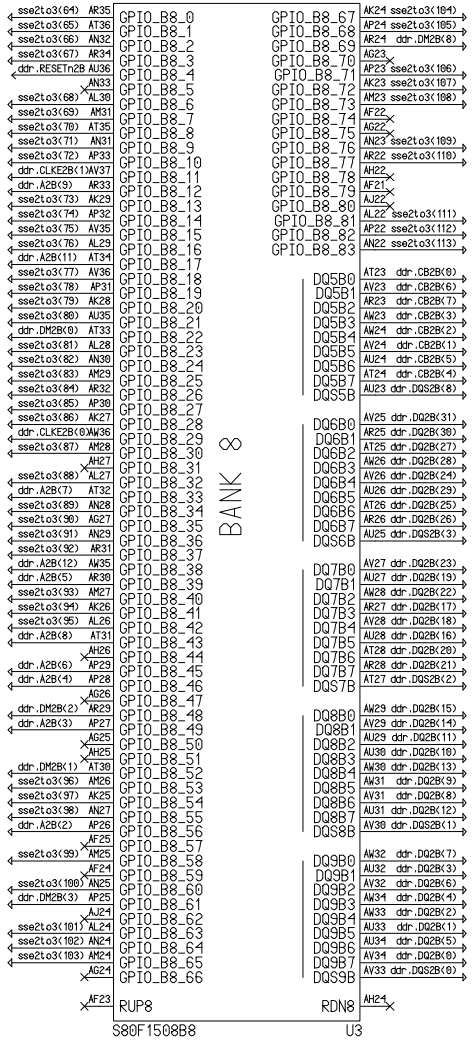
TM-4

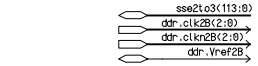
Josh Fender

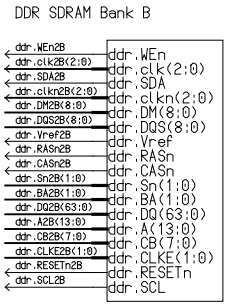
University of Toronto

Development FPGA 2 Banks 7 and 8





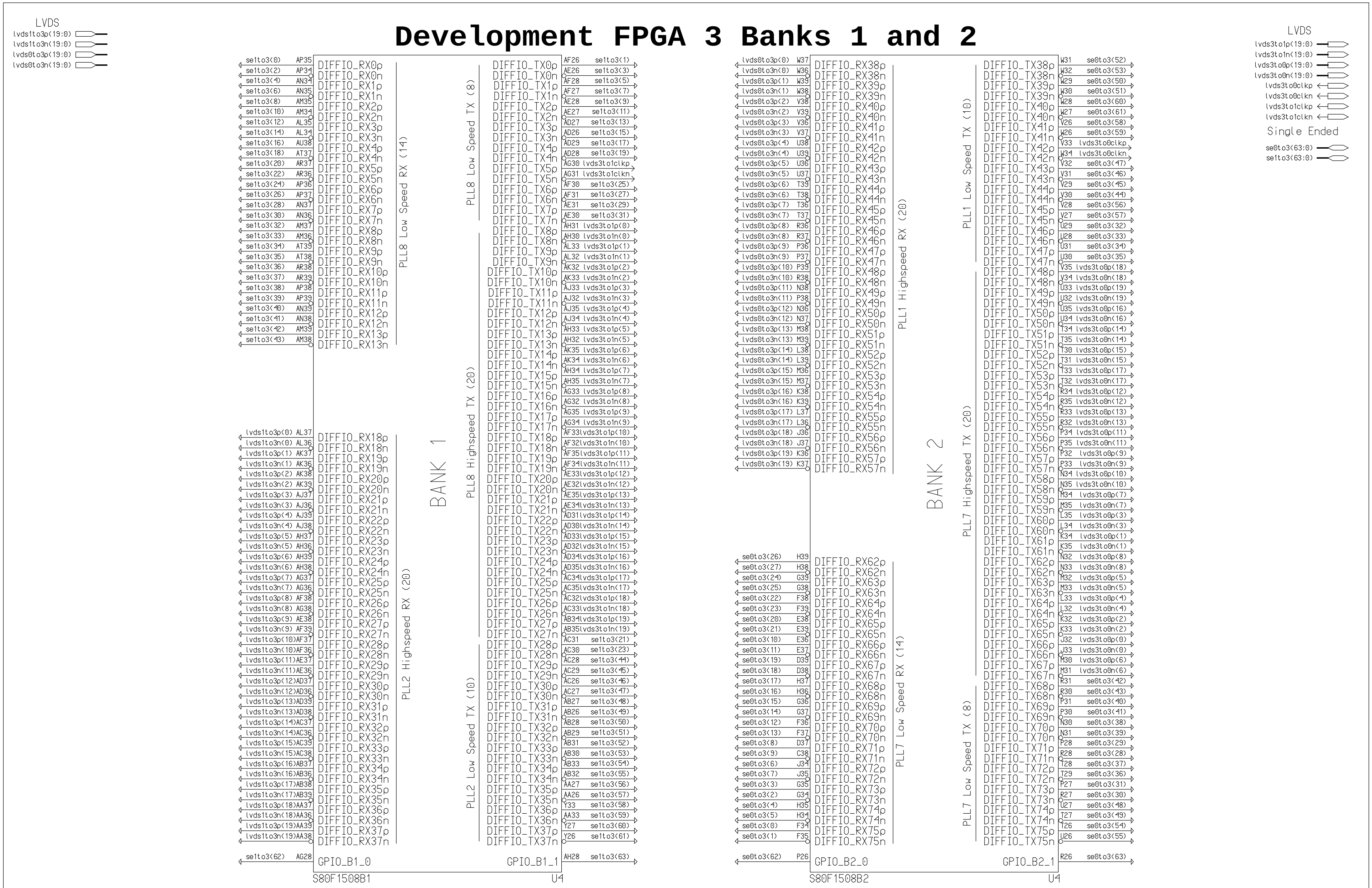




TM-4

Joshua Fender
University of Toronto

Development FPGA 3 Banks 1 and 2

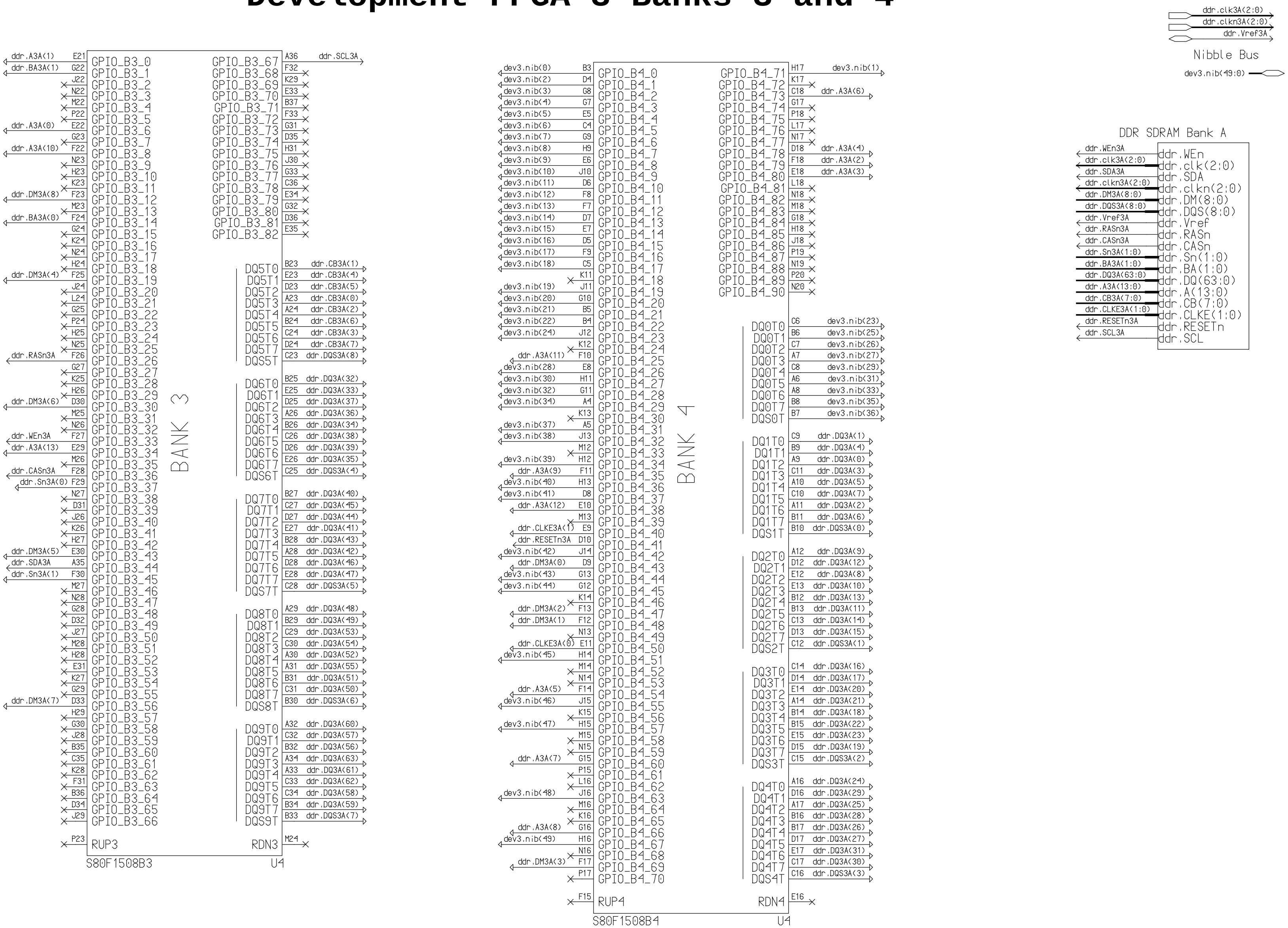


TM-4

Josh Fender

University of Toronto

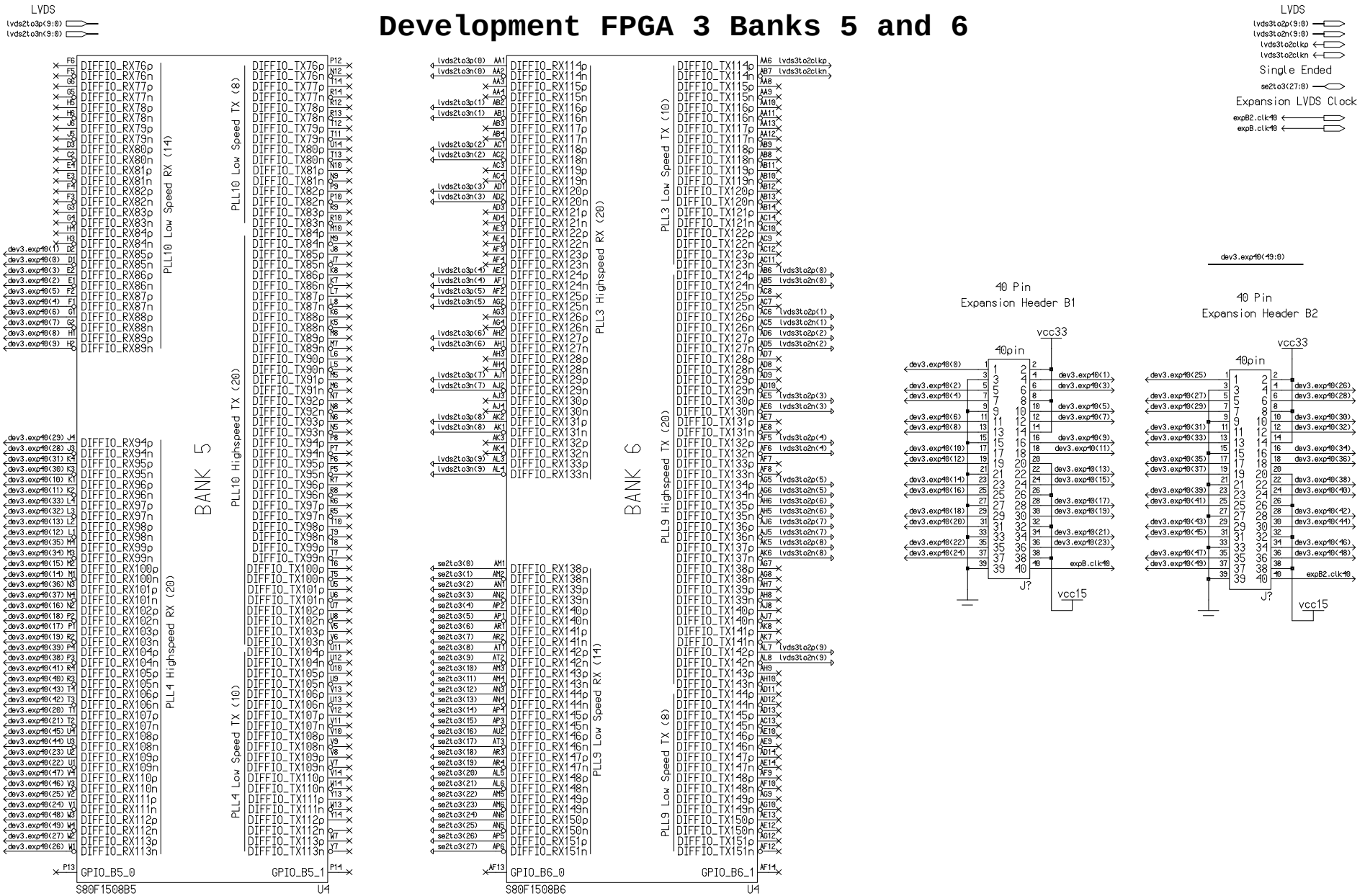
Development FPGA 3 Banks 3 and 4



TM-4

Josh Fender
University of Toronto

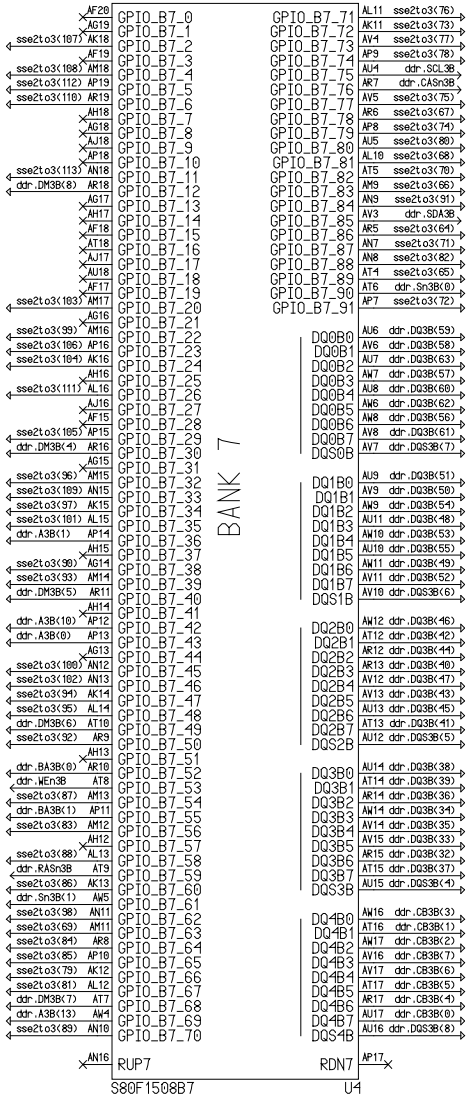
Development FPGA 3 Banks 5 and 6

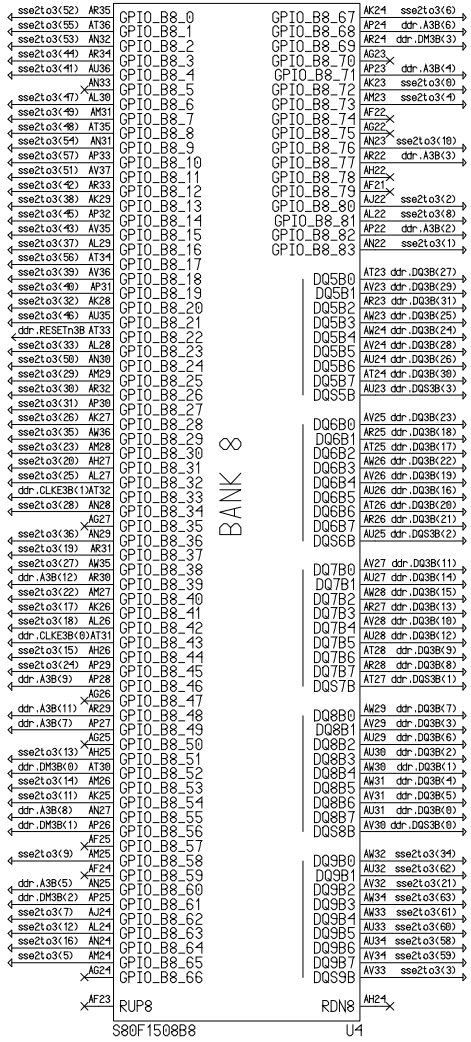


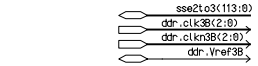
TM-4

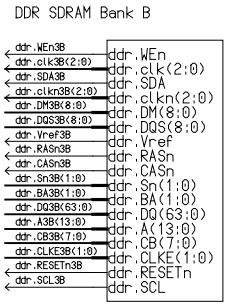
Josh Fender
University of Toronto

Development FPGA 3 Banks 7 and 8





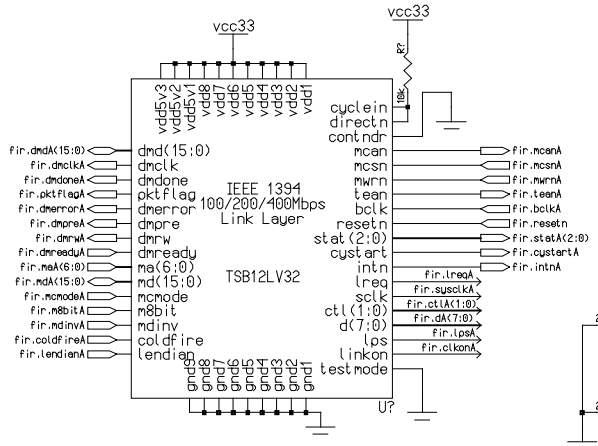


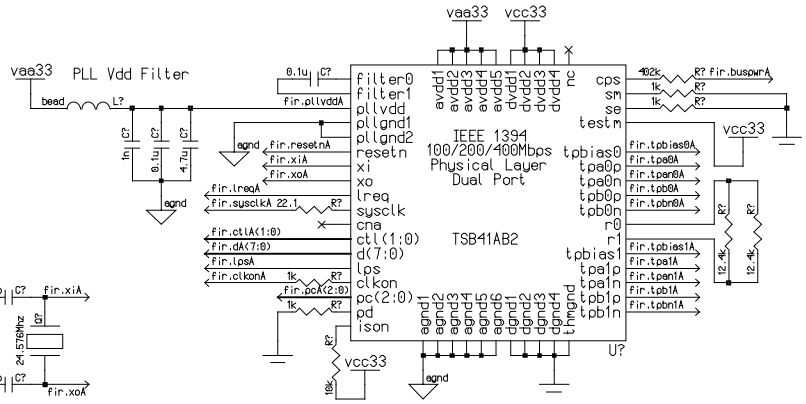


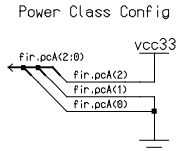
TM-4

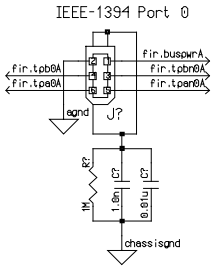
Jos Fiedler
University of Toronto

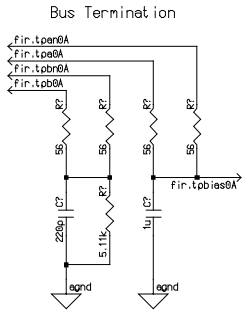
IEEE-1394 (Firewire) Channel A

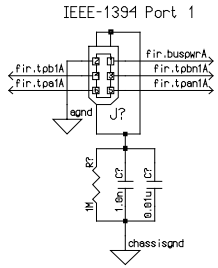


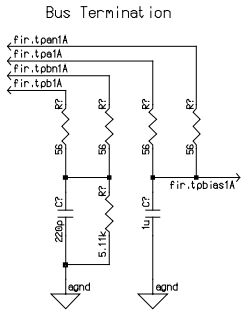


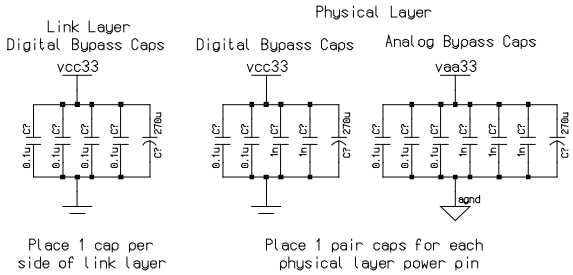


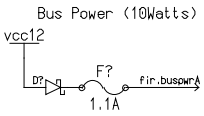


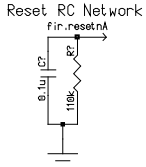






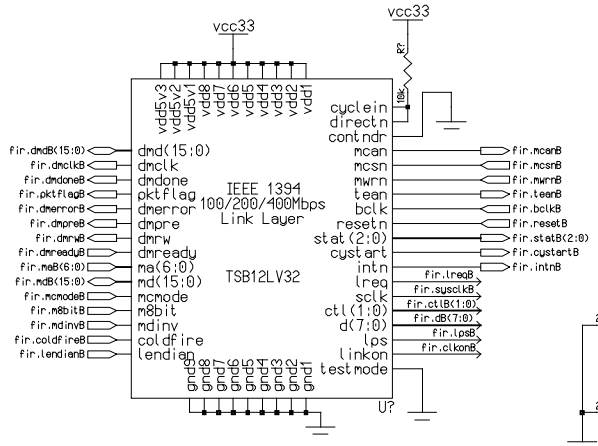


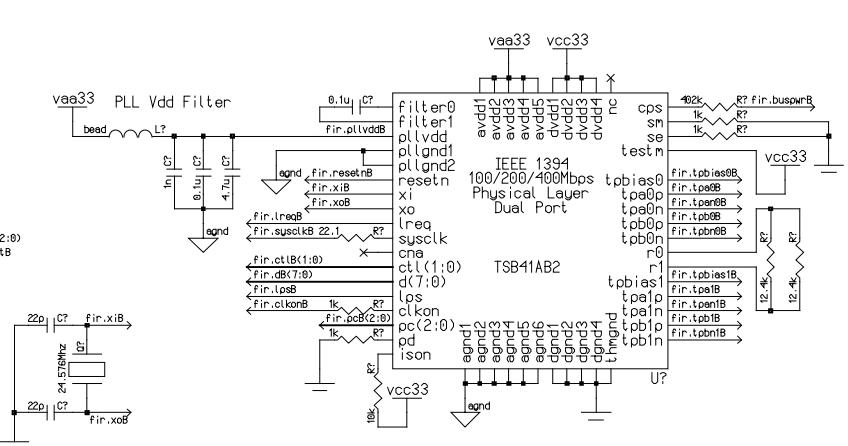


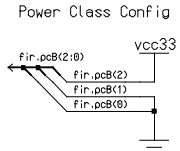


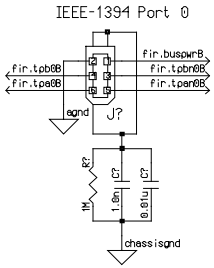
TM-4

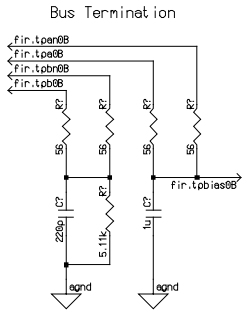
IEEE-1394 (Firewire) Channel B

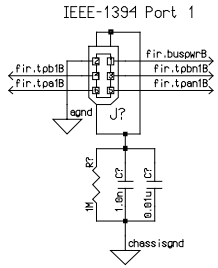


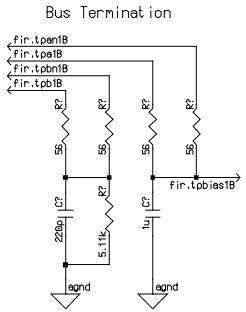


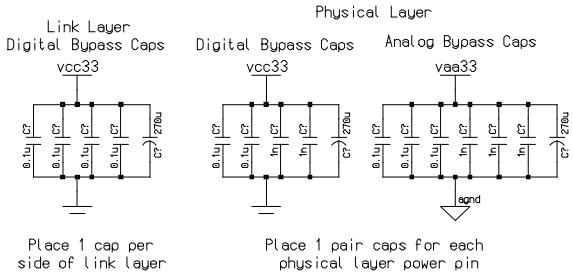


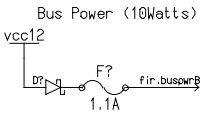


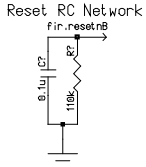












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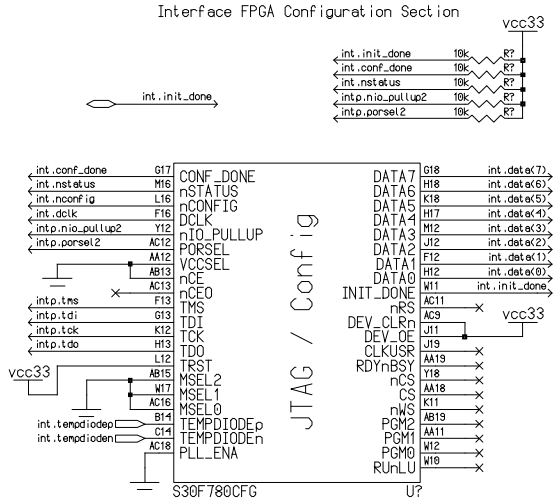
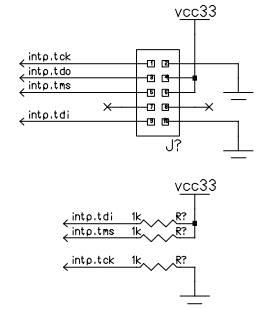
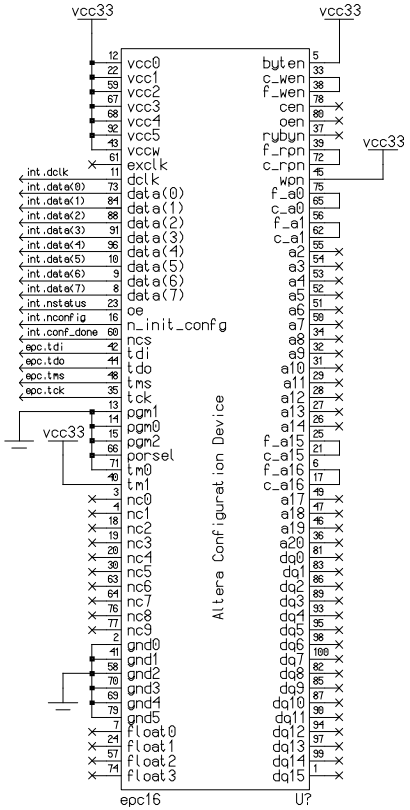
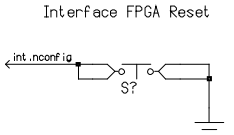
University of Toronto

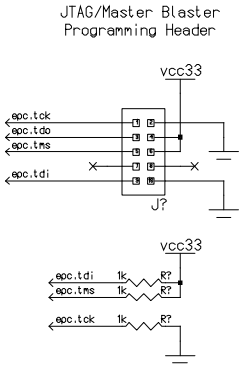
Interface FPGA Device Configuration

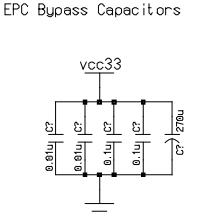












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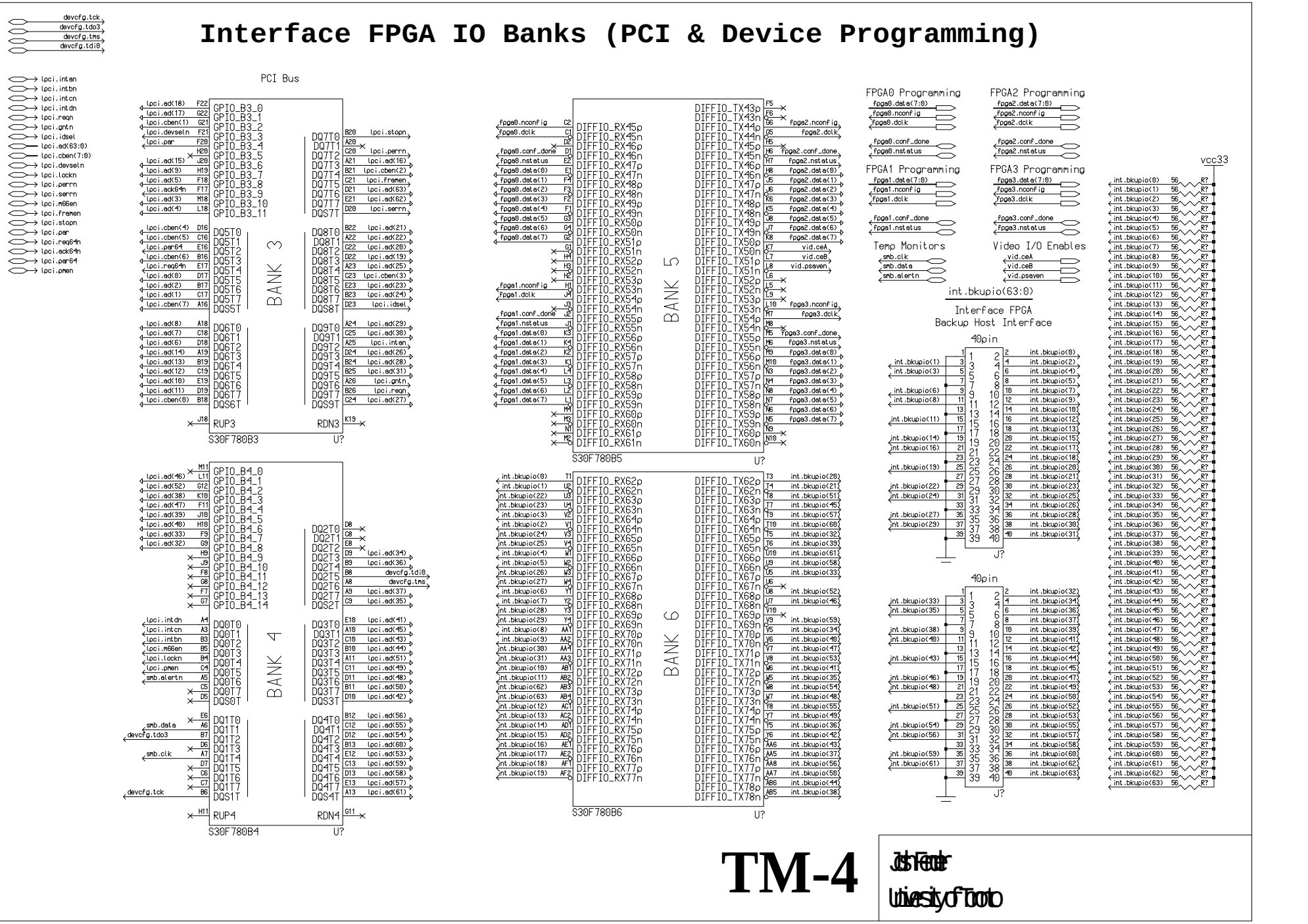
Interface FPGA Configuration
University of Toledo

Interface FPGA IO Banks (PCI & Device Programming)



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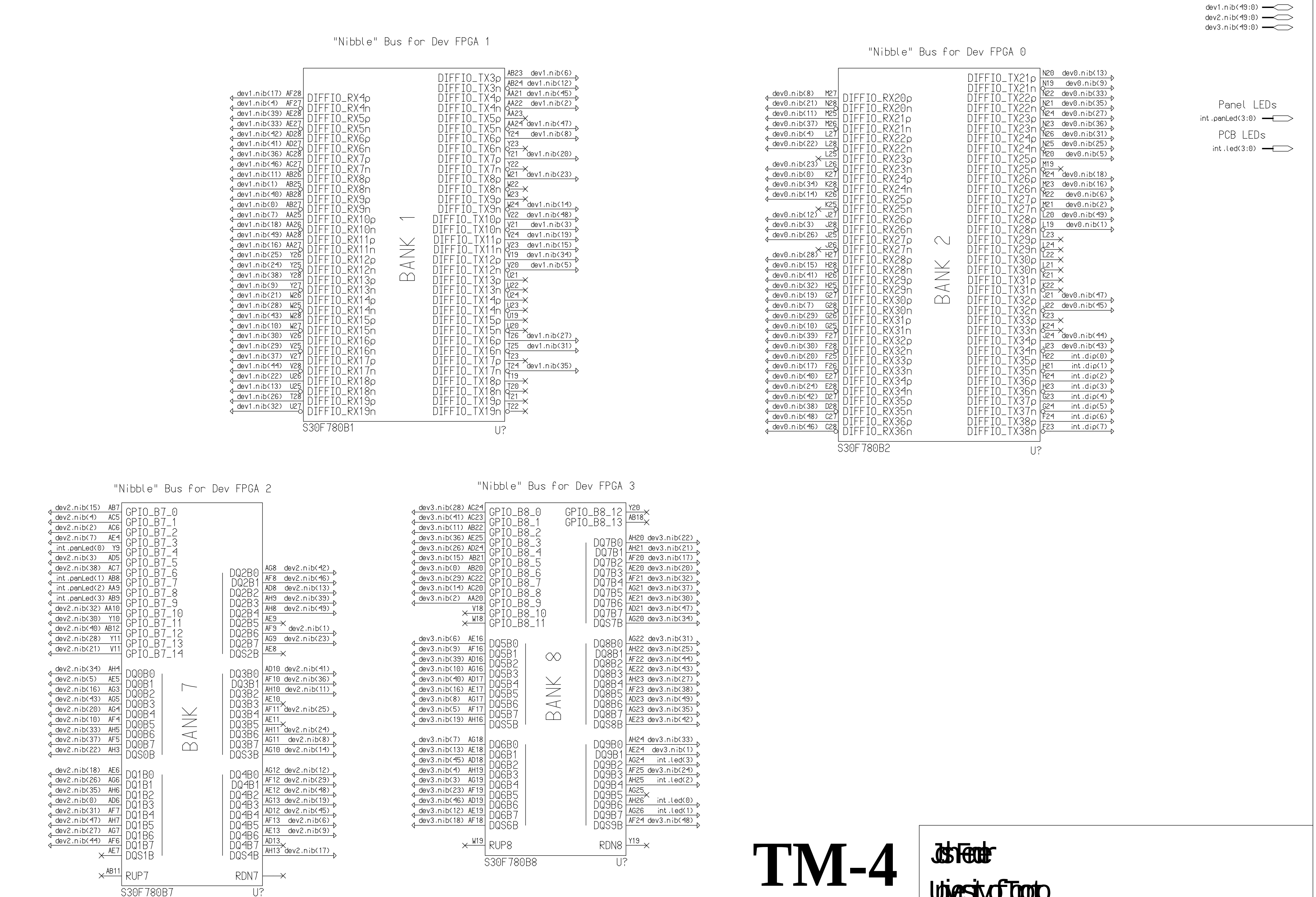
Interface FPGA "Nibble" Bus IO



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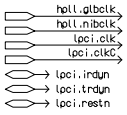
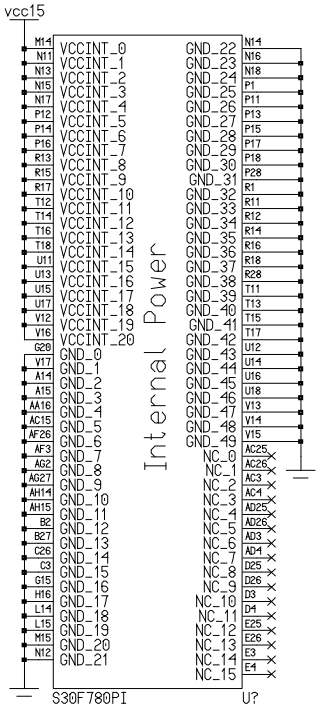
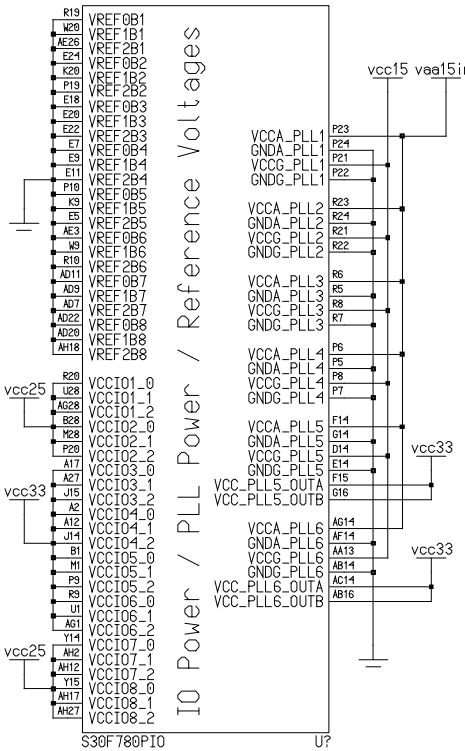
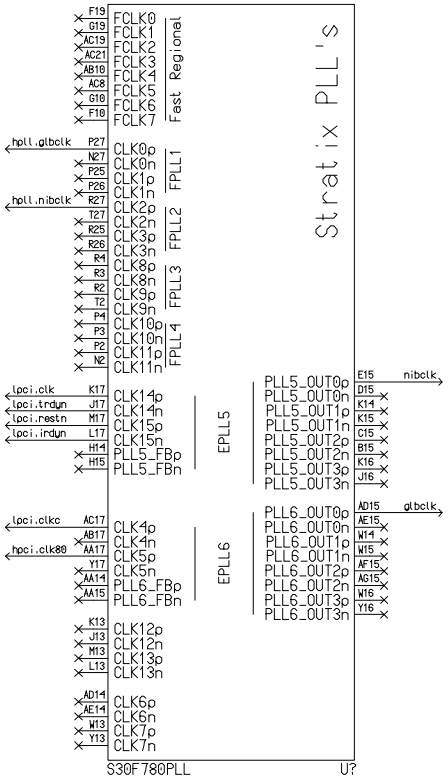
Interface FPGA Power & PLLs

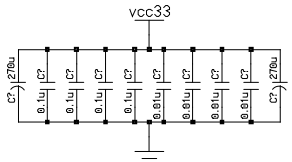




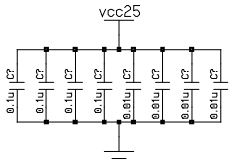




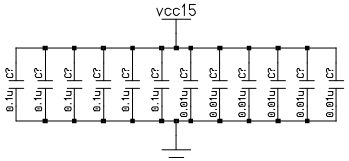
Interface FPGA vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side
Banks 3,4,5 and 6



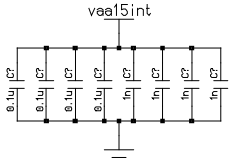
Interface FPGA vccio Bypass Caps 0603
Place near vccio pins of FPGA bottom side
Banks 1,2,7 and 8



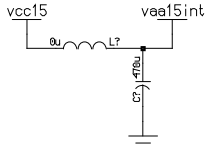
Interface FPGA Vccint Bypass Caps 0603
Place near center of FPGA bottom side



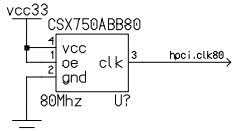
Interface FPGA Vcca_pll Bypass Caps 0603
Place pair by each of 5 power pin groups



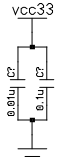
PLL Power Filter



Global Clock Reference



Global Reference Bypass



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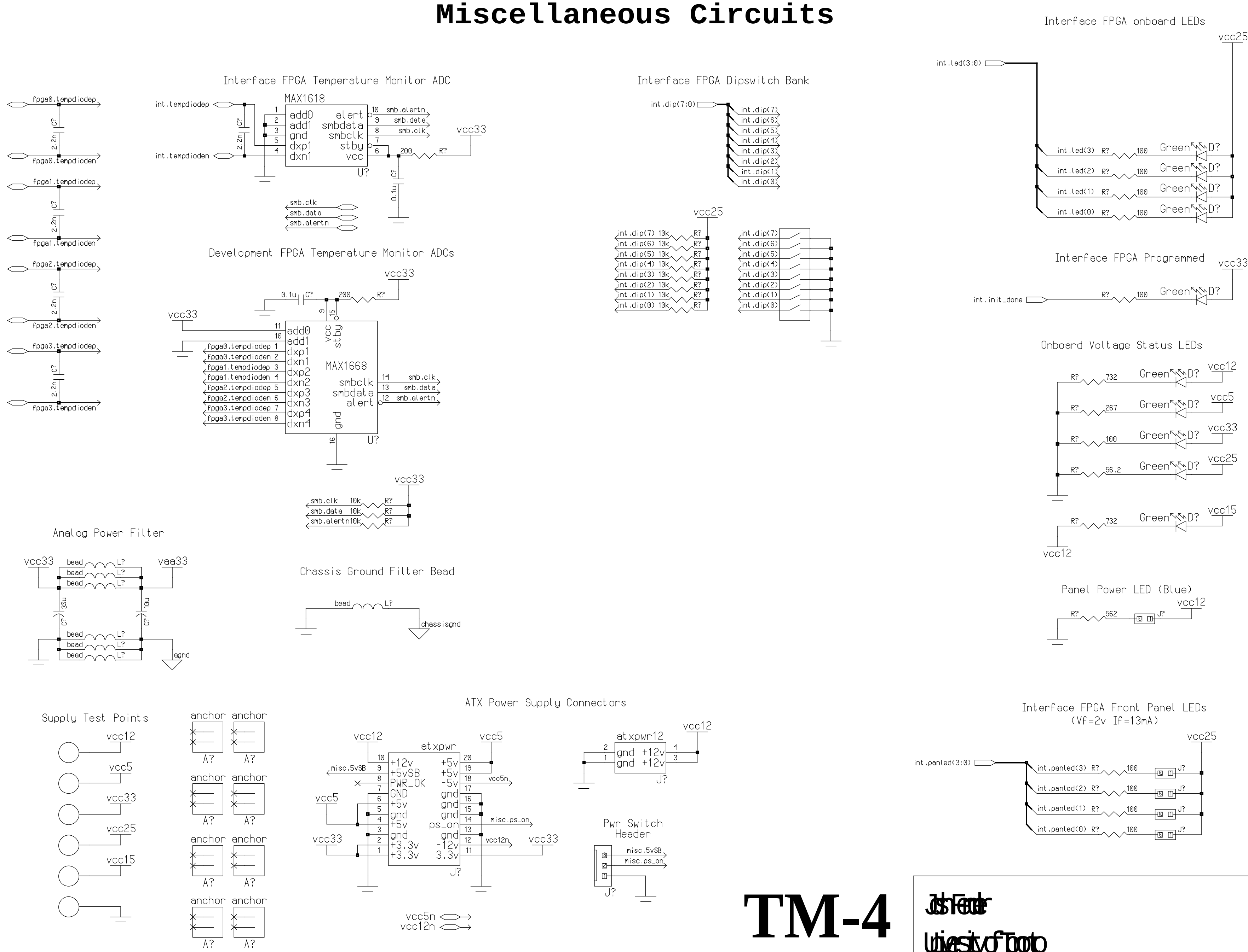
Miscellaneous Circuits



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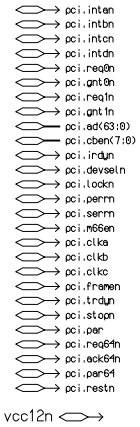
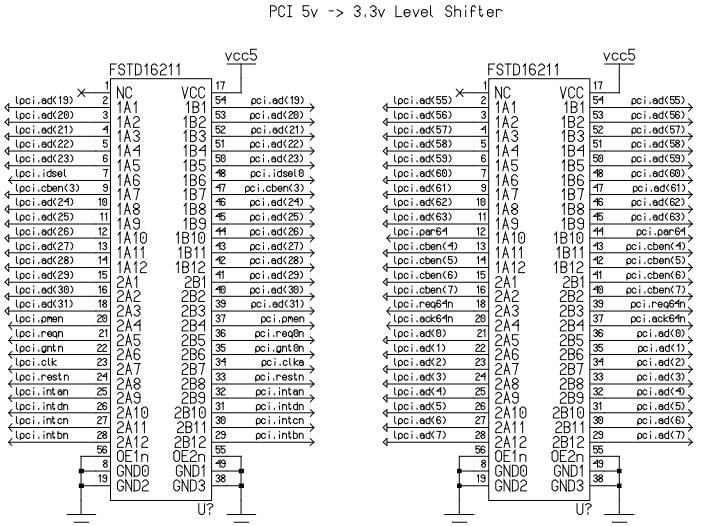
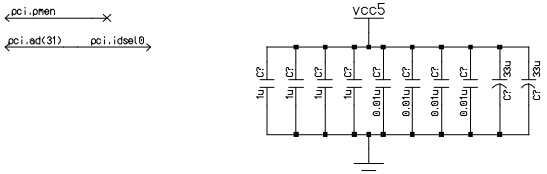
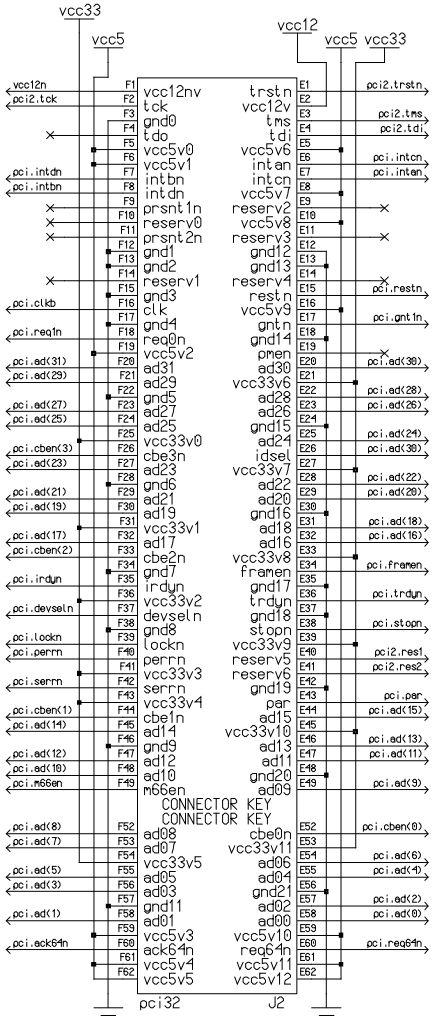
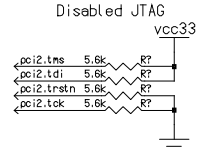
PCI Expansion Slot and Interface FPGA Voltage Converters

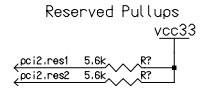


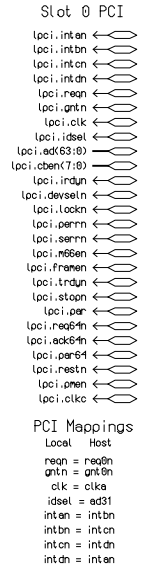


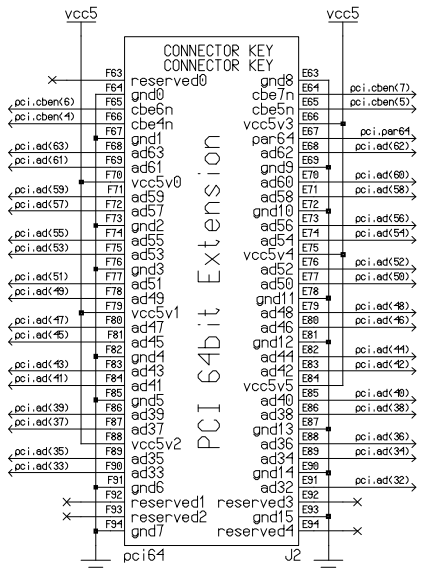












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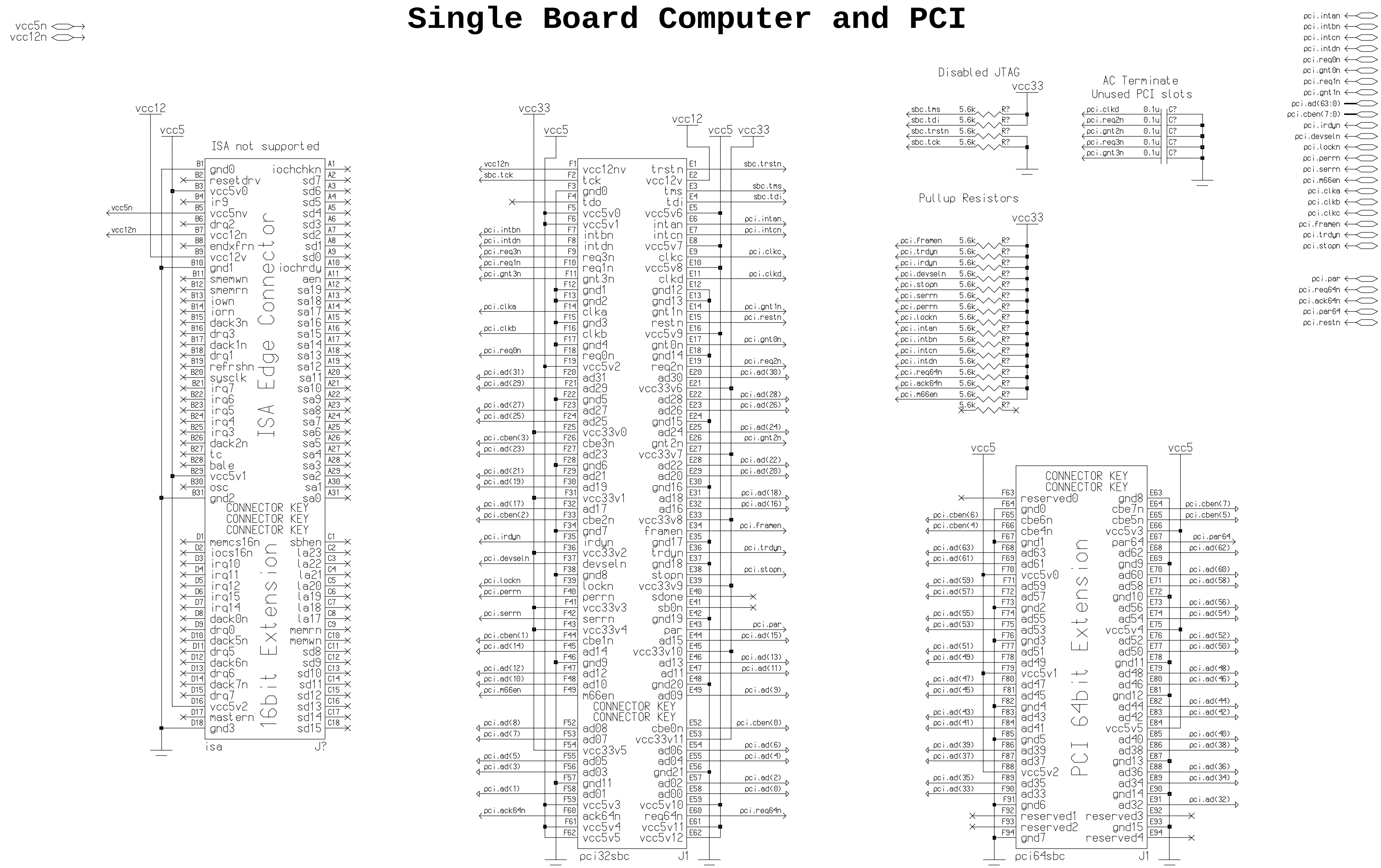
Single Board Computer and PCI



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