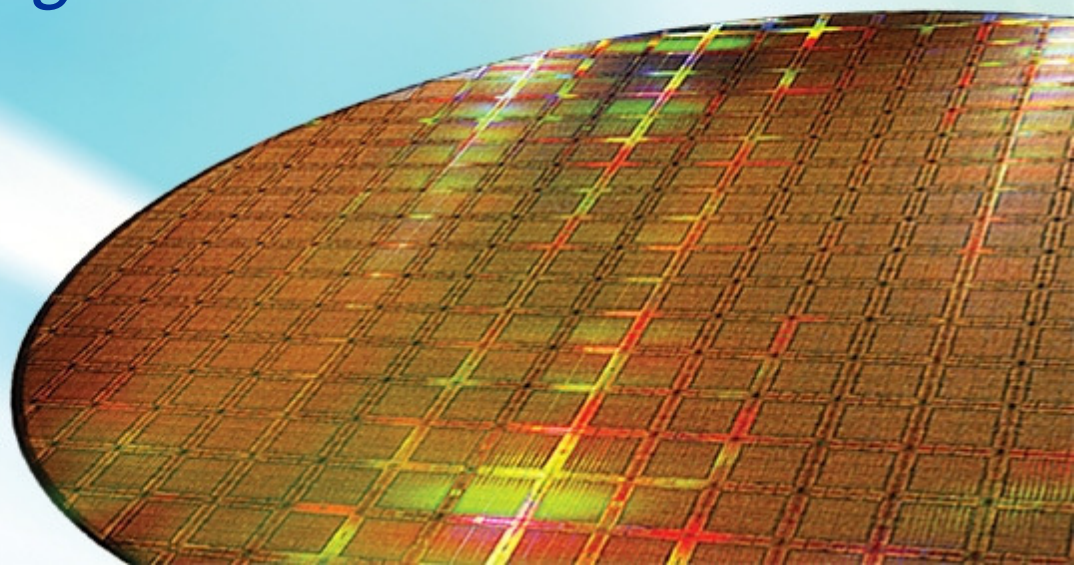
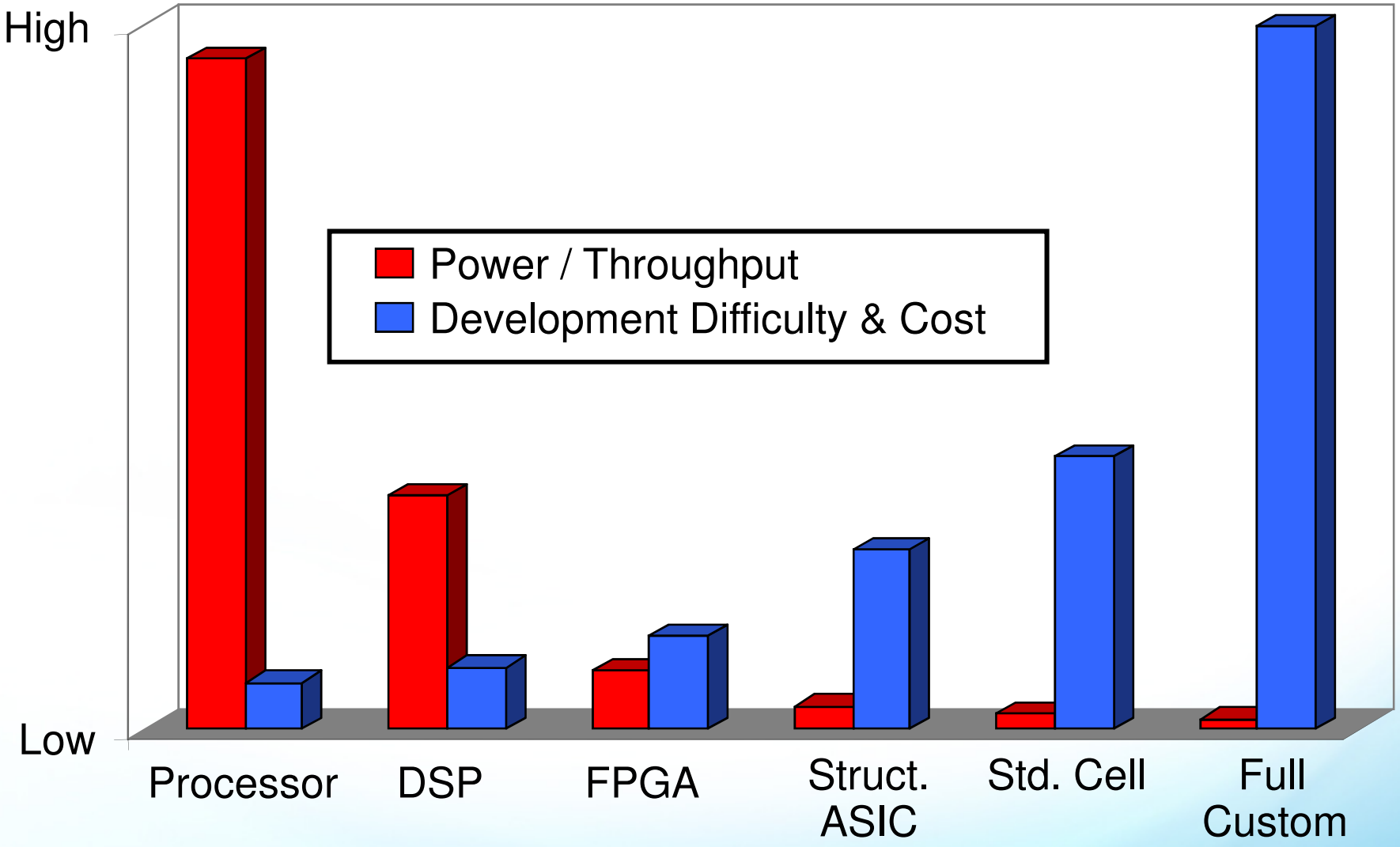
Will Power Kill FPGAs?

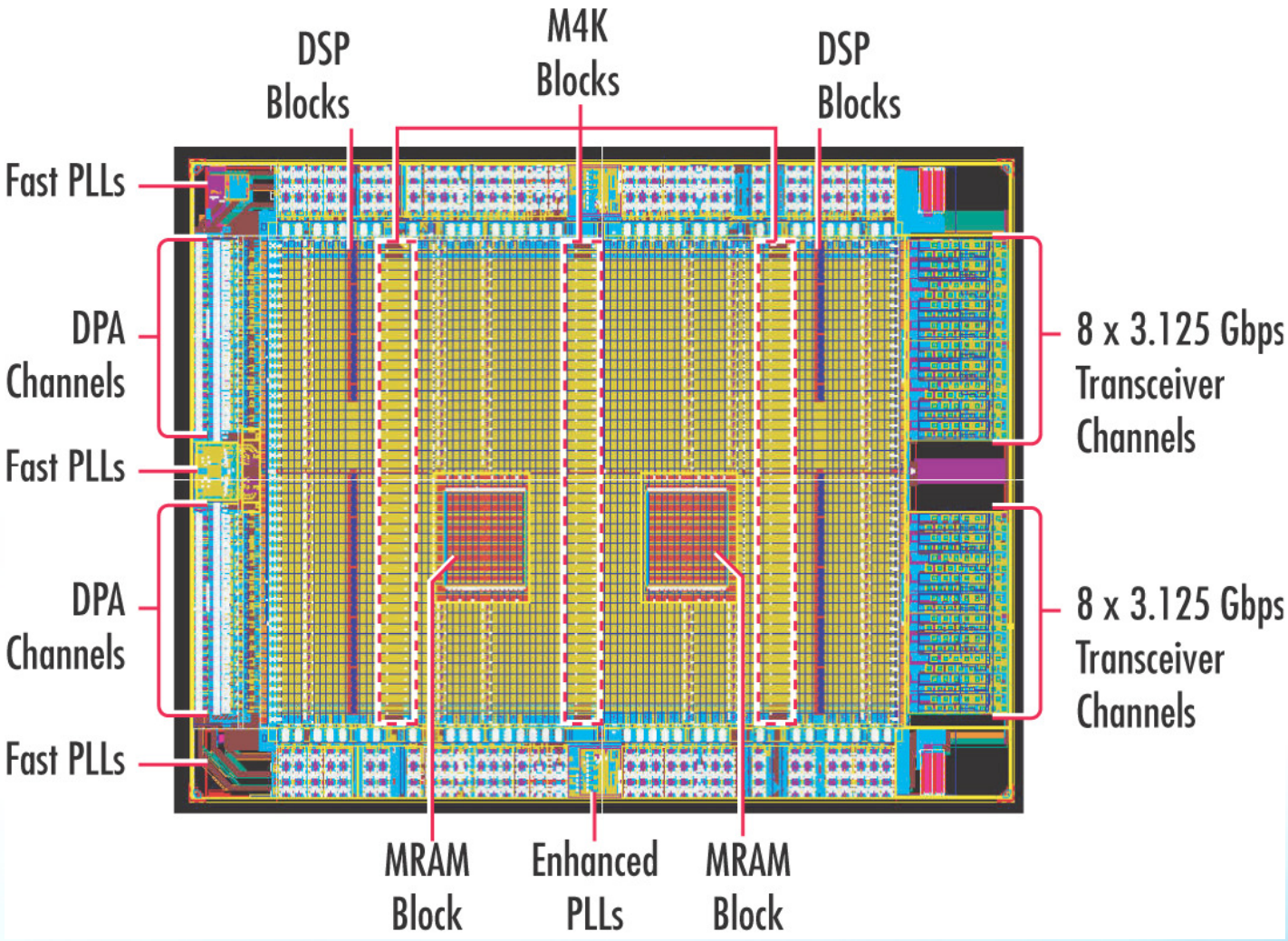
Vaughn Betz



Power vs. Development Cost

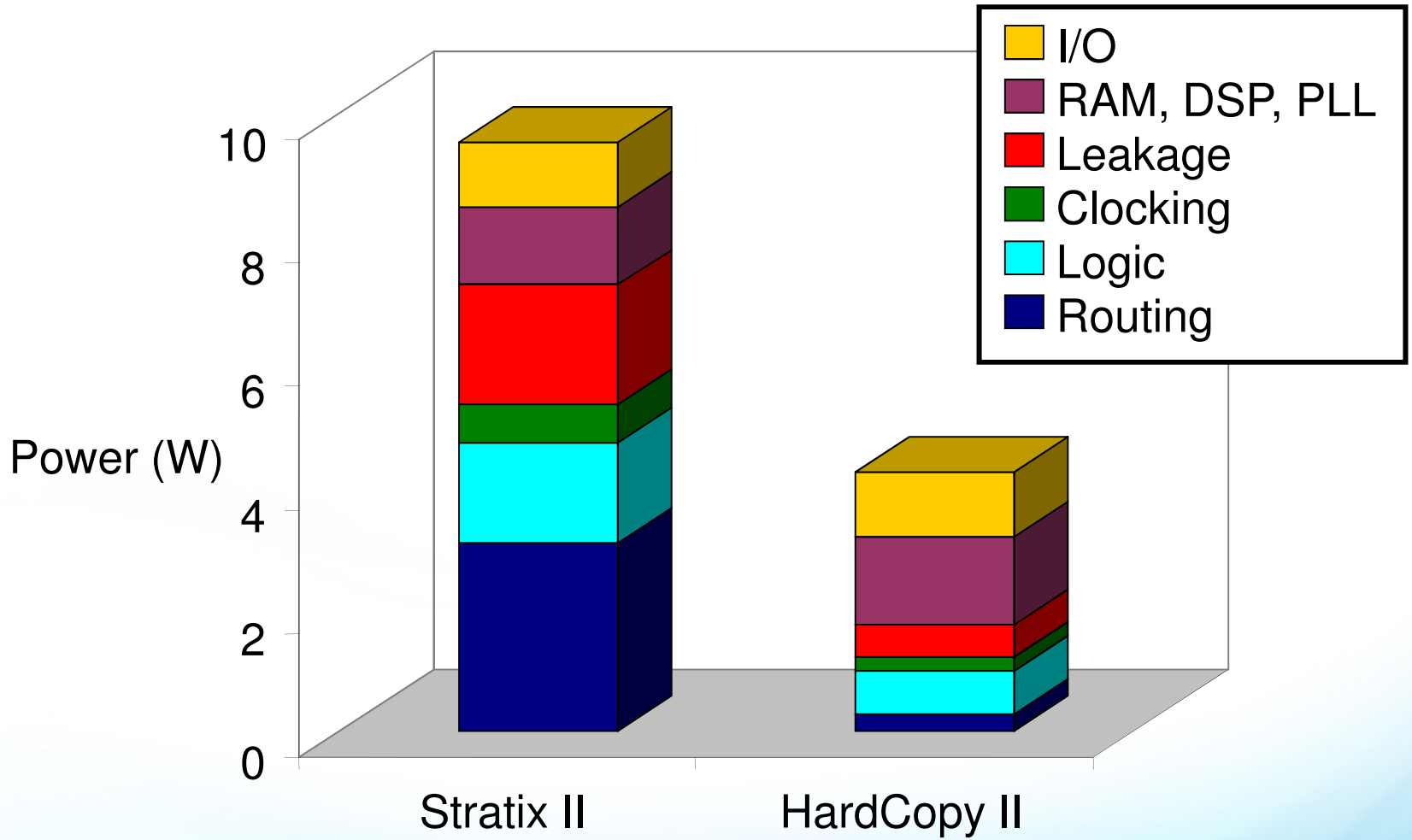


FPGAs: Not Just LUTs & Wires



Costly to verify all these functions in an ASIC

Amdahl's Law for Power



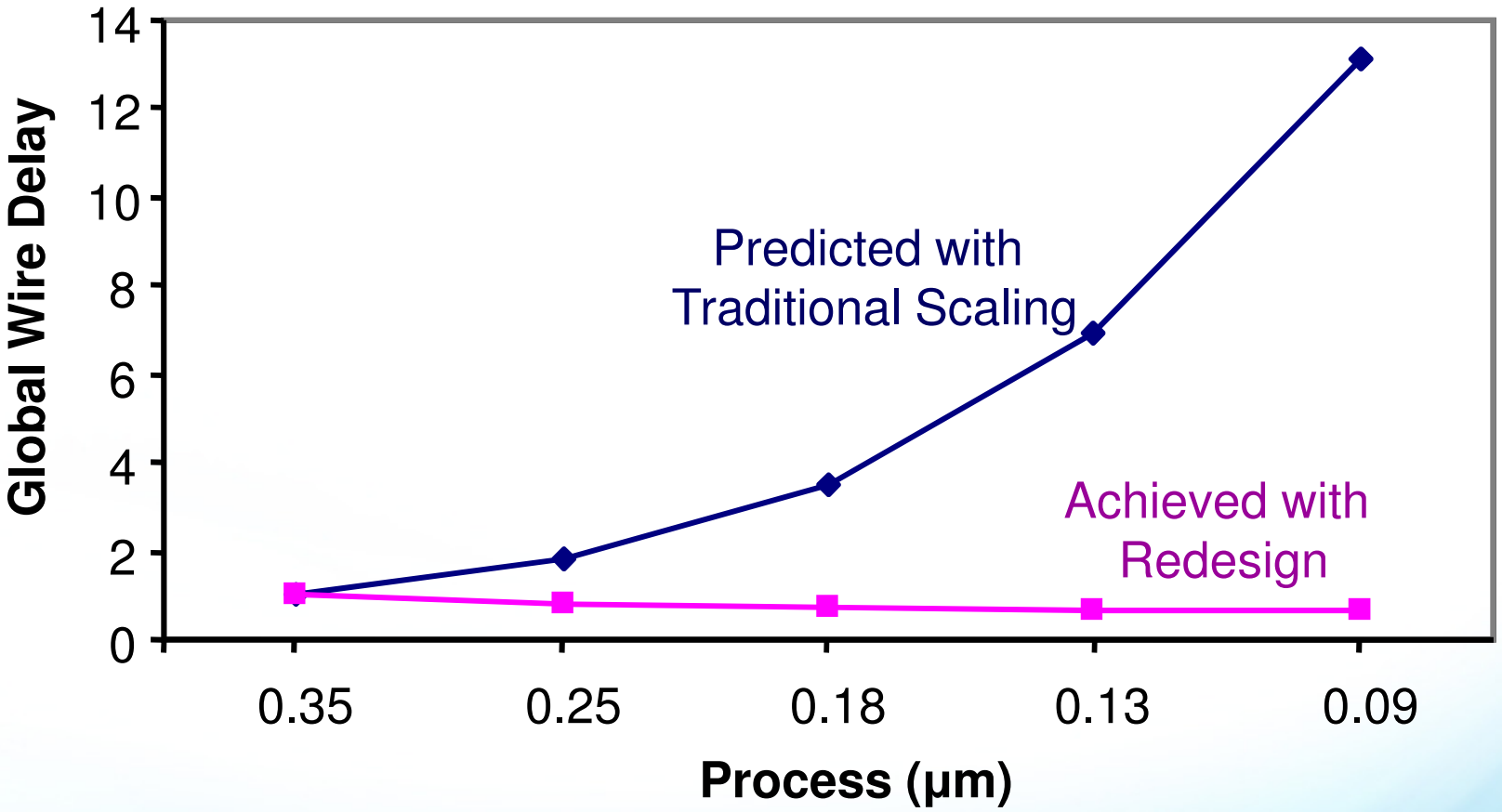
Power Scaling

- 130 nm and above
  - FPGAs scaled without regard to power
  - Got full performance boost of process
- 90 nm and below
  - Power-constrained scaling
  - Low-cost FPGA power budget: ¼ W to 3 W
  - High-speed FPGA: 2 W to 20 W
  - Maximum performance *within power budget*

Controlling Power: Many Ideas

- Trade-off P_{static}, $P_{dynamic}$, performance
  - And sometimes cost
- 90 nm
  - Process parameters
  - FPGA CAD tools optimize for power
  - Innovate on performance, then trade for P_{static}
    - E.g. Stratix II ALM: larger LUT
- 65 & 45 nm
  - More visible knobs
- 32 nm
  - Process will likely have better static power
    - Double-gates FETs, high-K gate dielectric

Don’t Bet Against Innovation

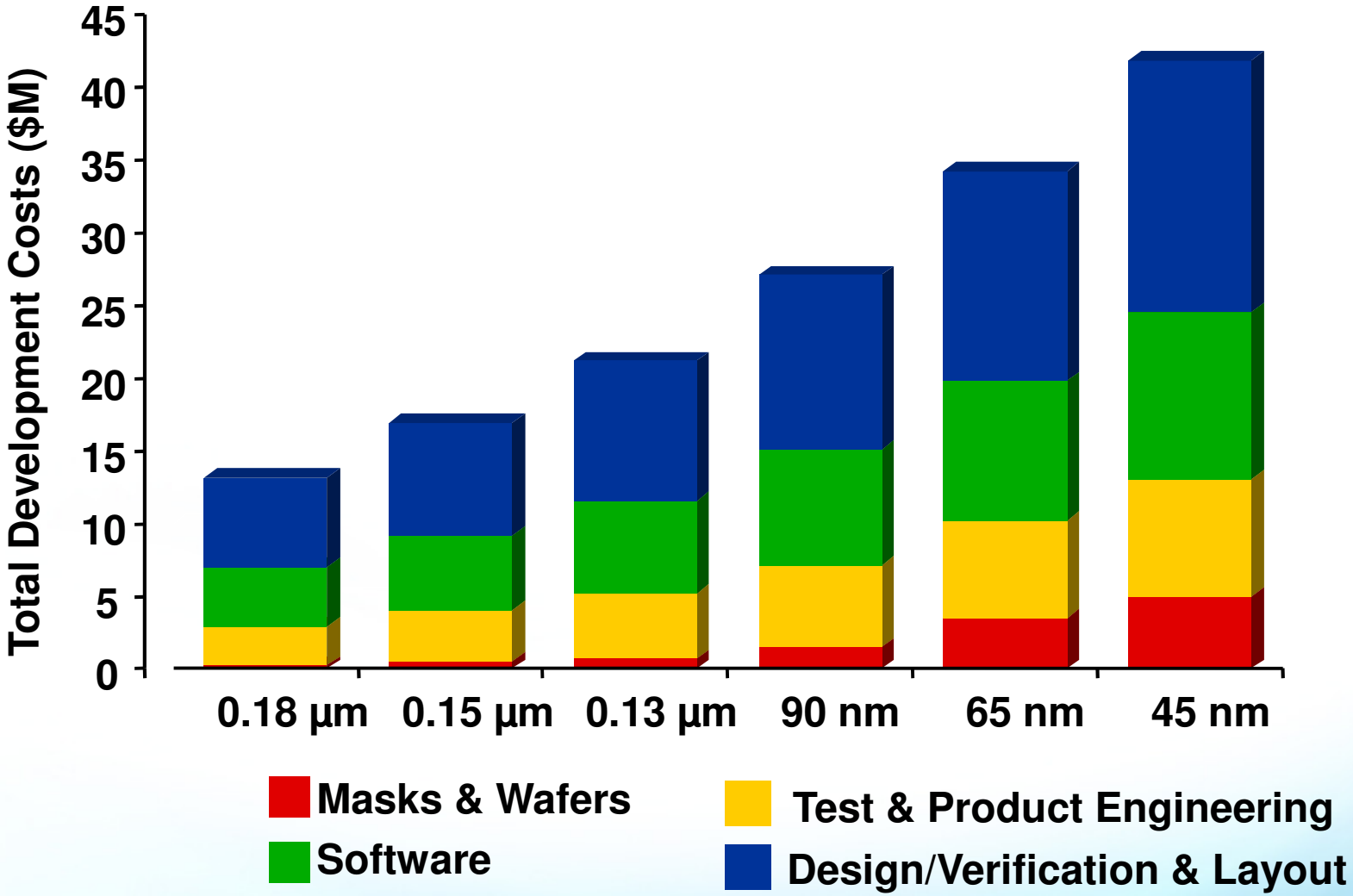


Will Scaling Still Benefit FPGAs?

- Scale process
  - Same power for largest device
  - But twice the capacity
    - ½ power for design migrated to new process
  - Some performance increase
    - But less than traditional 50% / generation
  - Cost reduction
    - Wafers more expensive, but 2X more logic / wafer means lower device cost

Scaling economics still good!

Std Cell ASIC: Development Cost vs. Scaling



Note: Conservative estimate; does not include re-spins.

Summary

- FPGAs have higher power than ASICs
  - Most systems: just a cost adder
    - If a $200 FPGA is OK, so is a $2 heat sink
- Std. cell development costs spiraling upward
  - Only huge markets merit traditional ASIC
- FPGAs: power-constant scaling
  - Scaling economics still work for FPGAs