Research Challenges for FPGAs

Vaughn Betz

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CAD Scalability

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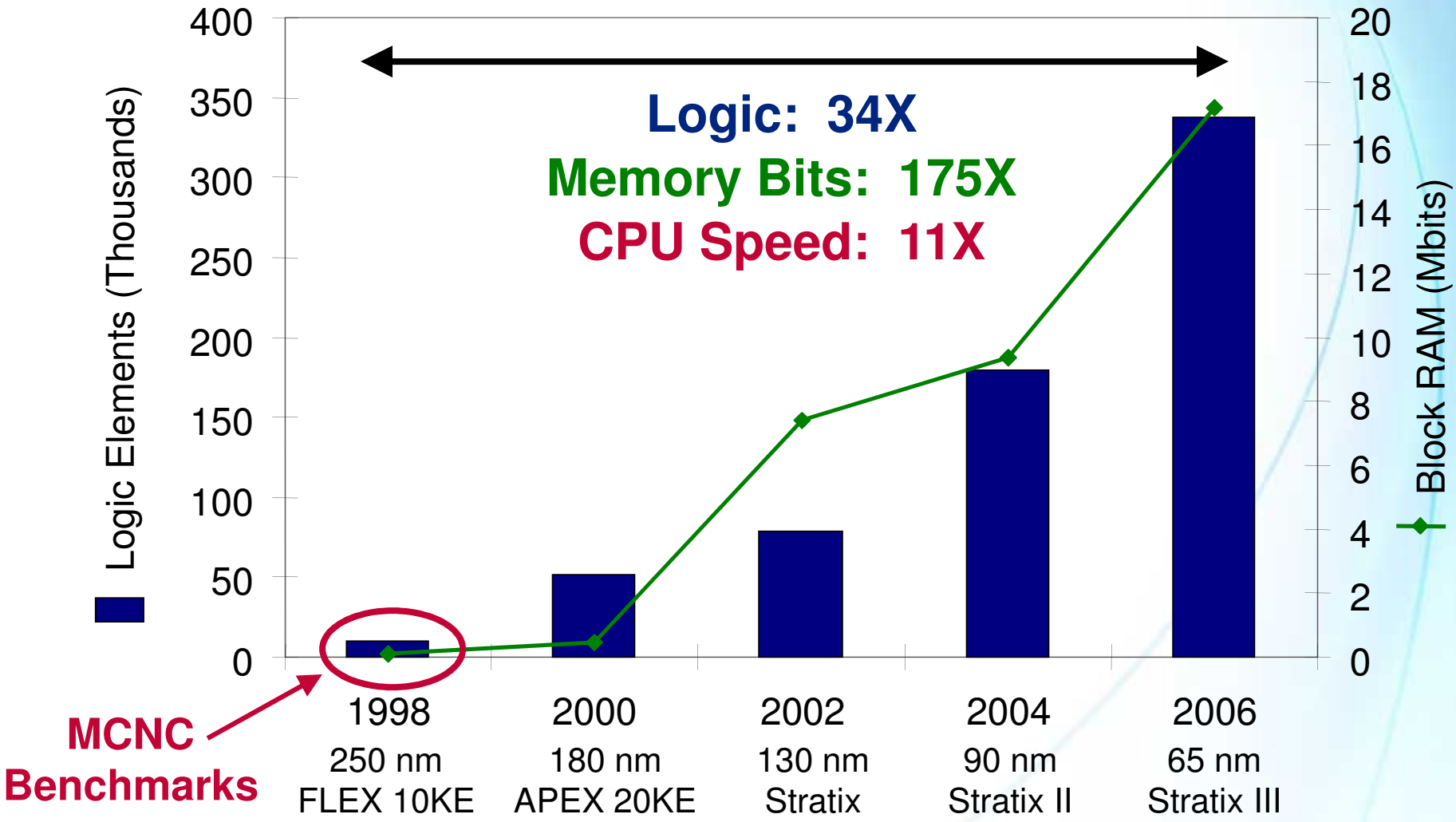
Recent FPGA Capacity Growth



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The Compile Time Challenge

- CAD problem growing faster than CPU speed
  - But productivity of FPGA designers depends on many compiles
- Need to find highly scalable algorithms
  - For **placement,** routing, synthesis
- New methodologies?
  - “Incremental compile” for only changed parts of design?
  - Can help, but still need fast tools
- Don’t sacrifice (much) result quality
  - Otherwise designer productivity suffers
- Need to test algorithms on much larger benchmarks
  - MCNC benchmarks do not fill even FLEX 10K

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Compile Time Future

- Single processor speed-up will fall further behind FPGA capacity growth
- But more cores per chip
  - Today: 2
  - Later this year: 4
- Parallel CAD tools, with same result quality?
- Need *sequentially equivalent* algorithms
  - Always get the same result, regardless of number of processors
  - Otherwise debugging is a nightmare

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Increasing Design Abstraction

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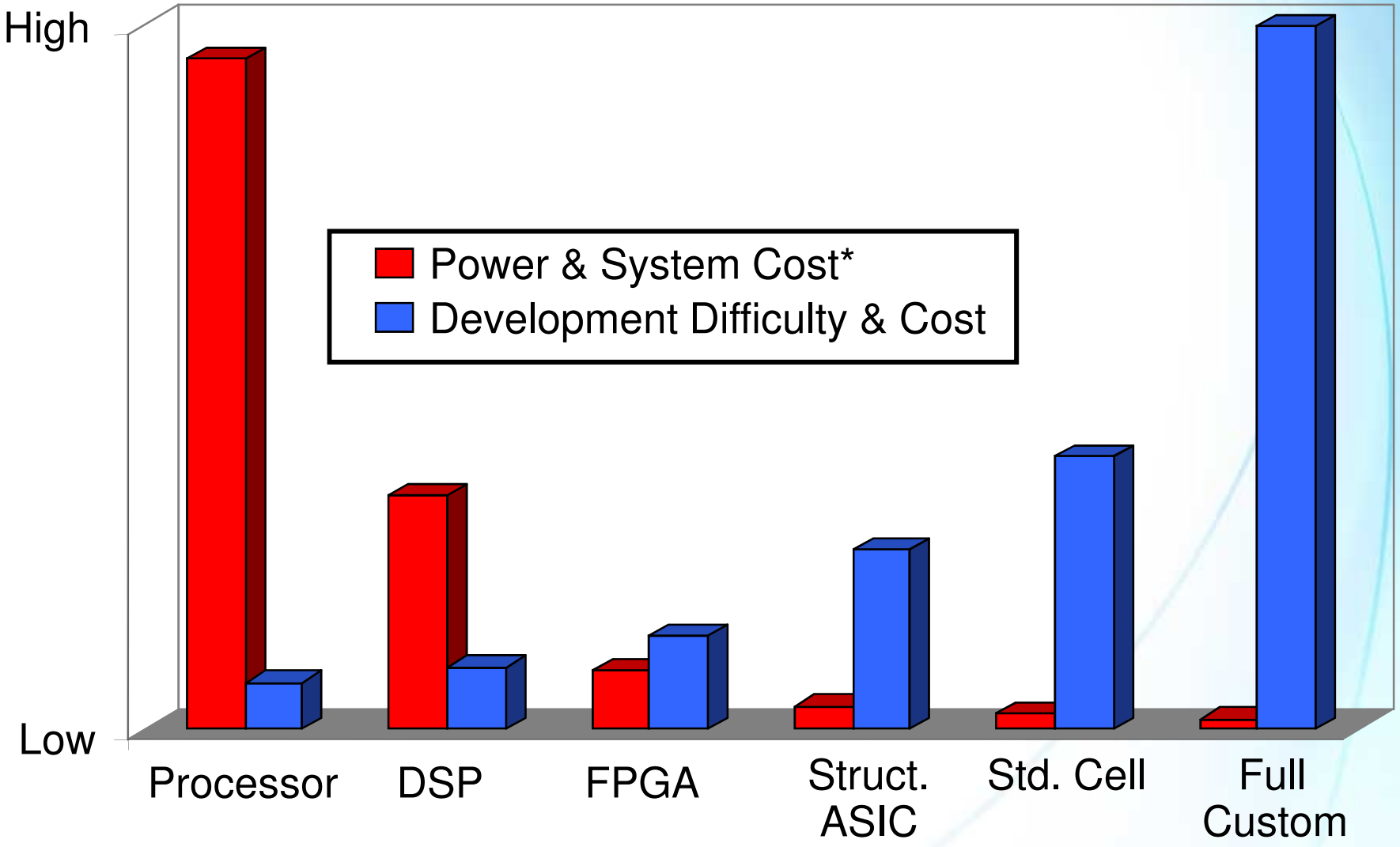
Efficiency vs. Development Cost



*For applications with significant parallelism

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Raising Design Abstraction

- Most FPGA design is in HDL
  - Limits FPGA use to hardware engineers
- Ideal: software engineers can use FPGAs
- Practical: domain-specific higher-level tools
  - IP re-use and push-button integration (e.g. SoPC builder):
    - Build a custom microcontroller
    - Integrate IP cores
  - Hardware accelerator for targeted C code, processor for rest
  - **APIs and libraries** for high performance computing
  - Domain-targeted configurable platforms

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Power

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Power Scaling

- Low-cost FPGA power budget: ¼ W to 3 W
- High-speed FPGA: 2 W to 20 W
- Not much market beyond these ranges
  - Goal: maximum performance *within power budget*
- Large and growing mobile market
  - Need to hit new lows in power to penetrate

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Process Scaling & Power

- Dynamic Power: drops per LE
  - But reduction < 50% / LE
    - Doubling LE count increases power
- Static Power: tends to increase
  - Innovate to reduce
  - If still too high, sacrifice speed by increasing Vt, Tox, and/or L
- Need architecture and CAD for static and dynamic power
  - Compare new ideas to changing process
  - Did you beat the universal speed – power curve?
- How to meet a mobile power budget?
  - Near-zero static (uW)
  - As low as possible dynamic (mW)
- Hard block impact on power

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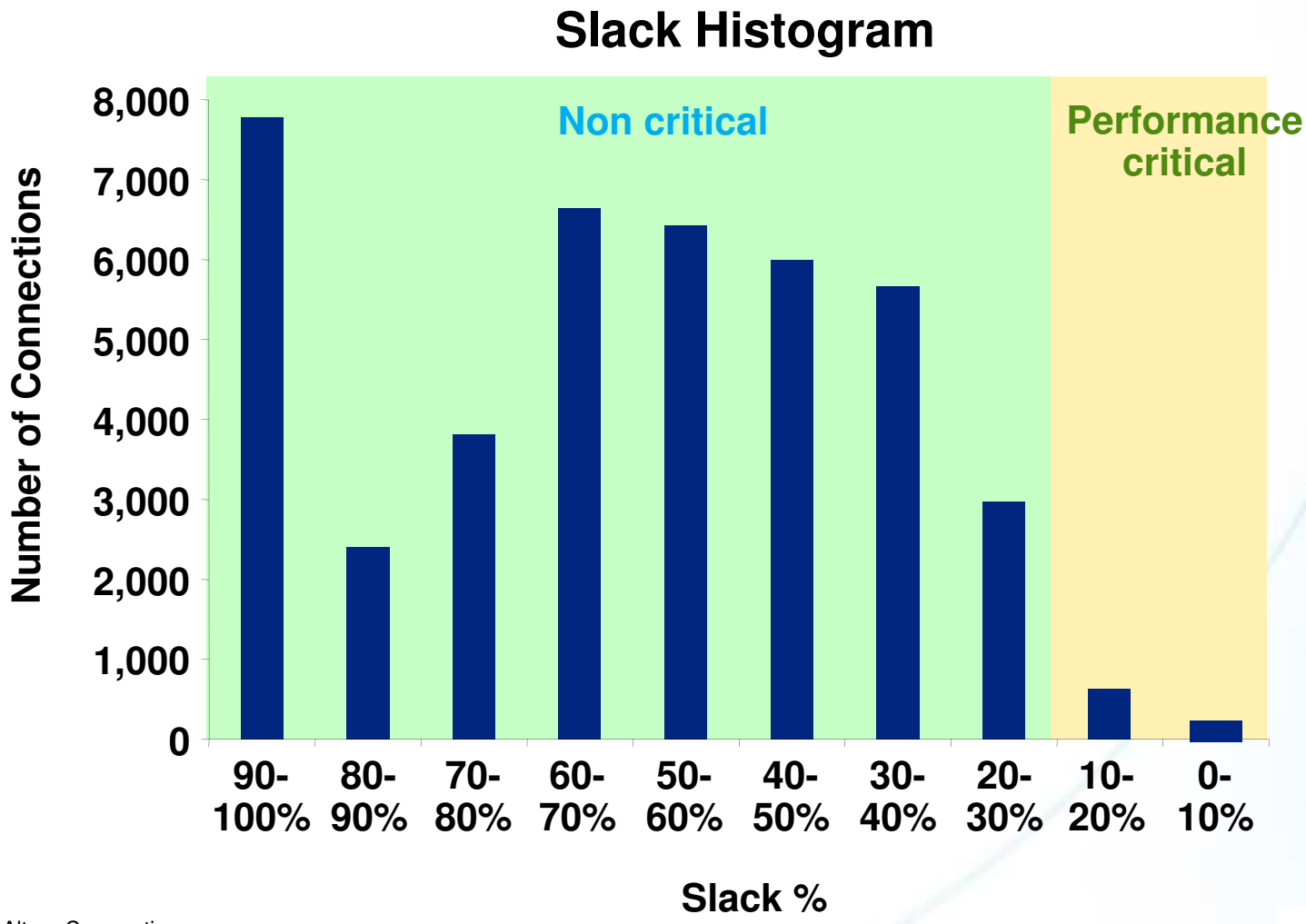
Design-Specific Power Optimization

- Only a small proportion of logic is performance critical



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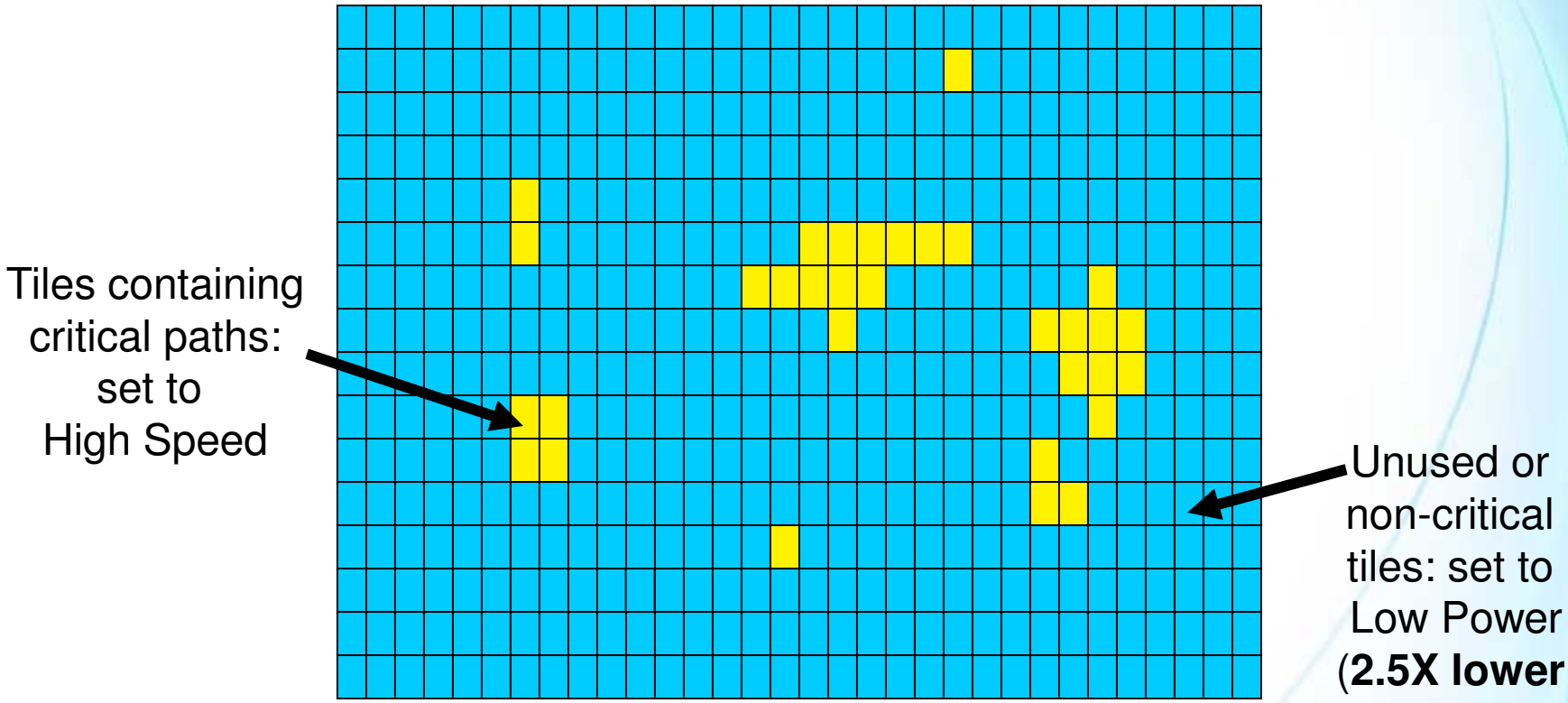
Stratix III Programmable Power™



- High Speed tiles define device speed
- Static power mostly determined by low power tiles
- Speed / power tradeoff adapts to user design

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I/O Architecture

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I/O Architecture

- Fast, programmable I/O is key
  - FPGA communicates with everything
- Cost
  - 20% to 48% of Stratix II die is I/O, PLL and related circuitry
  - Significant fraction of power consumption
- FPGA I/Os are unique
  - Stratix II I/Os support 28 different standards
- Supporting higher voltage standards: use thicker oxide transistors
  - Not optimal for lower voltage standards
- I/O speed requirements increasing

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I/O Ideas

- Clever circuit structures?
  - E.g. support higher voltage standards using thin-oxide transistors?
- Share / remove some circuitry?
- Specialize some I/Os?
  - Faster, lower power, less area
  - Too much: don't meet needs or can't lay out the circuit board

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